METHOD FOR REDUCING PATTERN DEFORMATION AND PHOTORESIST POISONING IN SEMICONDUCTOR DEVICE FABRICATION

BACKGROUND OF THE INVENTION

Field of the invention

Embodiments of the invention relate to semiconductor fabrication, and in particular, to methods of eliminating pattern deformation in semiconductor devices.

Related Art

The use of amorphous carbon film as part of a hardmask stack for patterning MOSFET features has been found to be beneficial due to the ease with which amorphous carbon may be patterned and the high selectivity of amorphous carbon relative to typically used capping or protective materials such as silicon oxide, silicon nitride and silicon oxynitride. Figure 1 shows a structure including amorphous carbon that may be used in the formation of a MOSFET. The structure includes a semiconductor substrate 2 having field oxides 4 that bound source/drain regions of a MOSFET. A layer of a gate insulating material 6 such as SiO_2 is formed over the substrate. A layer of a gate conductive material 8 such as doped polysilicon is formed over the substrate and will be patterned to form a gate line of the MOSFET. Formed over the gate conductive layer 8 is a hardmask stack including an amorphous carbon layer 10 and a capping material layer 12 such as SiON. A photoresist mask 14 for defining the pattern of the gate is formed on the SiON capping material layer 12. During processing, a first etch is used to transfer the photoresist mask pattern to the SiON layer, a second etch is used to transfer the SiON mask pattern to the amorphous carbon layer, a third etch is used to remove oxide from the surface of the gate conductive layer, and a further etches are performed to etch the underlying gate conductive layer using the SiON and amorphous carbon patterns as a hardmask.

One problem with the structure of Figure 1 is that the amorphous carbon material has relatively poor selectivity with respect to the polysilicon gate conductive material during the polysilicon etch, and as a result the amorphous carbon is also etched during etching of the polysilicon, resulting in degradation of the transferred pattern. A proposed solution to this problem is to dope the amorphous carbon with nitrogen, which enhances its selectivity with respect to polysilicon.

However, the nitrogen doping technique creates other problems that become more significant as device dimensions are reduced. One problem involves poisoning of the photoresist with nitrogen from the amorphous carbon layer. Poisoning is enabled by pinholes in the SiON cap layer that randomly occur during SiON deposition. The pinholes extend partly or entirely through the SiON layer, enabling nitrogen dopant from the amorphous carbon to diffuse into the photoresist. Poisoned photoresist is difficult to remove by conventional developing techniques and therefore the poisoned photoresist degrades the quality of the photoresist mask. As SiON cap layers become thinner, the poisoning problem becomes more pronounced.

A second problem of amorphous carbon is delamination of etched amorphous carbon from the underlying polysilicon. Figures 2a and 2b illustrate this problem. Figure 2a shows a top view of a patterned amorphous carbon line. The line is subject to compressive forces 16 resulting from differences in the thermal expansion coefficients of amorphous carbon, polysilicon and SiON. As the width of the line decreases relative to its length, the compressive forces along the length of the line become significantly greater than those across the width of the line. So long as a SiON top layer is present on the amorphous carbon line, the compressive forces do not deform the line. However, during typical processing, an etch for removing oxide from the

polysilicon layer is performed after patterning the amorphous carbon, and this etch typically removes most or all of the SiON overlying the amorphous carbon line. At that point the internal compressive forces of the amorphous carbon are no longer restrained, and the amorphous carbon delaminates from the underlying polysilicon and may assume a "squiggle" pattern as shown in Figure 2b that effectively lengthens the line to relieve compressive stress. This pattern will be reproduced in the polysilicon upon further etching, resulting in a deformed gate line. The severity of this problem is enhanced by nitrogen doping.

Consequently, there is a need for methods that reduce pattern deformation and photoresist poisoning while maintaining the desirable etch selectivity properties of nitrogen doped amorphous carbon.

SUMMARY OF THE DISCLOSURE

It is an object of the present invention to reduce pattern deformation in semiconductor device fabrication.

In accordance with one preferred embodiment of the invention, a hardmask stack is comprised of alternating layers of doped amorphous carbon and undoped amorphous carbon. The undoped amorphous carbon layers serve as buffer layers that constrain the effects of compressive stress within the doped amorphous carbon layers to prevent delamination. The stack is provided with a top capping material layer. The layer beneath the capping material layer is preferably undoped amorphous carbon to reduce photoresist poisoning.

In accordance with a second preferred embodiment, a hardmask stack is comprised of alternating layers of a capping material and amorphous carbon. The amorphous carbon layers may be doped or undoped. The capping material layers serve as buffer layers that constrain the effects of compressive stress within the amorphous carbon layers to prevent delamination. The top layer of the stack is formed of the capping material. The layer beneath the capping layer is preferably undoped amorphous carbon to reduce photoresist poisoning. The lowest layer of the hardmask stack is preferably amorphous carbon to facilitate easy removal of the hardmask stack from the underlying materials by an ashing process.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention will hereafter be described with reference to the accompanying drawings.

Figure 1 shows a structure formed during fabrication of a semiconductor device using an amorphous carbon layer.

Figures 2a and 2b illustrate doped amorphous carbon line deformation.

Figures 3a and 3b show structures formed during fabrication of a semiconductor device in accordance with a first preferred embodiment of the invention.

Figure 4 shows a process flow encompassing the first preferred embodiment and alternative embodiments.

Figures 5 shows a structure formed during fabrication of a semiconductor device in accordance with a second preferred embodiment of the invention.

Figure 6 shows a process flow encompassing the second preferred embodiment and alternative embodiments.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figures 3a and 3b show alternative structure formed in accordance with a first preferred embodiment of the invention.

The structure of Figure 3a includes a semiconductor substrate 2 having field oxides 4 that bound source/drain regions of a MOSFET. Layers of a gate insulating material 6 such as SiO_2 and a gate conductive material 8 such as doped polysilicon are formed over the substrate and will be patterned to form a gate line and gate insulator of the MOSFET. Formed over the gate conductive layer 8 is a hardmask stack including an amorphous carbon portion formed in contact with the underlying polysilicon. The amorphous carbon portion is comprised of discrete alternating layers of doped amorphous carbon 22 containing dopant such as nitrogen for enhancing its etch selectivity relative to the polysilicon, and undoped amorphous carbon 20 that contains essentially none of the etch selectivity enhancing dopant of the doped layers 22. A capping layer 12 of SiON, silicon oxide or silicon nitride is formed over the amorphous carbon portion of the hardmask stack, and a photoresist mask 14 for defining the pattern of the gate line is formed on the capping layer 12. The total height of the hardmask stack is preferably approximately 500 angstroms.

The structure of Figure 3a differs from the structure of Figure 1 in its use of undoped amorphous carbon layers 20 in conjunction with one or more doped amorphous carbon layers 22. The undoped layers 20 serve as buffering layers that constrain the compressive stresses within the doped layers 22 to prevent delamination. While any number and order of doped and undoped layers may be employed in accordance with this embodiment, it is preferred to provide an uppermost layer of undoped amorphous carbon in contact with the capping layer to reduce photoresist poisoning, and to provide a lowermost layer of undoped amorphous carbon formed on the underlying polysilicon layer to increase resistance to delamination.

The layers of the amorphous carbon portion illustrated in Figure 3a are formed as discrete layers in independent processing steps. In an alternative to the structure of Figure 3a, the doped and undoped layers may be formed as continuous layers as illustrated in Figure 3b. This is done by varying dopant source gas flow rates during a single continuous deposition process to produce a dopant profile having a desired gradient through the amorphous carbon portion of the hardmask.

Further alternatives to the structures of Figures 3a and 3b may employ a greater number of layers of doped and undoped amorphous carbon, and may arrange those layers in a different order, such as by having a doped layer formed on the underlying polysilicon. In further embodiments, alternative capping materials such as silicon rich oxide, or silicon rich nitride may be employed. In still further embodiments, such hardmask structures may be formed over a different material to be etched, such as a metal wiring layer, or may be used to form a different type of patterned structure, such as a contact or interconnect.

Figure 4 shows a process flow for manufacture of a semiconductor device encompassing the first preferred embodiment, its aforementioned alternatives, and further alternative embodiments not explicitly discussed. Initially a substrate comprising an upper layer of material is provided (30). A hardmask stack is then formed on the upper layer of material (32). The hardmask stack is comprised of an amorphous carbon portion formed in contact with the layer of material, and a capping layer formed on the amorphous carbon portion. The amorphous carbon portion is comprised of alternating layers of doped amorphous carbon

containing dopant for enhancing etch selectivity with respect to the material, and undoped amorphous carbon that contains essentially none of the dopant.

A photoresist mask is then formed over the hardmask (34). The photoresist mask may be trimmed by a photoresist trimming process. The hardmask stack is then etched using the photoresist mask as an initial etch mask to form a hardmask for patterning the underlying material (36).

Further processing may also be performed such as patterning the upper layer of material and removing the hardmask.

Figure 5 shows a structure formed in accordance with a second preferred embodiment of the invention.

The structure of Figure 5 includes a semiconductor substrate 2 having field oxides 4 that bound source/drain regions of a MOSFET. Layers of a gate insulating material 6 such as silicon oxide and a gate conductive material 8 such as doped polysilicon are formed over the substrate. The gate conductive layer 8 will be patterned to form a gate line of a MOSFET. Formed over the gate conductive layer 8 is a hardmask stack including alternating layers of amorphous carbon 40 and a layer of a capping material 42 such as silicon oxide, silicon nitride, or silicon oxynitride. The amorphous carbon may be doped or undoped. A photoresist mask 14 for defining the pattern of the gate line is formed on the upper layer of capping material. The total height of the hardmask stack is preferably approximately 500 angstroms. The layers of capping material are preferably 20 - 50 angstroms in height.

The structure of Figure 5 differs from the structure of Figure 1 in its use of multiple alternating layers of amorphous carbon and capping material. The layers of capping material 42 serve as buffering layers that constrain compressive stresses within amorphous carbon layers 40 to prevent delamination. While the uppermost layer of capping material will typically be removed during the course of etching the hardmask, the remaining layer or layers of capping material will remain to resist delamination.

It is preferable to form the lowermost layer of the hardmask stack from amorphous carbon in order to enable removal of the hardmask by an ashing process, and to form the uppermost amorphous carbon layer of the hardmask stack from undoped amorphous carbon to reduce photoresist poisoning. However, in alternative embodiments the lowermost layer may be formed of a capping material, and the uppermost amorphous carbon layer may be doped. In further embodiments, alternative capping materials such as silicon rich oxide, or silicon rich nitride may be employed, and different capping materials may be used in different layers within the same hardmask stack. In still further embodiments, such hardmask structures may be formed over a different material to be etched, such as a metal wiring layer, or may be used to form a different type of patterned structure, such as a contact or interconnect.

Figure 6 shows a process flow for manufacture of a semiconductor device encompassing the second preferred embodiment, its aforementioned alternatives, and further alternative embodiments not explicitly discussed. Initially a substrate comprising an upper layer of material is provided (50). A hardmask stack is then formed on the upper layer of material (52). The hardmask stack is comprised of alternating layers of capping material and amorphous carbon including at least a first upper layer of capping material, a layer of amorphous carbon underlying the first upper layer of capping material, and a second layer of capping material underlying the layer of amorphous carbon. A photoresist mask is then formed over the hardmask (54). The

photoresist mask may be trimmed by a photoresist trimming process. The hardmask stack is then etched using the photoresist mask as an initial etch mask to form a hardmask for patterning the underlying upper layer of material (56).

Further processing may also be performed such as patterning the underlying material and removing the hardmask.

While the invention has been described with reference to its preferred embodiments, those skilled in the art will understand and appreciate from the foregoing that variations in equipment, operating conditions and configuration may be made and still fall within the spirit and scope of the present invention which is to be limited only by the claims appended hereto.

CLAIMS

What is claimed is:

1. A method for fabricating a semiconductor device comprising:

providing a substrate comprising an upper layer of material (8);

forming a hardmask stack on the upper layer of material, the hardmask stack comprising an amorphous carbon portion formed in contact with the layer of material (8), and a capping layer (12) formed on the amorphous carbon portion, the amorphous carbon portion comprising alternating layers of doped amorphous carbon (22) containing dopant for enhancing etch selectivity with respect to said upper layer of material, and undoped amorphous carbon (20) containing essentially none of said dopant;

forming a photoresist mask (14) over the hardmask stack; and

etching the hardmask stack using the photoresist mask (14) as an initial etch mask to form a hardmask for patterning said upper layer of material.

2. The method claimed in claim 1, further comprising:

patterning the upper layer of material (8) using the hardmask; and

removing the hardmask by an ashing process.

3. The method claimed in claim 1, wherein forming said photoresist mask comprises:

forming a photoresist pattern on said capping layer; and

trimming said photoresist pattern.

4. A structure formed during fabrication of a semiconductor device, comprising:

a substrate comprising an upper layer of material (8); and

a hardmask stack formed on said upper layer of material, the hardmask stack comprising an amorphous carbon portion formed in contact with said upper layer of material, and a capping layer formed on the amorphous carbon portion, the amorphous carbon portion comprising alternating layers of doped amorphous carbon (22) containing dopant for enhancing etch selectivity with respect to the material, and undoped amorphous carbon (20) containing essentially none of said dopant.

5. The structure claimed in claim 4, wherein the amorphous carbon portion of the hardmask comprises:

a lowermost layer of undoped amorphous carbon (20) formed on said upper layer of material (8);

an uppermost layer of undoped amorphous carbon (20) formed in contact with said capping layer (12); and

at least one layer of doped amorphous carbon (22) between said uppermost (20) and lowermost (20) layers of undoped amorphous carbon.

6. A method for fabricating a semiconductor device comprising:

providing a substrate comprising an upper layer of material (8);

forming a hardmask stack on the upper layer of material (8), the hardmask stack comprising alternating layers of capping material (42) and amorphous carbon (40) including at least an upper capping material layer (42) and a lower capping material layer (42), and at least one amorphous carbon layer (40) formed between the upper and lower capping material layers (42);

forming a photoresist mask (14) over the hardmask stack; and

etching the hardmask stack using the photoresist mask (14) as an initial etch mask to form a hardmask for patterning said upper layer of material (8).

7. The method claimed in claim 6, wherein the hardmask stack further comprises a lower amorphous carbon layer (40) formed on said upper layer of material (8), said lower capping material layer (42) being formed on said lower amorphous carbon layer (40), and

wherein the method further comprises:

patterning the upper layer of material (8) using the hardmask; and

removing the hardmask from the upper layer of material (8) by an ashing process.

8. The method claimed in claim 6, wherein said lower amorphous carbon layer (40) contains dopant for enhancing etch selectivity with respect to said upper layer of material (8).

9. A structure formed during fabrication of a semiconductor device, comprising:

a substrate comprising an upper layer of material (8); and

a hardmask stack formed on said upper layer of material, the hardmask stack comprising alternating layers of capping material (42) and amorphous carbon (40) including at least an upper capping material layer (42) and a lower capping material layer (42), and at least one amorphous carbon layer (40) formed between the upper and lower capping material layers (42).

10. The structure claimed in claim 9, wherein the hardmask further comprises a lower amorphous carbon layer (40) formed on said upper layer of material (8), said lower capping material layer (42) being formed on said lower amorphous carbon layer (40), and

wherein said lower amorphous carbon layer (40) contains dopant for enhancing etch selectivity with respect to said upper layer of material (8).