SPECIFICATION

Semiconductor device

This inventon relates to semiconductor devices and in particular to techniques for reducing leakage currents in such devices.

Leakage currents in semiconductor devices represent a departure from ideal behaviour which in some applications can lead to a serious limitation on performance. One such application is in dynamic random-access memories using insulated-gate field effect transistors.

U.S. Patent, 4,012,757 to Koo disclosed an MOS random access memory. The circuit sturcture of this type of memory is such that leakage currents cause stored charges to decay. These charges represent data stored in capacitive memory locations. Consequently, to retain stored data in the memory locations over an extended period of time, periodic readout and refresh pulses become necessary.

Memories subject to these periodic readout and refresh pulses are referred to as dynamic random access memories or dynamic RAMs. While dynamic RAM device structure is simpler than a static RAM device structure is simpler than a static RAM device structure and therefore more desirable, in making such a dynamic RAM it is also desirable to minimise the decay of the stored charges.

A slower decay time amounts to the possibility of slowing down the frequency of the refresh pulses. A slower decay time also decreases the possibility of losing stored data during the interval betweeen two consecutive refresh pulses. Since there is a relationship between the rate of decay of the stored data and the reverse biased junction-type leakage current in the device, it becomes desirable to reduce this leakage current.

U.S. Patent 3,997,368 to Petroff *et al.* entitled "Elimination of Stacking Faults in Silicon Devices: A Gettering Process" discloses a reduction of p-n junction leakage currents by suppressing the formation of crystal defects near p-n junctions in semiconductive material through a gettering process. The gettering includes the introduction of lattice distortion by forming a stressed layer on the back surface of the wafer. The layer is then annealed for a time and at a temperature effective to cause stacking fault nucleation sites to diffuse to a region near to the back surface of the wafer. The diffusion of the nucleation sites to the vicinity of the back surface suppresses the formation of stacking faults in the device.

Gettering processes similar to those described in U.S. Patent 3,997,368 have been used in the manufacture of typical dynamic memories. For such memories typical hold times have been found to lie in the range of about 6 to 40 milliseconds at an 85°C junction temperature. The term "hold time" refers to the time interval at which refresh pulses can be spaced without losing information from the memory cells.

Of course, for any number of memories tested hold times vary within a range, and the term "typical" with respect to hold time values is here used to mean the median value of a number of devices. It therefore appears desirable to manufacture dynamic memories with typical hold times well above minimum hold time requirements. To obtain an acceptable yield of manufactured memory devices, it is desirable to have substantially all such devices meet the minimum hold time requirements.

In a device as claimed the diffusion component of leakage current is reduced by the nearby presence of a highly doped substrate which reduces the number of minority carriers available to contribute to the diffusion component. If minority carriers generation centres are eliminated to a sufficient extent that the contribution leakage current from minority carrier generation is dominated by the contribution from the diffusion component, then the reduction in the diffusion component achieved by the invention gives rise to a considerable reduction in leakage current. Furthermore, we have found that if the difference in doping level between the substrate and the layer is sufficiently great there is a gettering effect which tends to trap minority carrier generation centres in the substrate, thus helping to reduce the generation component.

The thickness of the epitaxial layer in which the device is formed needs to be small compared with the diffusion length of minority carriers in the layer. Preferably the thickness of the layer is not more than one-tenth of the diffusion length and better still not more than one-thirtieth.

The layered structure is typically prepared so that its minority carriers have an average diffusion length of at least about 500 microns (1 micron equals 10^{-6} metres) which corresponds to an effective lifetime for such minority carriers of about 500 microseconds. Furthermore, the quality of the epitaxial layer with respect to minority carrier generation centres is preferably such that the number of such centres is so small that a diode formed in the epitaxial layer is substantially diffusion current dominated within normal operating temperatures of circuit devices in the body.

It is found that a p-n junction entirely formed in the epitaxial layer will have a very low reverse leakage current. Accordingly, a dynamic random access memory cell formed in the epitaxial layer is provided with a surprisingly long hold time, well worth the extra processing effort involved. Moreover, if p-n junctions of such a cell are confined to a region close to the surface of the layer and entirely within the thickness of the layer, breakdown characteristics and capacitances of such junctions remain substantially those typically corresponding to the moe lightly doped layer than those associated with the dopant concentrations in the substrate portion of the body.

The present invention is particularly useful with respect to MOS dynamic RAMs. It is with respect to this type of semiconductor device that the present invention will be described. However, this does not mean that the invention does not have broader applicability. In general, the invention applies to various semiconductor elements which require the leakage current through reverse biased p-n junctions to remain comparatively low.

Prior art n-channel dynamic RAMs have been made by conventional manufacturing techniques at one surface of a p-type doped silicon wafer. It is known, for instance, that there is a correlation between the lifetime of minority carriers in the semiconductor material and the ultimate hold times of the memory cells being formed at the one surface of the semiconductor wafer. For instance, for a prior art memory circuit structure, minority carrier lifetimes in the bulk silicon material of 10 to 50 microseconds corresponded approximately to typical hold times in the finished memories of two to ten milliseconds. The manufacturing steps for making such prior art memory included gettering steps similar to those disclosed in U.S. Patent No. 3,997,368.

The desired "quality" or crystalline structural integrity to reduce minority carrier generation is one with the lowest level of contaminants or harmful impurities that is obtainable with present manufacturing techniques and equipment. These harmful impurities include, for instance, such elements as iron, nickel, copper, calcium or gold. The harmful impurities for purposes of this invention are those which have an energy level about half-way between the valence and the conduction band of silicon. They consequently provide, by their presence in the crystal lattice, generation centres for minority carriers. Also, they are believed to be a cause in the formation of stacking faults and other crystal defects which are known to increase reverse leakage currents when they occur in the vicinity of p-n junctions.

In the absence of such harmful impurities it appears that the diffusion of minority carriers; e.g. electrons in p-type material, becomes the controlling mechanism by which reverse leakage currents can occur. This environment, namely, a predominantly diffusion current dominated semiconductor structure within the temperature operating range of a device formed therein, is significant in connection with this invention.

Minority carrier diffusion currents are found to be highly temperature dependent and a sharp increase in reverse leakage currents across diode junctions has been looked upon in the past as a high temperature phenomenon. The change in the temperature dependence of the reverse leakage current appears to be the crossover from a generation current dominated to a diffusion current dominated leakage current as the temperature of a device is increased.

When a device is made in accordance with a preferred form of this invention however the reverse bias leakage current of its p-n junctions shows the temperature dependence of the diffusion current mechanism in the high temperature portion of its contemplated operational temperature range. The operational temperatures can range from normal room temperature to in excess of 90°C. When reference is made to the high portion of the temperature range temperatures normally higher than 70°C are meant. A typical high portion of temperatures ranges from 70°C to 90°C. However, in pure crystalline structures the reverse bias leakage current may already be dominated by diffusion currents at temperatures above 40°C. Such a diffusion current dominated structure requires that the harmful impurities be substantially eliminated from the structure in which the device is formed.

A preferred embodiment of the invention is dynamic n-channel random access memory device which is incorporated into a p-type epitaxial layer on a silicon body. The body includes a substrate or bulk portion which is preferably boron-doped (boron is a-type dopant) to a relatively high concentration, preferably 10^{19} atoms of the dopant per cubic centimetre. On the bulk silicon there is formed an epitaxial layer, also of boron-doped silicon. However, in the preferred embodiment, the epitaxial layer is doped only to a concentration of about 2×10^{15} dopant atoms per cubic centimetres. It is in this epitaxial layer that memory cell elements are formed.

We have found that if the described epitaxial device structure is diffusion current dominated junction characteristics such as capacitance and threshold and break-down voltage of the memory cell elements are determined by the doping level in the epitaxial layer. On the other hand, the reverse leakage currents across junctions in the elements are limited by the reduced availability of the minority carriers, i.e. electrons, within one diffusion length from the junction, in the highly doped substrate. A memory in such structure can thus be constructed which has optimum capacitance, threshold and breakdown voltage characteristics, and in addition low reverse leakage characteristics which translate into advantageously long hold times for each of the individual cells in the memory.

Some embodiments of the invention will now be described by way of example with reference to the accompanying drawings of which:–

Figure 1 is a section through a portion of a semiconductor wafer showing an epitaxial layer on a substrate in proportional thickness to the substrate, useful to explain the invention;

Figure 2 is an enlarged sectional view of the epitaxial portion shown in FIG. 1 and depicting various doped regions for forming p-n junctions having low leakage current in accordance with the invention;

Figure 3 is a schematic diagram of the electrical function of the structure of FIG. 2;

Figure 4 is a diagram of preferred boron concentrations in the semiconductor material of the wafer of FIG. 1;

Figure 5 is a sectional view of an alternate and presently preferred structure to which the invention is applicable to obtain favourable reverse leakage current characteristics; and

Figure 6 is a block diagram of a process highlighting steps of forming a semiconductor device in accordance with a preferred embodiment of the invention.

The Semiconductor Body

In FIG. 1 there is shown a portion of a semiconductor wafer which is designated generally by the numeral 11. The wafer 11 is shown in cross section to show the relative thickness between the substrate or bulk portion 12 of the wafer 11 and an

epitaxial layer 14 which is formed at one surface of the wafer. The bulk silicon 12 has a thickness of approximately 500 microns (500×10^{-6} metres).

In comparison to the bulk silicon 12, the thickness of the epitaxial layer is preferably only ten to fifteen microns. FIG. 1 is greatly enlarged in the vertical (thickness) direction to render the epitaxial layer 14 visible.

The starting bulk material 12 of the wafer 11 is a p+ type silicon material with a (100) crystal orientation. The p+ type doping is a boron doping at a level of at least 10^{18} atoms per cubic centimetre. The doping level for the starting material of at least 10^{18} boron atoms per cubic centimetre was found to be a threshold limit to take full advantage of the invention in relationship to the doping of the epitaxial layer 14. When the bulk silicon 12 was doped to at least such a level, the epitaxial layer 14 could be grown with unmeasurably low concentrations of harmful impurities such as iron, nickel, copper, calcium or gold.

On the other hand, when the boron doping level dropped below 10^{18} atoms per cubic centimetres, the epitaxial layer was found to show signs of increasingly higher concentrations of the harmful impurities. The higher concentrations of the harmful impurities resulted in correspondingly shorter effective lifetimes of minority carriers. Consequently, it may be possible in a very clean process with virtually no introduction of any of the harmful impurities into the semiconductor structure to achieve the same high effective lifetime characteristics even with a lower doping level than 10^{18} atoms per cubic centimetre in the substrate.

In a preferred embodiment, the boron concentration in the bulk silicon 12 is consequently about 10^{19} atoms per cubic centimetre. It is believed that at this doping level in the process described, the bulk silicon acts as a barrier to, or a trap for, the harmful impurities diffusing through the wafer 11.

The highly doped bulk silicon appears to exhibit an increased capacity to trap any of the harmful impurities. An explanation for such an increased capacity to trap impurities is not proven. However, some theories are offered which may give some insight.

One mechanism of such a barrier may be the result of possible ionic bonds between the harmful impurities and other atoms in the doped crystalline semiconductor structure. Such bonds are believed to account at least in part for the retention of the harmful impurities within the bulk silicon 12 as they diffuse throughout the structure. However, such ionic bonding by which the impurities tend to be retained within the highly doped structure of the bulk silicon may be only one of several mechanisms to result in gettering of harmful impurities.

Another mechanism is believed to involve lattice strain which has been detected at the interface between the bulk silicon 12 and the epitaxial layer 14. The strain is the result of the different doping levels in the bulk silicon 12 and the epitaxial layer 14. The different doping levels establish differences in the lattice spacing of the bulk silicon 12 and of the epitaxial layer 14 which result in lattice strain misfit dislocations. These misfit dislocations are believed to contribute to the trapping or gettering of the harmful impurities from the epitaxial layer 14.

Gettering as a result of misfit dislocations introduced on one surface of a wafer is known. U.S. Patent 3,997,368 to Petroff et al. discloses such a means for gettering impurities. However, in the wafer structure according to the present invention, the plane of the misfit dislocations is located at the interface between the bulk silicon 12 and the epitaxial layer 14. The proximity of the misfit dislocations to the active p-n junctions in the epitaxial layer 14 is believed to enhance their effectiveness in gettering through out all heated processing steps. This enhancement is believed to exist in comparison to the back surface gettering process disclosed in patent 3,997,368. It should be understood, however, that the invention is not predicated on any of the mechanisms or theories discussed herein. These theories are merely offered as possible explanations to the results.

With such an observed increased capacity to retain the harmful impurities in the bulk silicon once they enter the wafer, and with various precautions to prevent the harmful impurities from diffusing into the wafer 11 during the process of making the semiconductor devices, the epitaxial layer 14 becomes relatively free of such impurities. Consequently, the layered structure or wafer 11 exhibits relatively long minority carrier lifetime characteristics.

The epitaxial layer is grown to have a doping level of about 2×10^{15} boron atoms per cubic centimetre. This doping level determines, for instance, the capacitance of any junctions in the material.

Typically, at the interface between the epitaxial layer and the original substrate there will be a region of graded concentration resulting from the out-diffusion of boron from the substrate into the epitaxial layer during growth of the epitaxial layer. However, in an epitaxial layer of a thickness about 10–15 microns, as it is typical of the preferred embodiment, this effect is negligible.

The formed layered structure of the described bulk silicon substrate and the epitaxial layer typically is found to have an electron lifetime of at least 500 microseconds. Such a value corresponds to a diffusion length for the minority carriers, namely, the electrons, of about 500 microns. The thickness of the epitaxial layer 14 is consequently no more than one-thirtieth of the diffusion length of the electrons. It can, accordingly, be appreciated that within the volume where free electrons can be expected to diffuse across a rectifying junction as the effective leakage current of such junction, the material is largely the heavily doped material of the substrate. In this heavily doped bulk silicon the density of conduction electrons is low compared with the lightly doped epitaxial layer where the conduction electron density, being inversely proportional to the doping level, is greater. Thus, in a defect free epitaxial alyer, the measured generation lifetimes reflect the diffusion current limited attributes of the structure. However, at the same time, the junction is embedded in a finite thickness of the lightly doped mater-

ial. It is this lightly doped material that determines good breakdown characteristics and low capacitance of MOS elements in the layer.

The Device Structure

Referring now to FIG. 2, there is shown on an enlarged scale a portion of the epitaxial layer 14 with a portion of the adjacent bulk silicon 12. Into the epitaxial layer 14, regions of opposite conductivity (donor) impurities such as phosphorus or arsenic atoms are imbedded to a relatively shallow depth (approx. 0.5 to 2 microns).

The selective predominance of the n-type impurities forms n-type regions 22, 23 and 24 at the surface of the epitaxial layer 14 and results in p-n junctions 25, 26 and 27, respectively. Selectively patterned oxide layers and additional conductive patterns deposited over oxide dielectric layers form active MOS devices of the n-channel dynamic RAM described herein. In particular, there are shown transistors 28 and 29 (FIG. 3). These devices and their interconnecting structures can be formed in accordance with known processing steps. It is important to notice, however, that noe of the active MOS structures including the p-n junctions extend beyond regions close to the upper surface of the epitaxial silicon layer. The entire device structure of each memory cell is located near the upper surface of the epitaxial layer 14.

In fact, an optimum thickness for the epitaxial layer 14 is one which exceeds only slightly the depth of the p-n junction from the upper surface of the layer added to the expected depth of the depletion region about the junction. The determination of the depth of the depletion region is well known in the art. It depends, of course, on the doping of the semiconductor material, e.g., that of the epitaxial layer 14, and the maximum reverse bias voltage to be applied to the junction. Such a thickness of the layer 14 still permits the junction to possess the characteristics of the lightly doped layer 14, while it maximises at the same time the influence of the bulk silicon with its greatly reduced number of free electrons.

The transistors 28 and 29 belong to two adjacent memory cells which are designated generally by the numerals 30 and 31 in FIG. 3. Another element of each of the cells 30 and 31 is a capacitor, 32 and 33 respectively.

A plate 34 of the capacitor 32 is part of the epitaxial layer 14. Similarly, a plate 35 of the capacitor 33 is the epitaxial silicon adjacent the region 24. Facing plates 36 and 37 of the respectively capacitors 32 and 33 are spaced from the epitaxial layer 14 by thin silicon oxide films 38 and 39.

The plates 36 and 37 are preferably formed of polycrystalline silicon with connecting extensions 41 and 42 to a common constant voltage plane. Gates 43 and 44 of the transistors 26 and 27 are also formed of polycrystalline silicon. The gates 43 and 44 are also, like the plates 36 and 37, separated from the epitaxial silicon by thin films 46 and 47 of silicon oxide.

The thickness of the thin films 38, 39, 46 and 47 are chosen to lie in a range from about 200 Angstrom units to 2000 Angstrom units. Typically, about 900 Angstrom units is presently preferred. The thicknesses of such thin films of oxide are consequently only about one-tenth of the thickness of thicker field oxide layers 48, which are preferred to lie in the range of 1 micron. The junction depths of the n-type diffusions are in comparison also about 0.8 microns below the upper surface of the epitaxial layer 14.

The gates 43 and 44 integrally form word select lines which extend perpendicular to the section of FIG. 2. The extensions 41 and 42 continue to lead away from the memory cells 30 and 31 separated from the epitaxial layer 14 by the field oxide layers 48.

A second level metallisation pattern 49, preferably of aluminium, is separated from the gates and capacitor plates by an interlevel dielectric layer 50. Selective openings 51 in the layer 50 permit the pattern 49 to contact the region 23. As can be seen in FIG. 2, through each opening two memory cells (30 and 31 of FIG. 3) are contacted. Conductors of the pattern 49 form bit sense lines of the memory device. The upper surface of the cells 30 and 31 is passivated by a top dielectric layer 52.

FIG. 4 shows a typical concentration profile in the epitaxial layer 14, the bulk silicon 12 and in the interfacing region between the epitaxial layer and the bulk silicon. As the epitaxial layer 14 is grown on the top of highly doped silicon, some outdiffusion of boron dopants from the bulk silicon into the epitaxial layer is encountered. However, the rate of growth of the epitaxial layer exceeds that of the outdiffusion of boron from the bulk silicon. Consequently, the boron concentration in the epitaxial layer quickly settles to the desired value of approximately 2×10^{15} atoms per cubic centimetre of boron. Comparing the dopant concentration profile with an overlay portion of the wafer 11, including one of the highly doped n-type regions for reference, it is seen that the active regions and p-n junctions are formed entirely within silicon having a uniform dopant concentration.

FIG. 5 refers to an alternate memory to which the invention preferably applies. The previously referred-to-patent 4,012,757 to Koo discloses, for instance, a merged drain and capacitor region. FIG. 5 also discloses an embodiment of a memory with a merged drain and capacitor region (34 and 35). Such an embodiment tends to save space in the layout of the memory cells (30 and 31). It appears that larger memories, e.g., 16,384 bits compared to 4,096 bits, are particularly advantageously affected by the present invention, when the physical design of the cells with reduced storage capacitance, for instance, results in reduced holdtimes. The embodiment in FIG. 5 represents such a memory. Numerals pointing out similar functional elements have been kept the same as in FIGS. 2 and 3.

However, the section of FIG. 5 through the two memory cells 30 and 31 differs from the section in FIG. 2 because of an offset layout of the adjacent cells 30 and 31. Also, the region 23, an arsenic implant, is extended perpendicular to the plane of the section to function as the bit select line 49. The gates 43 and 44 are formed of polycrystalline sili-

con, but their common extension of a word select line 55 is now formed of aluminium. The contact of the word select line 55 with the gate 44 is not shown since it exists in an offest position from the plane of the section. The respective capacitor plates 36 and 37 extend perpendicularly to the section by the extensions 41 and 42 to the common constant voltage source. Interlevel dielectric layers 56 and 57 separate the capacitor plates 36 and 37 from the adjacent gate conductors 43 and 44, respectively.

The mode of operation of memory structures similar to the ones disclosed herein is well known in the art. The increase in the holdtimes of the cells appears as distinct departure when the described memory structure can operate in a diffusion current controlled structure. In this mode leakage currents become inversely proportional to the concentration of the dopants in the semiconductor to the concentration of the dopants in the semiconductor material in which the junctions of interest are located.

Eliminating Harmful Impurities

It has been found that the capacity of the highly doped bulk silicon 12 to trap the harmful impurities, while improved over less highly doped material is, nevertheless, limited.

It is, therefore, desirable to minimise *ab initio* the level of the harmful impurities which enter the silicon wafer 11. During the process of growing the epitaxial layer 14, the harmful impurities enter the system through contaminated gases. However, the level of the harmful impurities entering from contacting gases is low. Generally, the contacting gases are sufficiently pure that they can mostly be disregarded as a substantial source of contaminants or harmful impurities.

However, a more significant possible source of harmful impurities has been discovered. It has been found that while the wafers 11 are being heated for the deposition of the epitaxial layer 14 impurities may readily migrate from a susceptor 63 (FIG. 1) through an interface 64 between the wafer 11 and the susceptor 63. It becomes, therefore, desirable to eliminate the in-diffusion of the harmful impurities from the susceptor 64. It has, for instance, been found that some type of susceptors are more apt to contain the harmful impurities than others.

Susceptors which have been found to be particularly advantageous are made of pyrolytic graphite. Impurity levels in pyrolytic graphite susceptors were sufficiently low to permit their use to result in typical lifetimes in the layered structure of more than 500 microseconds.

The transfer of the harmful impurities from the susceptor 63 to the wafers 11 is furthered by direct contact between the wafers 11 and the susceptor 63 during the growing of the epitaxial layer 14 on each of the wafers 11.

Prior to growing the epitaxial layer 14 with the desired boron concentration of 2×10^{15} atoms per cubic centimetre auto-doping advantageously should be limited. Auto-doping is a phenomenon by which the epitaxial layer 14 accepts dopants from the bulk silicon through the gaseous environment of the wafers 11. The boron elements out-diffuse from the bulk silicon into the gaseous atmosphere of the reactor and then redeposit in the crystalline structure of the epitaxial layer 14 of each of the wafers.

To control outdiffusion of boron dopants from the bulk silicon 12, a layer 66 of highly pure polycrystalline silicon advantageously is deposited on the surface of the susceptor 63 to a thickness of approximately two to three microns. The wafers 11 are then supported on the surface of the coated susceptor 63.

In reference to FIG. 6, the wafers 11 are then heated to a temperature of approximately 1100°C in a hydrogen atmosphere. At this temperature boron tends to evaporate from the wafer surface and hydrochloric acid is injected in gaseous form for a time interval of five minutes during which approximately 0.5 micron of the silicon materialis etched from its surface. The etching velocity proceeds much more rapidly than the evaporation of boron atoms from the silicon. The "in-situ" etching step is done for perfection. Our experience has been that without the etching step, a great number of defects occur in the epitaxial layer.

While the wafers remain on the susceptor in the reactor the temperature is lowered slightly to approximately 1040°C during a time span of approximately one to two minutes. After that time a dichlorosilane process of growing the epitaxial layer 14 is started. The main carrier gas is hydrogen with dopant gases introduced in very low quantities. It is desirable to adjust the quantities to achieve precise doping levels in the epitaxial layers. Even under ideal conditions outdiffusion from the highly doped bulk silicon 12 has some effect on the dopant level of the epitaxial layer.

Further processing steps pertain to the forming of the MOS memory cells 30 and 31 in the epitaxial layer 14. In the epitaxial layer 14, the regions 22, 23 and 24 of opposite conductivity type are formed either by diffusion or by ion implantation techniques. Selectivity in exposing designated areas of the surface of the epitaxial layer 14 to dopants of the opposite conductivity type is achieved by selective oxide masking in accordance with known techniques. Further steps include thin oxide forming and deposition and definition of the polycrystalline silicon. Interlevel dielectric layers are formed, followed by aluminium deposition for the bit sense lines. These processing steps can be executed in accordance with techniques well known in the art.

During these processing steps, harmful impurities may be introduced at various levels either through rinsing waters or through handling into the top surface of the wafer 11. A final open window phosphorus gettering step is therefore done prior to forming metallisation patterns. However, continuous gettering of harmful impurities by the heavily doped bulk silicon 14 is believed to take place through the various device forming steps to minimise crystalline defects in the active areas of the epitaxial layer 14 as the devices are being formed at its surface.

In the completion of MOS memories in accordance with the present invention, the exclusion of

sources of harmful impurities during the various processing steps is of continuous concern. It must, however, be recognised that in a substantially clean environment active exclusion of such impurities becomes of lesser concern. This is particularly true in view of the impurity trapping mechanism established.

CLAIMS

1. A semiconductor device formed in a surface region of an epitaxial layer of doped semiconductor material, the epitaxial layer being substantially free from impurities constituting minority carrier generation centres, having a thickness which is small compared with the diffusion length of minority carriers in the layer and being on a substrate of the same conductivity type as but heavily doped compared with the layer.

2. A semiconductor device formed in a surface region of an epitaxial layer of doped semiconductor material, the epitaxial layer having a thickness which is small compared with the diffusion length of minority carriers in the layer and being on a substrate of the same condductivity type as but heavily doped compared with the layer, and wherein leakage current in the device has the temperature dependence associated with diffusion of minority carriers in a temperature range extending down to below 90°C.

3. A device as claimed in claim 2 wherein the said temperature range includes the range 70 to 90°C.

4. A device as claimed in claim 3 wherein the said temperature range extends down to 50°C or below.

5. A device as claimed in any of the preceding claims wherein the layer and the substrate are of silicon.

6. A device as claimed in any of the preceding claims wherein the conductivity of the layer and substrate is p-type.

7. A device as claimed in any of the preceding claims, wherein the thickness of the layer is not more than one-tenth of the diffusion length of minority carriers in the layer.

8. A device as claimed in claim 4, wherein the thickness of the layer is not more than one-thirtieth of the diffusion length of minority carriers in the layer.

9. A device as claimed in any of the preceding claims, wherein the diffusion length of minority carriers in the layer is at least about 500 microns.

10. A device as claimed in any of the preceding claims wherein the epitaxial layer is sufficiently thick so that depletion or inversion regions formed when the device is in normal use do not extend to the substrate.

11. A device as claimed in claim 10 wherein the epitaxial layer is not substantially thicker than is required by claim 10.

12. A device as claimed in any of the preceding claims wherein the dopant concentration in the substrate is at least one hundred times the dopant concentration in the layer.

13. A device as claimed in any of the preceding claims, wherein the dopant concentration in the substrate is at least 10^{18} atoms per cubic centimetre.

14. A device as claimed in any of the preceding claims, including at least one insulated-gate field-effect transistor.

15. A device as claimed in any of the preceding claims, including at least one capacitative element comprising a conductive element insulatedly overlying a portion of the layer.

16. A device as claimed in claim 15, wherein the said portion of the layer constitutes the drain region of an insulated-gate field-effect transistor.

17. A device as claimed in any of the preceding claims, constituting a dynamic random-access memory.

18. A device substantially as herein described with reference to Figs. 1 to 4 or Fig. 1 and Figs. 3 to 5 of the accompanying drawing.

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