(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 June 2005 (02.06.2005)

PCT

(10) International Publication Number
WO 2005/050740 A3

(51) International Patent Classification[7]: H01L 29/792

(21) International Application Number:
PCT/US2004/038261

(22) International Filing Date:
16 November 2004 (16.11.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/714,753 17 November 2003 (17.11.2003) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

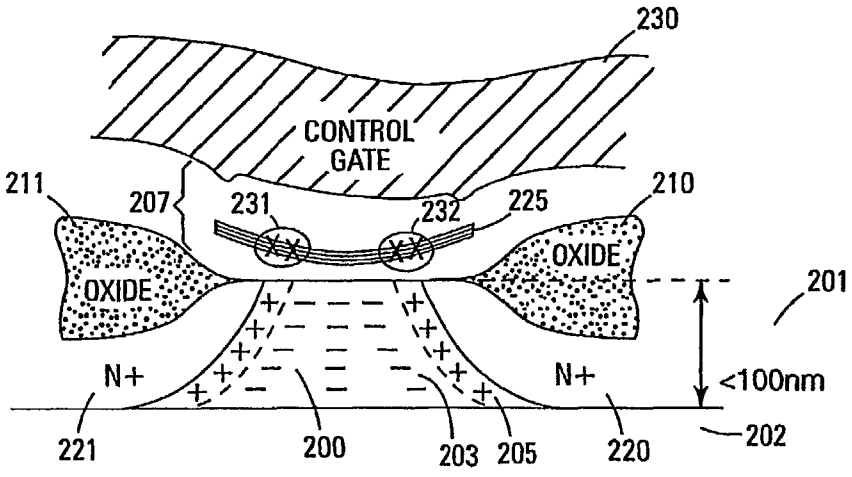
Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) Title: NROM FLASH MEMORY DEVICES ON ULTRATHIN SILICON



(57) Abstract: An NROM flash memory cell is implemented in an ultra-thin silicon-on-insulator structure. In a planar device, the channel (200) between the source/drain (220, 221) areas is normally fully depleted. An oxide layer (210, 211) provides an insulation layer between the source/drain areas and the gate insulator layer (207) on top. A control gate (230) is formed on top of the gate insulator layer. In a vertical device, an oxide pillar (310) extends from the substrate with a source/drain area (330, 331) on either side of the pillar side. Epitaxidal regrowth is used to form ultra-thin silicon body regions (300, 301) along the sidewalk of the oxide pillar. Second source/drain areas (320, 321) are formed on top of this structure. The gate insulator (307) and control gate (330) are formed on top.

WO 2005/050740 A3

(88) Date of publication of the international search report:
6 October 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.