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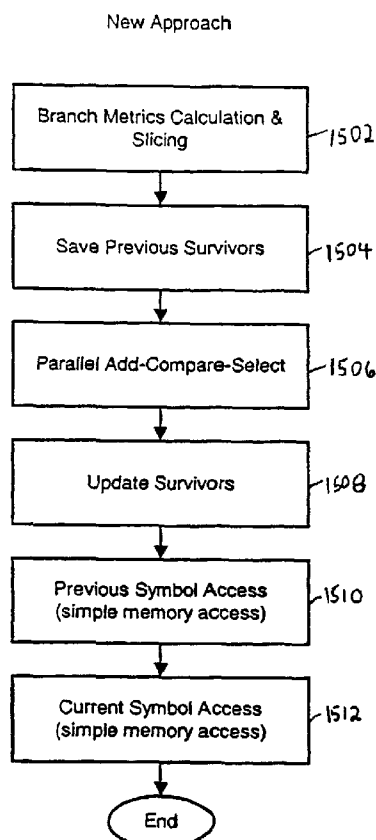
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(54) Title: METHOD AND APPARATUS FOR CONSTELLATION DECODER



(57) Abstract: A method and apparatus for performing a slicer and Viterbi decoding operations which are optimized for single-instruction/multiple-data type of parallel processor architectures. Some non-regular operations are eliminated and replaced with very regular repeatable tasks that can be efficiently parallelized. A first aspect of the invention provides a pre-slicer scheme where once eight input symbols for a Viterbi decoder are ascertained and their distances calculated, these distances are saved in an array. A second aspect of the invention provides a novel way of performing the path and branch metric calculations in parallel to minimize processor cycles. A third aspect of the invention provides a method to implement the Viterbi decoder without continually performing a trace back. Instead, the previous states along the maximum likelihood paths for each trellis state are stored. When the path with the shortest distance is later selected, determining the trace back state merely requires a memory access.



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