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(71) Applicant (for all designated States except US): **TELEFONAKTIEBOLAGET L M ERICSSON (PUBL)**
[SE/SE]; S-164 83 Stockholm (SE).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **CHENG, Jung-Fu**
[—/US]; 109 Bradwyck Drive, Cary, NC 27513 (US).

(74) Agent: **WEATHERFORD, Sidney, L.**; Ericsson Inc.,
6300 Legacy, MS EVR 1-C-11, Plano, TX 75024 (US).

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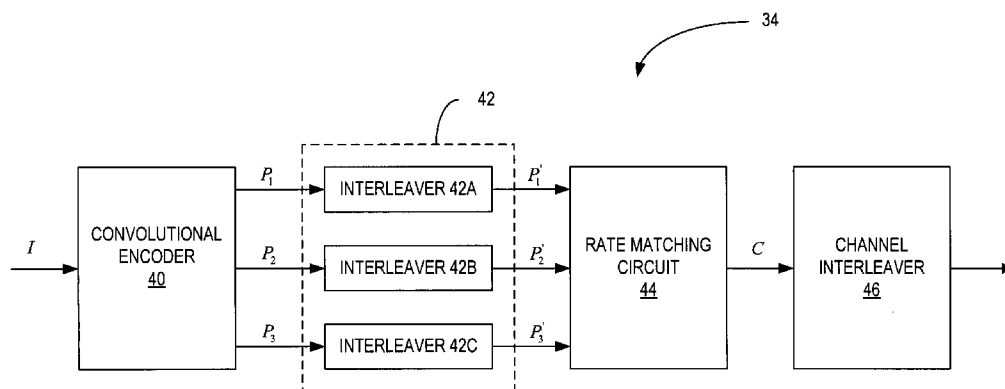


FIG. 2

(57) Abstract: An error coding circuit comprises a non-systematic convolutional encoder for coding an input bit stream to produce two or more groups of parity bits, an interleaver circuit for interleaving parity bits within each group of parity bits, and a rate-matching circuit for outputting a selected number of the interleaved parity bits ordered by group to obtain a desired code rate.