

~~[0117] What Is Claimed Is:~~

1. A semiconductor device comprising:

a well region;

a drain region and a source region disposed in the well
5 region;

a gate electrode disposed above the well region;

a thin gate insulating layer and a thick gate
insulating layer disposed under the gate electrode, the thick
gate insulating layer being disclosed closer to the drain region
10 than the thin gate insulating layer; and

an extended drain junction region disposed below the gate
electrode.

2. The semiconductor device according to claim 1,
15 wherein the well region is a first conductivity region, the
drain region and the source region are second conductivity
regions, and the extended drain junction region is a second
conductivity region.

20 3. The semiconductor device according to claim 1,
wherein the extended drain junction region extends laterally
to a portion of the well region from the drain region.

4. The semiconductor device according to claim 1,
25 ~~wherein a length of the extended drain junction region~~

~~overlapping with the gate electrode is greater than a length~~
of the gate electrode overlapping with the thick gate insulating
layer.

5 5. The semiconductor device according to claim 4,
wherein a difference between the length of the gate electrode
overlapping with the thick gate insulating layer and the length
of the extended drain junction region overlapping with the gate
electrode is equal to or less than 0.1 μm .

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6. The semiconductor device according to claim 1,
wherein an upper surface of a semiconductor region between the
gate insulating layer and the drain region is coplanar.

15 7. The semiconductor device according to claim 1,
wherein the extended drain junction region has a depth of 500
 $\text{\AA}$ to 3500 $\text{\AA}$.

8. The semiconductor device according to claim 1,
20 further comprising an isolation layer having a depth deeper than
the extended drain junction region.

9. The semiconductor device according to claim 3,
wherein the extended drain junction region extends to a portion
25 ~~of the well region under the thin gate insulating layer.~~

~~10. The semiconductor device according to claim 1,~~
wherein the drain region is formed in the extended drain
junction region and is isolated from the source region by the
5 well region.

11. The semiconductor device according to claim 3,
wherein the extended drain junction region extends to only a
portion of the well region under the thick gate insulating
10 layer.

12. The semiconductor device according to claim 1,
wherein a length of the gate electrode overlapping with the
thick gate insulating layer is shorter than a length of the
15 extended drain junction region overlapping with the gate
electrode.

13. The semiconductor device according to claim 1,
further comprising a second conductive type medium well region
20 between the extended drain junction region and the drain region.

14. The semiconductor device according to claim 1,
wherein the extended drain junction region contacts the well
region.

~~15. A method for manufacturing a semiconductor device~~
comprising:

forming an extended drain junction region in a well region
of a substrate;

5 forming two or more gate insulating layers having
different thicknesses on the well region; and

forming a gate electrode on the gate insulating layers,
wherein the extended drain junction region overlaps with
the gate electrode.

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16. The method for manufacturing a semiconductor device
according to claim 15, further comprising:

forming the well region in the substrate prior to forming
the extended drain junction region; and

15 forming a source region and a drain region on both sides
of the gate electrode.

17. The method for manufacturing a semiconductor device
according to claim 15, wherein the gate insulating layers
20 comprise a first gate insulating layer and a second gate
insulating layer, and the first gate insulating layer has a
thickness thinner than the second gate insulating layer.

18. The method for manufacturing a semiconductor device
~~25 according to claim 16, wherein the first gate insulating layer~~

~~is formed closer to the source region than the second gate insulating layer.~~

19. The method for manufacturing a semiconductor device
5 according to claim 15, wherein the extended drain junction region is formed through ion implantation for logic well voltage adjustment.

20. The method for manufacturing a semiconductor device
10 according to claim 15, wherein the extended drain junction region has a dopant concentration of approximately $1\text{E}17$ atoms/cm³ to $1\text{E}19$ atoms/cm³.

21. The method for manufacturing a semiconductor device
15 according to claim 17, wherein the extended drain junction region is formed to extend from the drain region to a portion under the first gate insulating layer.

22. The method for manufacturing a semiconductor device
20 according to claim 17, wherein the first gate insulating layer
~~has a thickness of 5 Å to 50 Å.~~

What is claimed is:

1. A semiconductor device comprising:

a substrate;

a well region of a first conductivity type disposed in the substrate;

an extended drain junction region disposed in the well region of a first conductivity type;

a source region disposed in the well region;

a drain region disposed in the extended drain junction region;

a shallow trench isolation region disposed adjacent to the drain region; and

a stepped gate oxide layer disposed on the extended drain junction region comprising a thin gate insulating layer and a thick gate insulating layer, the thick gate insulating layer being disposed closer to the drain region than the thin gate insulating layer;

a gate electrode disposed above the stepped gate oxide layer;

wherein the gate electrode is positioned to overlap an entire length of the thick gate insulating layer that overlaps the extended drain junction region,

wherein the extended drain junction region overlaps with a portion of the thick gate insulating layer and a portion of the thin gate insulating layer,

wherein the extended drain junction region extends laterally to a portion of the well region from the drain region, and

wherein the well region of the first conductivity type is disposed to have a depth deeper than a depth of the shallow trench isolation region.

2. The semiconductor device according to claim 1, wherein the drain region and the source region are second conductivity regions, and the extended drain junction region is a second conductivity region.

3. The semiconductor device according to claim 1, wherein a length of the extended drain junction region overlapping with the gate electrode is greater than a length of the gate electrode overlapping with the thick gate insulating layer.

4. The semiconductor device according to claim 3, wherein a difference between the length of the gate electrode overlapping with the thick gate insulating layer and the length of the extended drain junction region overlapping with the gate electrode is equal to or less than 0.1 μm .

5. The semiconductor device according to claim 1, wherein the extended drain junction region has a depth of 500 Å to 3500 Å.

6. The semiconductor device according to claim 1, wherein the shallow trench isolation region has a depth deeper than the extended drain junction region.

7. The semiconductor device according to claim 1, wherein the extended drain junction region extends to a portion of the well region under the thin gate insulating layer.

8. The semiconductor device according to claim 1, wherein the drain region is formed in the extended drain

junction region and is isolated from the source region by the well region.

9. The semiconductor device according to claim 1, further comprising a second conductive type medium well region between the extended drain junction region and the drain region.

10. The semiconductor device according to claim 1, wherein the extended drain junction region contacts the well region.

11. The semiconductor device according to claim 1, wherein the thick gate insulating layer is not a LOCOS oxide layer.

12. The semiconductor device according to claim 1, wherein an upper surface of a semiconductor region between the gate insulating layer and the drain region is coplanar.

13. The semiconductor device according to claim 1, wherein a sidewall of the gate electrode facing the drain region is aligned with a sidewall of the thick gate insulating layer.

14. The semiconductor device according to claim 1, wherein the well region of the first conductivity type surrounds the extended drain region and the drain region.

15. The semiconductor device according to claim 1, further comprising a deep well region of a second conductivity type disposed in the substrate, and wherein

the well region of the first conductivity type and the extended drain region is disposed in the deep well region.

16. The semiconductor device according to claim 1, further comprising a second shallow trench isolation region disposed adjacent to the source region, wherein the depth of the well region of the first conductivity type is deeper than a depth of the second shallow trench isolation region.

17. A semiconductor device comprising:

- a substrate;

- a deep well region of a first conductivity type disposed in the substrate;

- a well region of the first conductivity type disposed in the deep well region;

- an extended drain junction region disposed in the deep well region;

- a source region disposed in the well region;

- a drain region disposed in the extended drain junction region;

- a stepped gate oxide layer disposed on the extended drain junction region comprising a thin gate insulating layer and a thick gate insulating layer, the thick gate insulating layer being disposed closer to the drain region than the thin gate insulating layer, a lower surface of the thin gate insulating layer being coplanar to a lower surface of the thick gate insulating layer; and

- a gate electrode disposed above the stepped gate oxide layer,

wherein the gate electrode overlaps a portion of the thick gate insulating layer nearer to the drain region than to the source region, and

wherein the extended drain junction region overlaps with a portion of the thin gate insulating layer.

18. The semiconductor device according to claim 17, further comprising a shallow trench isolation region disposed adjacent to the drain region, wherein the deep well region of the first conductivity type has a depth deeper than a depth of the shallow trench isolation region.

19. The semiconductor device according to claim 18, further comprising a second shallow trench isolation region disposed adjacent to the source region, wherein the depth of the deep well region of the first conductivity type is deeper than a depth of the second shallow trench isolation region.

20. The semiconductor device according to claim 17, further comprising a shallow trench isolation region disposed adjacent to the drain region, wherein the well region of the first conductivity type has a depth deeper than a depth of the shallow trench isolation region.

21. The semiconductor device according to claim 17, further comprising a deep well contact region of the first conductivity type disposed in the deep well region.

22. The semiconductor device according to claim 17, wherein the well region of the first conductivity type

surrounds the source region and does not extend to the thick gate insulating layer.

23. The semiconductor device according to claim 17, wherein the well region of the first conductivity type interfaces with the extended drain region under the thin gate insulating layer.

24. The semiconductor device according to claim 23, wherein the well region of the first conductivity type does not interface with the extended drain region under the thick gate insulating layer.

25. A semiconductor device comprising:

- a substrate;

- a well region of a first conductivity type disposed in the substrate;

- an extended drain junction region disposed in the well region of a first conductivity type;

- a source region disposed in the well region;

- a drain region disposed in the extended drain junction region;

- a stepped gate oxide layer disposed on the extended drain junction region comprising a thin gate insulating layer and a thick gate insulating layer, the thick gate insulating layer being disposed closer to the drain region than the thin gate insulating layer, and a lower surface of the thin gate insulating layer being coplanar to a lower surface of the thick gate insulating layer;

- a gate electrode disposed above the stepped gate oxide layer and disposed continuously above at least half of a length of the thick gate insulating layer; and

wherein the extended drain junction region overlaps with a portion of the thin gate insulating layer,

wherein a length of the extended drain junction region overlapping with the thick gate insulating layer is greater than a length of the extended drain junction region overlapping with the thin gate insulating layer.