

PATENT SPECIFICATION

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COMPLETE SPECIFICATION

Driver-Sense Circuit Arrangement in Memory Systems

We, RADIO CORPORATION OF AMERICA, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a memory system having active storage elements, particularly to a circuit arrangement for selectively writing information into a storage element and for selectively sensing the output of that element via a common input-output line. The inventive circuit arrangement further may be operative for sensing information stored in such an element non-destructively.

It has been suggested that a high speed memory for a data processing system take the form of a plurality, e.g. an array, of active memory elements. It has been suggested further that the memory elements be flip-flops employing field-effect transistors, and that the entire memory array be fabricated as an integrated structure in order to provide a large quantity of storage in a small area and to reduce line delays so as to achieve high speed operation.

The capacitance on the output line of an integrated memory may be quite high, especially when the active memory elements employ insulated-gate field-effect transistors. Higher speed operation obtains when current sensing is employed, as opposed to voltage sensing, since it is then unnecessary to charge or discharge the capacitance through a high impedance.

Accordingly, it is an object of this invention to provide a circuit arrangement for both writing information into a memory element and sensing the output of that element on a

common input-sense line, in which current sensing is employed.

According to the invention we provide a memory system comprising; an active storage element having an output point; an input-sense line; means including a coincidence gate selectively operative during a reading operation for connecting a source of first potential to the input-sense line, or not, in accordance with the condition of the storage element and a current sensing circuit having a device coupled to and which presents low impedance to the input-sense line, the device being operative during a reading operation for sensing current flowing from the first potential source through the gate and the input sense line and for maintaining the input-sense line at a substantially constant second potential which is different from the first potential.

In the accompanying drawing, like reference characters denote like components, and:

FIGURE 1 is a block diagram of a memory system;

FIGURE 2 is a schematic diagram of one of the memory cells and a driver-sense circuit for that cell and others of the same column; and

FIGURE 3 is a schematic diagram of another type of memory cell.

In the system of FIGURE 1, a memory 10 comprises a plurality of memory elements 12, only a few of which are shown. These memory elements may be arranged in a rectangular array of rows and columns. For purposes of example, it is assumed that the memory is word organized, wherein each row of memory elements stores a different word of information, and wherein the memory elements in the same column store the digits of like place or significance in the respective words. Each row of elements has a pair of row conductors, one for receiving WRITE

command levels and the other for receiving READ command levels. All of the WRITE lines $W_1, W_2 \dots W_x$ are connected at their input ends to a decoder 16, which receives input signals from a source (not shown) and energizes a selected one only of the WRITE lines during a WRITE operation. The READ lines $R_1, R_2 \dots R_x$ are connected to a decoder 18 which, in response to received input signals, energizes a selected one only of the READ lines during a READ operation. Although separate decoders 16 and 18 are illustrated, a single decoder could be employed with suitable output logic to drive the WRITE and READ lines of the memory.

Signals representing a word to be written into a row of the memory are supplied from a data input source 20 by way of DIGIT lines $D_1 \dots D_n$, there being a separate DIGIT line for each column of memory elements. The data stored in the input device 20 is written into a given row of memory elements 12 when the WRITE line for that row is energized.

In order to reduce or minimize the number of row and column lines in the memory, it is desirable to use the DIGIT lines $D_1 \dots D_n$ for both writing information into the memory and for reading out (sensing) information stored in the memory. As will be described, the information stored in a row of the memory may be read out selectively and non-destructively on the DIGIT lines when the READ control line for that row is energized. Circuitry for both driving the DIGIT lines and for output sensing are contained within the boxes $22_1 \dots 22_n$, and will be described.

All of the memory elements 12 in memory 10 are structurally the same and may take the form of an insulated-gate field-effect transistor flip-flop. The flip-flop for the memory cell at the intersection of row X and column 1 is illustrated within the dashed box 30 of FIGURE 2, and the driver-sense circuit 22_1 for the associated column of flip-flops is shown at the bottom of FIGURE 2.

This flip-flop is known in the art and, consequently, will only be described briefly here. The flip-flop includes a first circuit branch comprising an N-type insulated-gate field-effect transistor 32 and a P-type transistor 34 having their conduction paths, e.g. source-drain paths, connected in series between circuit ground and the positive terminal of a source 36 of V_1 volts, the negative terminal of source 36 being grounded. A second circuit branch comprises an N-type transistor 40 and a P-type transistor 42 having their conduction paths connected in series between circuit ground and the voltage source 36.

Feedback from the output of the first circuit branch to the input of the second branch is provided by a direct connection from output junction 44 to the gate electrodes of trans-

sistors 40 and 42. Feedback from the output of the second branch to the input of the first branch is by way of the conduction path of a normally "on" P-type transistor 50, which is connected between output junction 46 and the gate electrodes of transistors 32 and 34. Information is written into the flip-flop via the source-drain conduction path of an N-type transistor 56, one electrode of which is connected directly to the DIGIT line D_1 . The gate electrodes of transistors 50 and 56 are connected to WRITE line X. In ordinary operation, the voltage on WRITE line X is held at ground potential by the output of a signal source 54, which may be one section of the decoder 16 of FIGURE 1. Thus, in the steady state, transistor 50 is biased on to complete the feedback path for the flip-flop, and transistor 56 is biased off, effectively decoupling the input of the flip-flop from the DIGIT line D_1 .

In one steady state of the flip-flop, transistors 32 and 42 are biased on and transistors 40 and 34 are biased off. This may be considered the "set" state in which the flip-flop stores a binary "1" bit. The conducting states are reversed when the flip-flop is reset, i.e. storing a binary "0" bit. That one of a transistor's electrodes to which an arrowhead is fixed is the "source" electrode. Transistors 50 and 56 have arrowheads affixed to two electrodes, since these devices operate bi-directionally, one electrode functioning as source when current flows in one direction through the conduction both and the other electrode functioning as source when current flows in the opposite direction.

In order to provide isolation for data input and read output on a common DIGIT line, a coincidence gate means 66 is provided at one output of the flip-flop. In general, this coincidence gate means is one which has a conduction path connected between the positive terminal of source 36 and the common digit-sense line D_1 . The gate 66 is illustrated as comprising a pair of n-type insulated-gate field-effect transistors 68, 70 having their conduction paths connected in series. Gate electrode 72 of transistor 68 is connected directly at the output terminal 46 of the flip-flop, and gate electrode 74 of transistor 70 is connected to READ line X, which is held at ground potential except during read-out of word X.

It should be mentioned at this point that WRITE line X and READ line X are common to all of the memory elements in the same row of memory 10 (FIGURE 1), and that the common digit-sense line D_1 is common to all the elements in the same column of the memory. Dashed capacitor 78 represents the total capacitance on the digit-sense line D_1 . The value of this capacitance, which may be quite high, is a function of the number of memory cells in the column and other

factors. For high speed operation, means must be provided for charging and discharging this capacitance rapidly.

A sense-driver circuit 22₁ for DIGIT line D₁ is shown at the bottom of FIGURE 2. This circuit includes an NPN bipolar transistor 80 having its emitter electrode 82 connected directly to the digit-sense line D₁. An impedance element 86, illustrated as a resistor, is connected between the collector electrode 84 and the positive terminal of a source 88 of V₂ volts, the negative terminal of the source being grounded. An output terminal 90 is connected at collector electrode 84 for deriving sense output signals.

A second NPN transistor 94 is connected in the emitter circuit of transistor 80 and is biased for operation as a substantially constant current sink. Biasing is provided by a pair of resistors 96 and 98 connected in series between the positive terminal of source 88 and the negative terminal of a source 100 of V₃ volts, the positive terminal of the latter source being grounded. The base electrode 104 of transistor 94 is connected to the junction of resistors 96 and 98, and emitter electrode 106 is connected to source 100 by a resistor 108.

The base electrode 92 of first transistor 80 is connected to a source 112 of digital signals, which source may be one section of the data input device 20 of FIGURE 1. The digital signals have either a first, relatively high value or a second relatively low value. Since transistor 80 operates as an emitter follower, the voltages at emitter 82 follows the applied base 92 voltage. The high level and low level input signals preferably have values which result in voltages of +V₁ volts and ground potential, respectively, at emitter electrode 82.

Thus within driver sense circuit 22, transistor 80 operating as an emitter follower and transistor 94 operating as a constant current source function as a device which is coupled to and which presents low impedance to the input-(digit-) sense line D₁ for reasons explained below.

Consider now the operation of the FIGURE 2 circuitry. WRITE line X and READ line X are maintained at ground potential, except when writing a new word into the flip-flops in row X or sensing the outputs thereof. Transistors 56 and 70 are biased in the off condition, whereby the input to flip-flop 30 and the gate means 66 are effectively decoupled from the digit-sense line D₁ irrespective of the voltage applied on that line through transistor 80. Thus, it is possible to write into or read out of the elements in another row at this time without affecting the state of flip-flop 30 in any way, and without the flip-flop 30 or gate means 66 affecting the digit-sense line D₁ and other flip-flops coupled thereto.

When it is desired to write a binary "0" into flip-flop 30, control source 54 applies a voltage of +V₁ volts on WRITE line X. This voltage biases transistor 50 off in the flip-flop, and biases transistor 56 on. Input source 112 applies a low level signal to the base 92 of the transistor 80, whereby the voltage on the digit-sense line remains or becomes ground potential. If capacitor 78 is charged at this time, the capacitor discharges rapidly through the constant current sink (transistor 94 and related circuitry), which is operated at a high current level. The ground potential on digit-sense line D₁, applied through on transistor 56, biases transistor 34 on and biases transistor 32 off. The voltage at output junction 44 then is +V₁ volts, which biases transistor 40 on and biases transistor 42 off. This is the reset state of the flip-flop. At the termination of the WRITE period, the voltage on WRITE line X falls to ground potential. Transistor 50 then turns on to complete the feedback loop, and transistor 56 turns off, thereby decoupling the flip-flop input from digit-sense line D₁.

To write a binary "1" into flip-flop 30, source 54 applies +V₁ volts on WRITE line X, whereby transistor 50 turns off and transistor 56 turns on. Input source 112 now operates to apply a high level input to transistor 80, whereby the voltage on digit-sense line D₁ rises to +V₁ volts. Emitter follower transistor 80 provides a low output impedance drive for rapidly charging capacitor 78. The +V₁ volts on the digit sense line D₁, applied through on transistor 56, biases transistor 32 on and biases transistor 34 off. The voltage at output junction 44 then falls to ground potential, biasing transistor 42 on and biasing transistor 40 off. This is the set state of the flip-flop.

During a read, or sense, operation all the WRITE lines are held at ground potential, and all the READ lines except a selected one are held at ground potential. To sense the output of flip-flop 30, source 76 applies +V₁ volts on READ line X. This voltage biases transistor 70 on. Input source 112 operates to supply a low level signal to transistor 80, whereby the voltage on digit-sense line D₁ is at ground potential. If the flip-flop 30 is in the reset state at this time, the voltage at output junction 46 is ground potential, transistor 68 in the coincidence gate means 66 is held off, and no current flows in the digit-sense line D₁. All of the current for the current sink then is supplied by transistor 80, and there is a large voltage drop across collector resistor 86.

If the flip-flop is in the set state, however, transistor 68 is biased on by the output of the flip-flop, and transistors 68 and 70 provide a relatively low impedance path for current flow from source 36 to the current sink. The current flowing through transistor 80 is re-

duced an amount equal to the value of the current flowing through transistors 68 and 70. There is then less current flow through collector resistor 86, a smaller voltage drop across this resistor, and a higher voltage at output terminal 90. The voltage at this terminal 90 may be sampled at this time to determine the state of the flip-flop.

It should be noted that the sense operation does not destroy the information stored in flip-flop 30. Since the WRITE line X is held at ground potential, transistor 56 is biased off, and no new information can be written into the flip-flop. Also, current sensing is employed rather than voltage sensing. In particular, the voltage on the digit-sense line D_{1a} and, hence the charge on capacitor 78, is determined by the input voltage of transistor 80, and is not dependent upon the operating states of transistors 68 and 70. It is the current flowing through transistors 68 and 70 and in the digit-sense line D_{1a} , as determined by the state of flip-flop 30 that is sensed by circuit 22, which current is converted into a voltage drop or rise across collector resistor 86.

Another type of active memory cell is illustrated in FIGURE 3. This cell utilizes a single WORD line X for both write and read selection, but employs two DIGIT lines D_{1a} and D_{1b} . DIGIT line D_{1b} is used for both writing a "1" into the cell and for sensing the output of the cell. DIGIT line D_{1a} is used for writing a "0" into the cell.

The flip-flop portion of the cell is shown within dashed box 30' and comprises two directly cross-coupled circuit branches. A first branch includes the series connected conduction paths of transistors 32 and 34, and the second branch includes the conduction paths of transistors 40 and 42. The first circuit branch is connected to voltage source 36 by way of the parallel connected conduction paths of two P-type insulated-gate field-effect transistors 120 and 122. Transistors 124 and 126 are similarly connected with the second branch. N-type transistors 130 and 132 have their conduction paths connected between output junctions 44 and 46, respectively, and circuit ground by way of a common N-type transistor 134.

An output coincidence gate means 66' comprises a P-type insulated-gate field-effect transistor 140 and an N-type transistor 142 having their conduction paths serially connected between the positive terminal of voltage source 36 and the digit-sense line D_{1b} . The gates of transistors 126 and 132 also are connected to this line D_{1b} . Transistor 140 has its gate connected to the output junction 46 of the flip-flop, and transistor 142 has its gate connected to WORD line X. In addition, the gates of transistors 122, 124 and 134 are connected to WORD line X which, in turn, is connected to the output of a

READ/WRITE selection control source 150. Transistors 120 and 130 have their gates connected to DIGIT line D_{1a} . Both of the DIGIT lines D_{1a} and D_{1b} may be connected to separate circuits of the type shown at the bottom of FIGURE 2 and identified by reference character 22. In the circuit for DIGIT line D_{1a} , however, the collector resistor 86 and output terminal 90 could be omitted since no measuring is performed on line D_{1a} .

In operation, the voltages applied on WORD line X and DIGIT lines D_{1a} and D_{1b} have a value of either $+V_1$ volts or ground potential (or approximately these values). When the voltage on WORD line X is zero, transistors 134 and 142 are biased off, whereby no information can be written into the memory cell, and no output of the cell can be sensed. Transistors 122 and 124 are biased on and provide low impedance paths from source 36 to the flip-flop circuit branches to maintain the state of the flip-flop.

To write a binary "1" into the flip-flop, source 150 applies $+V_1$ volts on WORD line X. Concurrently, voltages of zero and $+V_1$ volts are applied on DIGIT lines D_{1a} and D_{1b} , respectively. Transistors 132 and 134 then are biased on and apply ground potential at output junction 46. Transistors 124 and 126 are now biased off, whereby the voltage at output junction 46 must remain at or fall to ground potential regardless of the biasing at the gates of transistor 40 and 42. With ground potential at junction 46, transistor 32 is biased off and transistor 34 is biased on. Thus, the voltage at output junction 44 remains at or rises to $+V_1$ volts (transistor 120 is biased on at this time by the ground potential on DIGIT line D_{1a}). This voltage turns transistor 40 on and biases transistor 42 off. This is the set-state of the flip-flop in which a binary "1" is stored, and the voltage at junction 46 is at ground potential (opposite to the conditions for the flip-flop of FIGURE 2).

To write a "0" into the flip-flop, $+V_1$ volts is applied on WORD line X and DIGIT line D_{1a} , and ground potential is applied on the DIGIT line D_{1b} . Transistors 120, 122 and 124 then are biased off and transistors 130 and 134 are biased on. The voltage at output junction 44 is driven to ground potential, turning transistor 42 on and turning transistor 40 off. This is the reset state of the flip-flop, and the voltage at output junction 46 is $+V_1$ volts.

To sense the output of the flip-flop, both of the DIGIT lines D_{1a} and D_{1b} are held at ground potential, and the voltage on WORD line X is raised to $+V_1$ volts. Although transistor 134 is now biased on, no new information is written into the flip-flop because transistors 130 and 132 are biased off. Transistors 120 and 126 remain on and maintain the status of the flip-flop. Transistor 142 in

the coincidence gate means 66' is biased on by the +V₁ volts on WORD line X. If a "1" is stored in the flip-flop, the voltage at output junction 46 is zero and transistor 140 then is biased on. There is then a relatively low impedance path through transistors 140 and 142, and current flows from source 36 to the digit-sense line D_{1b}. This current results in a change of voltage at output terminal 90 of the sense circuit 22₁ (see FIGURE 2), which output voltage may be sampled or strobed at this time.

Since the sense circuit 22₁ has a relatively low impedance, there is little or no change in voltage on DIGIT line D_{1b} during a sense operation. Stated in another way, output sensing is by way of current rather than voltage, and the voltage on the DIGIT line D_{1b} and, hence, the charge on the load capacitance, is not affected by the state of the sensed flip-flop during a sense operation. It should be noted, however, that if a slight rise in voltage should occur on the line D_{1b} during the sensing of a stored "1", such rise, should it be sufficient to bias transistor 132 on, would only tend to reinforce the state of the flip-flop, since the voltage at output junction 46 is zero at this time.

Reference is made to copending application No. 57216/66 (Serial No. 1,163,788) which describes and claims other memory systems.

WHAT WE CLAIM IS:—

1. A memory system comprising: an active storage element having an output point; an input-sense line; means including a coincidence gate selectively operative during a reading operation for connecting a source of first potential to the input-sense line, or not, in accordance with the condition of the storage element and a current sensing circuit having a device coupled to and which presents low impedance to the sense line, the device being operative during a reading operation for sensing current flowing from the first potential source through the gate and the input-sense line and for maintaining the input-sense line at a substantially constant second potential which is different from the first potential.

2. A memory system comprising: an active storage element having an input and an output point; an input-sense line connected to the input of the storage element; a source of first potential; means including a coincidence gate having a conduction path for connecting the source of first potential to the input sense line, the gate having a control input coupled to the storage element output point and being operative during a reading operation for controlling the impedance of the conduction path in accordance with the condition of storage element; and a current sensing circuit having a device coupled to and which presents low imped-

ance to the input-sense line, the device being operative during a reading operation for sensing current flowing from the first potential source through the gate conduction path and the input-sense line and for maintaining the input-sense line at a substantially constant second potential which is different from the first potential.

3. A system as claimed in Claim 2, wherein the low impedance device of the current sensing circuit has a constant current sink connected to the input-sense line.

4. A system as claimed in claim 3, wherein the current sensing circuit has a detector portion which includes a transistor having an emitter electrode connected to the input-sense line and a collector electrode, and the detector portion also includes an impedance element connected in the collector electrode of the transistor to define an output sense point at the junction of the collector and the impedance, and the constant current sink is connected to the emitter electrode of the transistor.

5. A system as claimed in Claim 4, wherein a control is operative during the writing operation to cause the storage element to admit a signal appearing on the digit-sense line; the current sensing circuit has a path connecting the base electrode of the transistor to a selectively operable source of digital signals of first and second values; and the transistor is effective to place the emitter electrode and digit-sense line at the first potential during a writing operation and at the second potential during a reading operation in response to the application of input signals of the first and second values, respectively, to the base electrode of the transistor.

6. A memory system comprising: an array of active storage elements functionally arranged in rows and columns; a plurality of row lines, one for each row of storage elements; a plurality of input-sense lines, one for each column of storage elements; where each storage element includes an input connected to the respective input-sense line, an output point, and a coincident gate having a conduction path connected between a source of first potential and the respective input-sense line, a first control electrode connected to the output point of the storage element, and a second control electrode connected to the respective row line; the gate being operative during a reading operation of its storage element for controlling the impedance of the conduction path in accordance with the condition of the storage element; and a plurality of current sensing circuits, each sensing circuit having a low impedance-device connected to a different input-sense line, and being operative during a reading operation for sensing current flowing from the first potential source through the gate conduction path

the coincidence gate means 66' is biased on by the $+V_1$ volts on WORD line X. If a "1" is stored in the flip-flop, the voltage at output junction 46 is zero and transistor 140 then is biased on. There is then a relatively low impedance path through transistors 140 and 142, and current flows from source 36 to the digit-sense line D_{1b} . This current results in a change of voltage at output terminal 90 of the sense circuit 22₁ (see FIGURE 2), which output voltage may be sampled or strobed at this time.

Since the sense circuit 22₁ has a relatively low impedance, there is little or no change in voltage on DIGIT line D_{1b} during a sense operation. Stated in another way, output sensing is by way of current rather than voltage, and the voltage on the DIGIT line D_{1b} and, hence, the charge on the load capacitance, is not affected by the state of the sensed flip-flop during a sense operation. It should be noted, however, that if a slight rise in voltage should occur on the line D_{1b} during the sensing of a stored "1", such rise, should it be sufficient to bias transistor 132 on, would only tend to reinforce the state of the flip-flop, since the voltage at output junction 46 is zero at this time.

Reference is made to copending application No. 57216/66 (Serial No. 1,163,788) which describes and claims other memory systems.

WHAT WE CLAIM IS:—

1. A memory system comprising: an active storage element having an output point; an input-sense line; means including a coincidence gate selectively operative during a reading operation for connecting a source of first potential to the input-sense line, or not, in accordance with the condition of the storage element and a current sensing circuit having a device coupled to and which presents low impedance to the sense line, the device being operative during a reading operation for sensing current flowing from the first potential source through the gate and the input-sense line and for maintaining the input-sense line at a substantially constant second potential which is different from the first potential.

2. A memory system comprising: an active storage element having an input and an output point; an input-sense line connected to the input of the storage element; a source of first potential; means including a coincidence gate having a conduction path for connecting the source of first potential to the input sense line, the gate having a control input coupled to the storage element output point and being operative during a reading operation for controlling the impedance of the conduction path in accordance with the condition of storage element; and a current sensing circuit having a device coupled to and which presents low imped-

ance to the input-sense line, the device being operative during a reading operation for sensing current flowing from the first potential source through the gate conduction path and the input-sense line and for maintaining the input-sense line at a substantially constant second potential which is different from the first potential.

3. A system as claimed in Claim 2, wherein the low impedance device of the current sensing circuit has a constant current sink connected to the input-sense line.

4. A system as claimed in claim 3, wherein the current sensing circuit has a detector portion which includes a transistor having an emitter electrode connected to the input-sense line and a collector electrode, and the detector portion also includes an impedance element connected in the collector electrode of the transistor to define an output sense point at the junction of the collector and the impedance, and the constant current sink is connected to the emitter electrode of the transistor.

5. A system as claimed in Claim 4, wherein a control is operative during the writing operation to cause the storage element to admit a signal appearing on the digit-sense line; the current sensing circuit has a path connecting the base electrode of the transistor to a selectively operable source of digital signals of first and second values; and the transistor is effective to place the emitter electrode and digit-sense line at the first potential during a writing operation and at the second potential during a reading operation in response to the application of input signals of the first and second values, respectively, to the base electrode of the transistor.

6. A memory system comprising: an array of active storage elements functionally arranged in rows and columns; a plurality of row lines, one for each row of storage elements; a plurality of input-sense lines, one for each column of storage elements; where each storage element includes an input connected to the respective input-sense line, an output point, and a coincident gate having a conduction path connected between a source of first potential and the respective input-sense line, a first control electrode connected to the output point of the storage element, and a second control electrode connected to the respective row line; the gate being operative during a reading operation of its storage element for controlling the impedance of the conduction path in accordance with the condition of the storage element; and a plurality of current sensing circuits, each sensing circuit having a low impedance-device connected to a different input-sense line, and being operative during a reading operation for sensing current flowing from the first potential source through the gate conduction path



of the storage element being read and through the input-sense line, and being operative for maintaining the input-sense line, at substantially constant second potential which is different from the first potential.

7. A memory system substantially as shown and described with reference to, and as illustrated by FIGURE 2 of the accompanying drawings.

8. A memory system substantially as shown and described with reference to, and as illustrative by FIGURE 3 of the accompanying drawings.

9. A memory system comprising; an array of active storage elements functionally arranged in rows and columns; a plurality of row lines, one for each row of storage elements; a plurality of input-sense lines, one for each column of storage elements; where each storage element includes an output point, and a coincidence gate; each coincidence gate

being selectively operative during a reading operation for connecting a source of first potential to the input-sense line, or not, in accordance with the condition of the respective one of the storage elements; and a plurality of current sensing circuits; each sensing circuit having a device which is coupled to and which presents low impedance to the input-sense line, the device being operative during a reading operation for sensing current flowing from the first potential source through the gate and the input-sense line and for maintaining the input-sense line at a substantially constant second potential which is different from the first potential.

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