FIG. 1

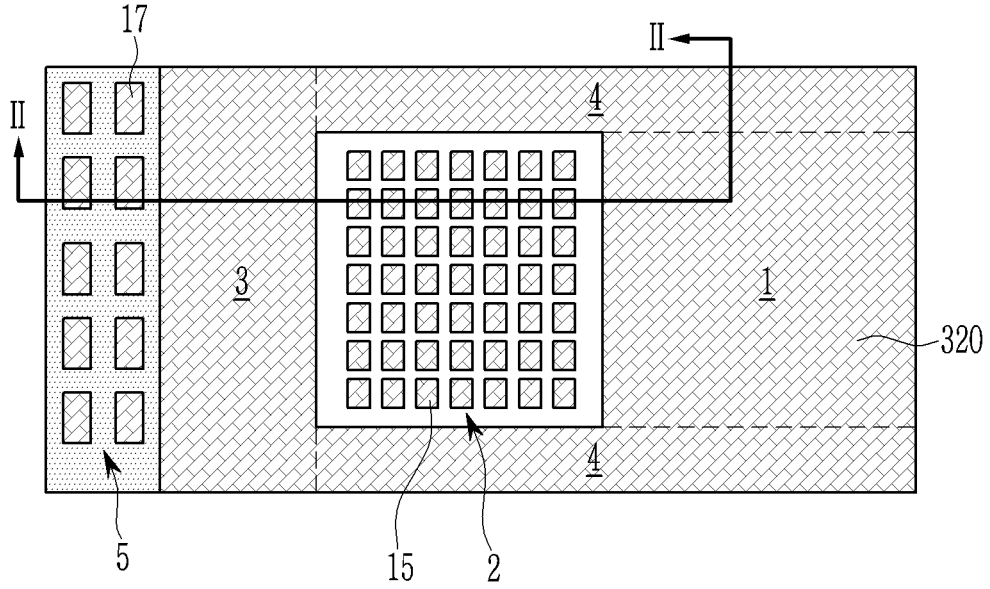


FIG. 2

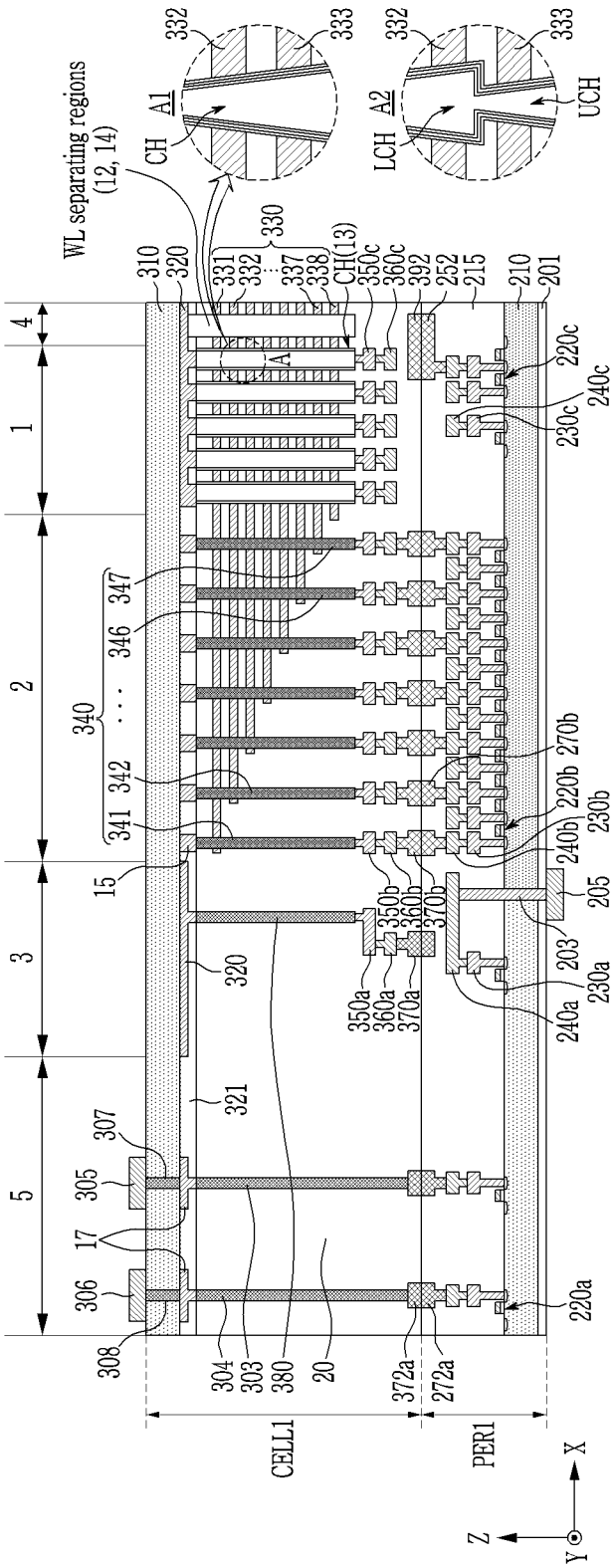

WL separating regions (12, 14)
CH
A1
LCH
A2
UCH
332
333
330
310
320
331
332
337
338
CH(13)
350c
360c
392
252
215
210
201
220c
240c
230c
347
346
340
342
341
270b
220b
230b
240b
205
203
230a
240a
350b
360b
370b
350a
360a
370a
321
307
305
17
306
308
304
303
380
20
372a
272a
220a
15
1
2
3
4
5
A
CELL1
PER1
X
Y
Z

FIG. 3

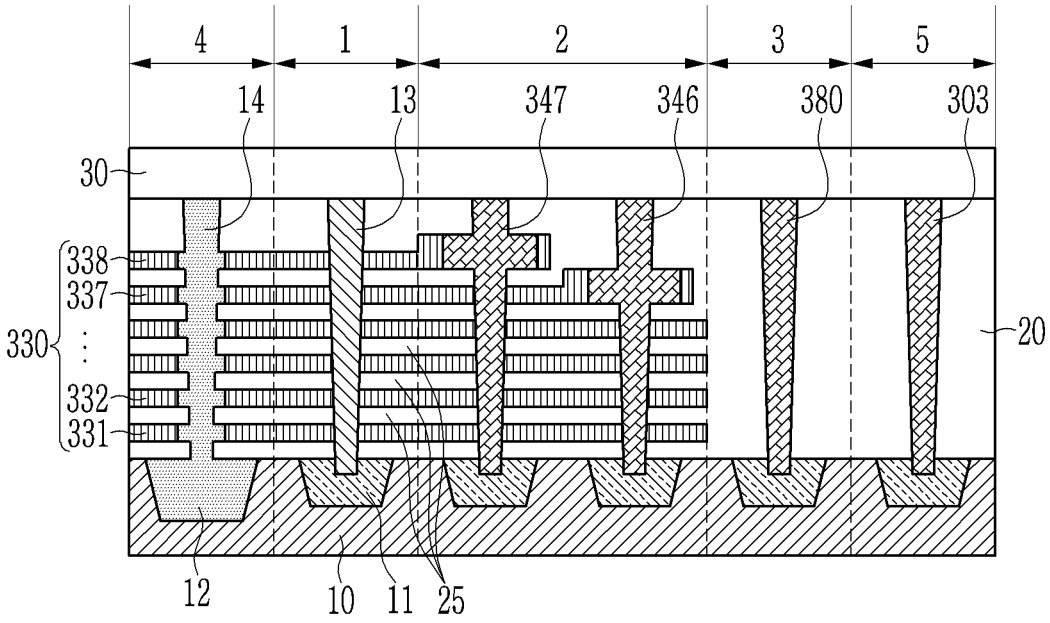


FIG. 4

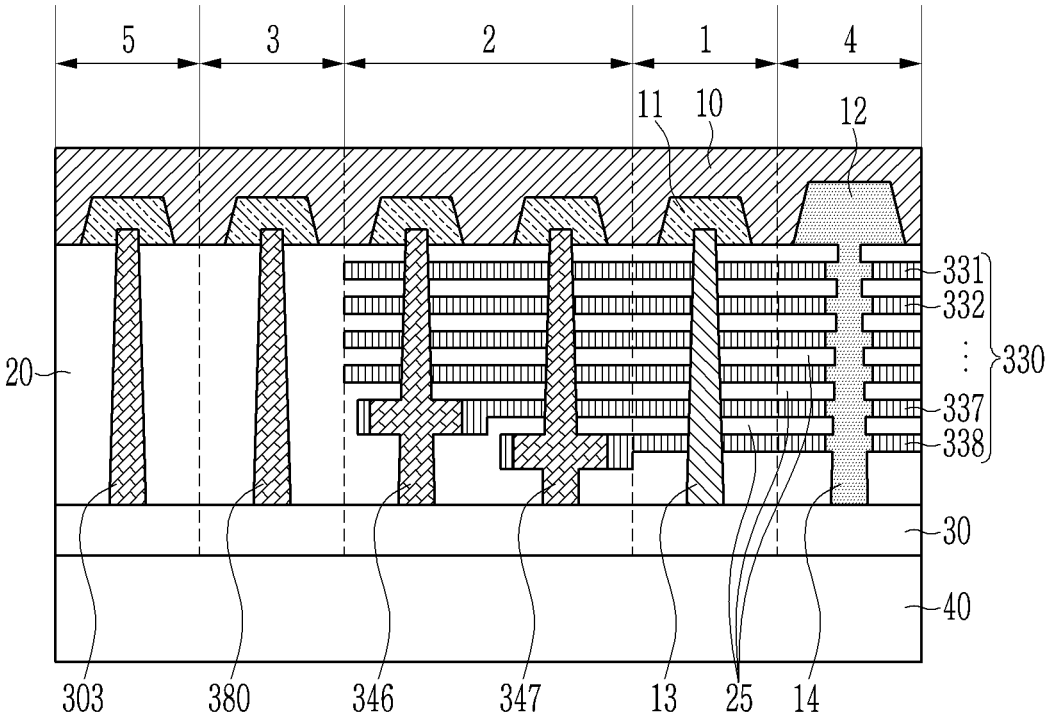

5
3
2
1
4
11
10
12
331
332
330
20
337
338
30
40
303
380
346
347
13
25
14

FIG. 5

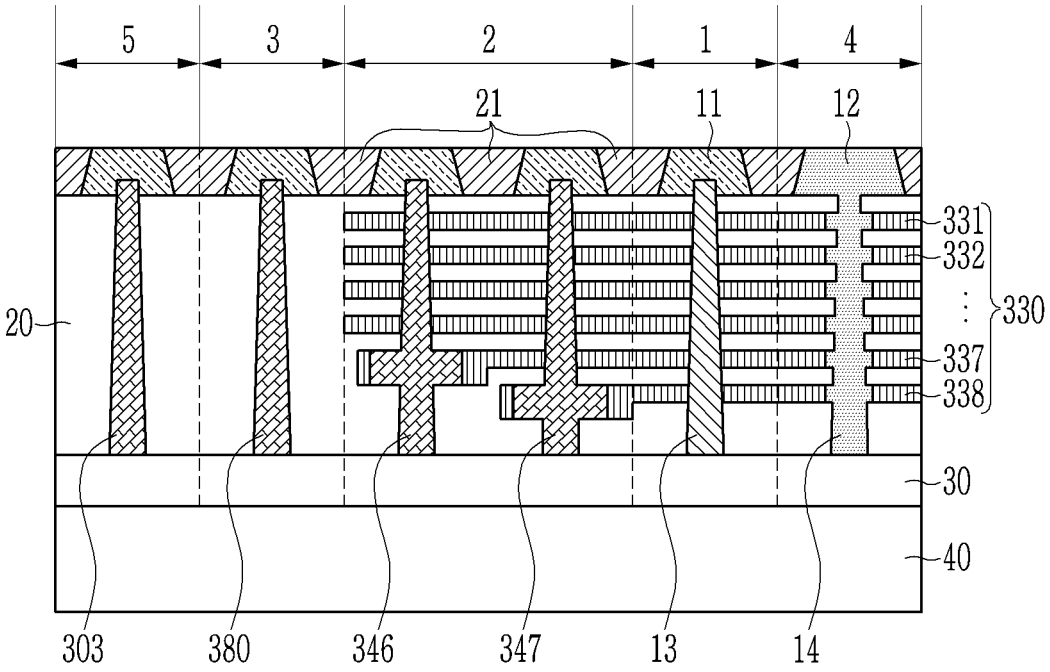


FIG. 6

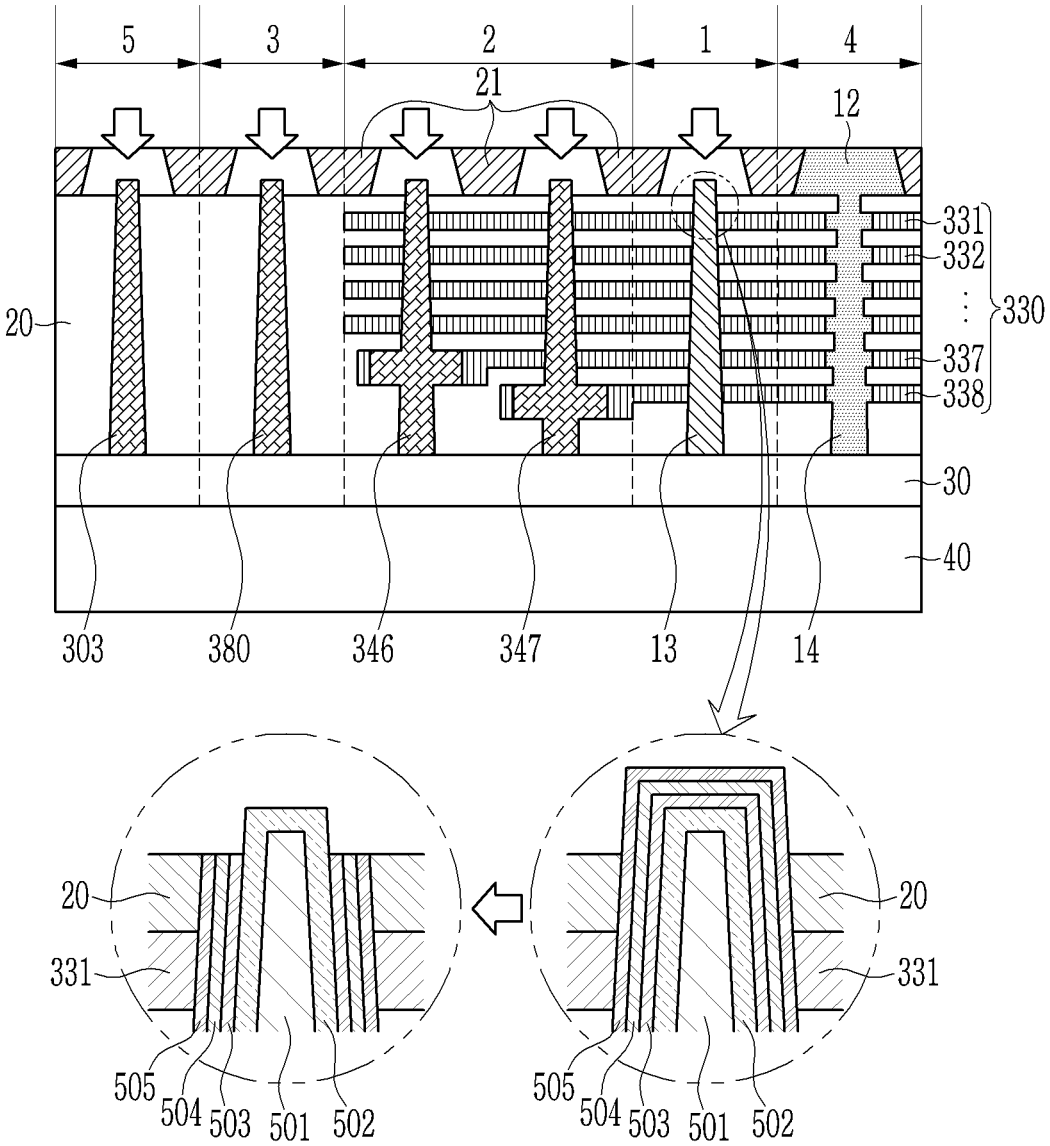

5
3
2
1
4
21
12
331
332
330
337
338
20
30
40
303
380
346
347
13
14
20
331
505
504
503
501
502
20
331
505
504
503
501
502

FIG. 7

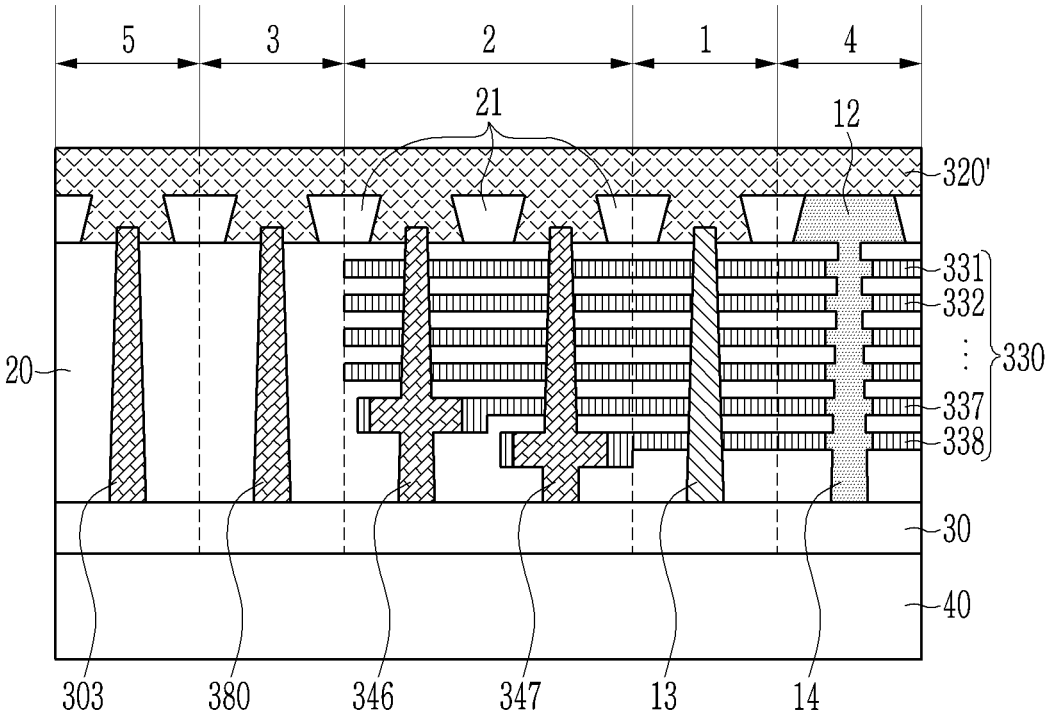


FIG. 8

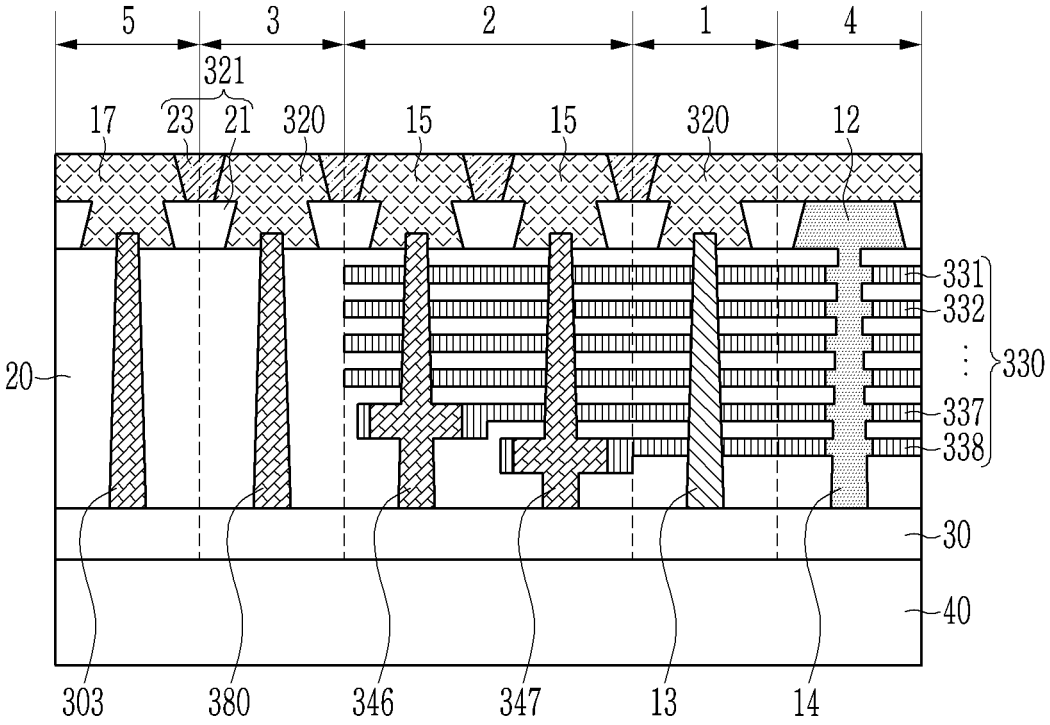

5
3
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1
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321
17
23
21
320
15
15
320
12
331
332
330
337
338
20
30
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303
380
346
347
13
14

FIG. 9

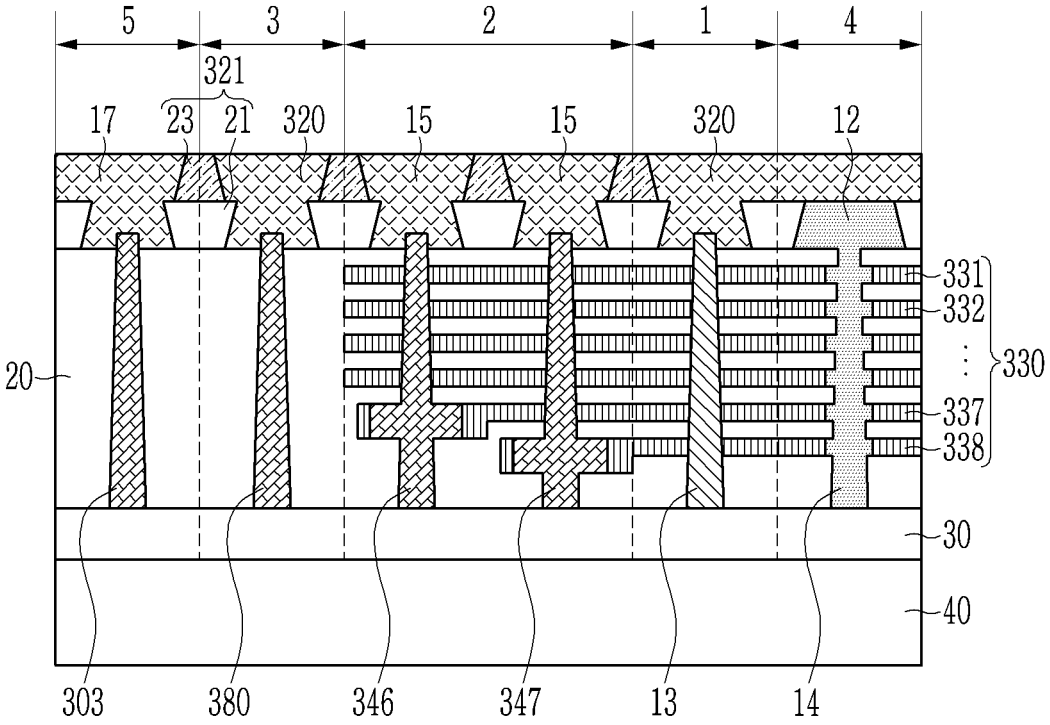

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23
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15
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12
331
332
330
337
338
20
30
40
303
380
346
347
13
14

FIG. 10

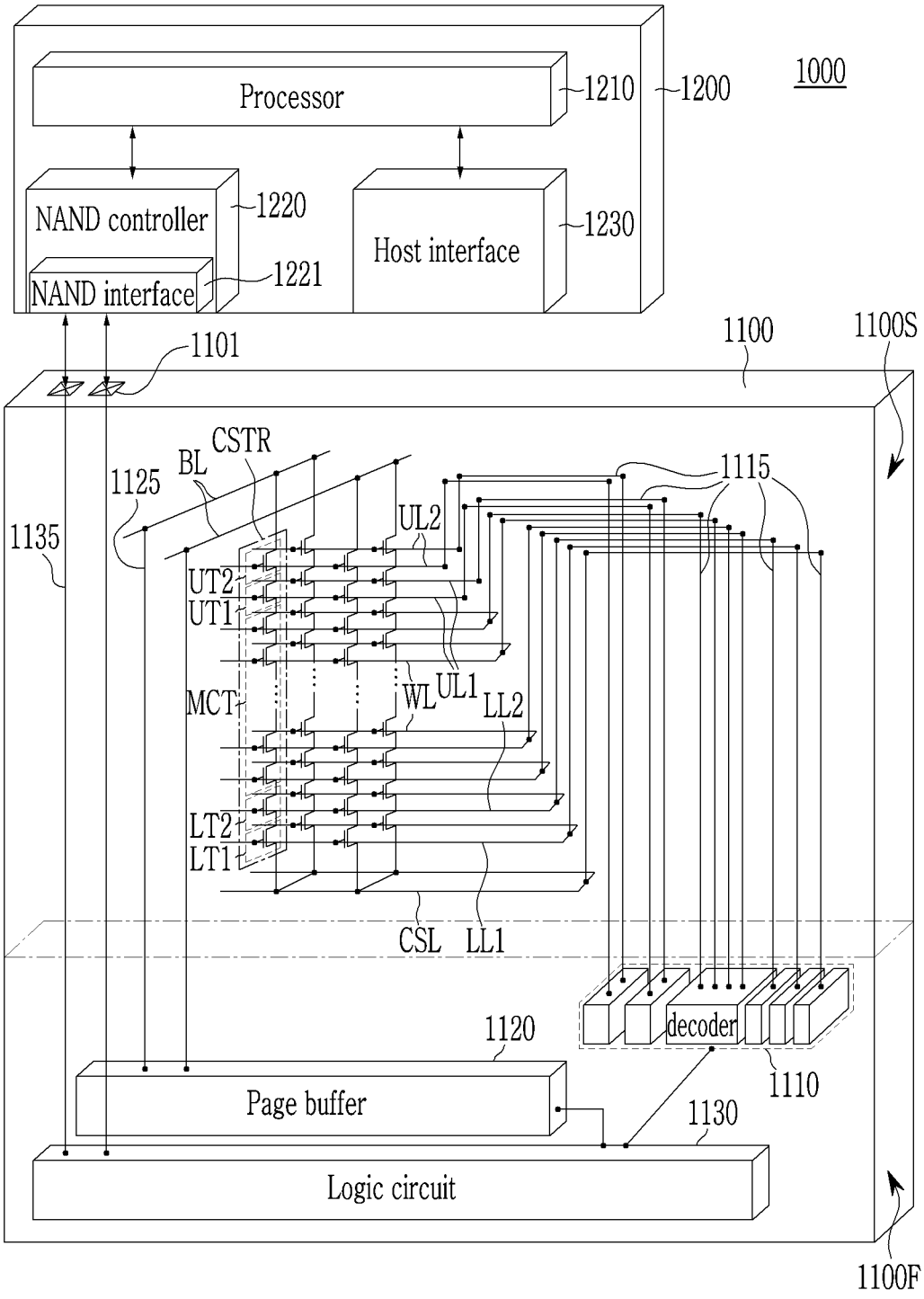
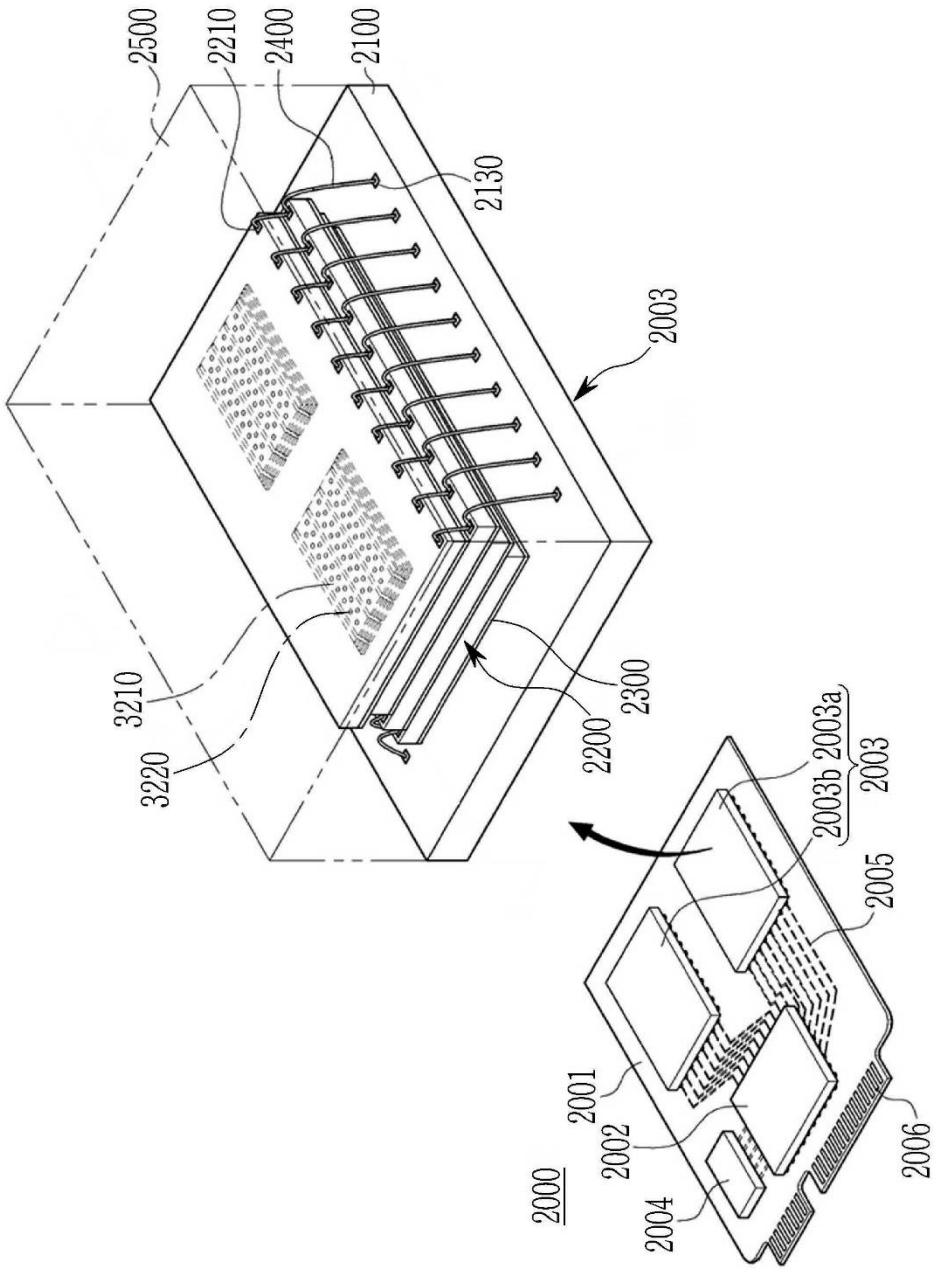

1000
Processor
1210
1200
NAND controller
1220
NAND interface
1221
Host interface
1230
1101
1100
1100S
CSTR
BL
1125
1135
1115
UL2
UT2
UT1
MCT
WL
UL1
LL2
LT2
LT1
CSL
LL1
decoder
1120
1110
Page buffer
1130
Logic circuit
1100F

FIG. 11


2500
2210
2400
2100
2130
2003
3210
3220
2200
2300
2003b
2003a
2003
2005
2001
2002
2000
2004
2006