

CURRENT SHARING MISMATCH AND SWITCHING OSCILLATION REDUCTION IN POWER SEMICONDUCTOR DEVICE MODULES

TECHNICAL FIELD

[0001] This description relates to semiconductor device assemblies. More specifically, this description relates to power semiconductor device modules.

BACKGROUND

[0002] Semiconductor devices (e.g., semiconductor die) can be included in package assemblies or modules, where such modules can include one or more semiconductor die (e.g., implemented in a circuit included in the module). The performance of semiconductor die, as well as an associated circuit in such modules can be adversely impacted by electrical impedances within the module, such as electrical resistance and/or parasitic (stray) inductance. For instance, in some power module implementations, such as half-bridge power modules including multiple parallel-connected high-side transistors and multiple, parallel-connected high-side transistors, current imbalance between parallel connected devices can cause gate signal oscillation (e.g., when switching), as well as reduce electrical efficiency of an associated module.

SUMMARY

[0003] In a general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate, a second patterned metal layer disposed on the surface of the substrate, and a third patterned metal layer disposed on the surface of the substrate. The module also includes a first high-side transistor disposed on the first patterned metal layer, a second high-side transistor disposed on the first patterned metal layer, a first conductive clip electrically coupling the first high-side transistor with the second patterned metal layer, and a second conductive clip electrically coupling the second high-side transistor with the second patterned metal layer. The module further includes a first low-side transistor disposed on the second patterned metal layer, a second low-side transistor disposed on the second patterned metal layer, a third conductive clip electrically coupling the first low-side transistor with the third patterned metal layer, and a fourth conductive clip electrically coupling the second low-side transistor with the third patterned metal layer.

[0004] In another general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate and electrically coupled with an output terminal, a second patterned metal layer disposed on the surface of the substrate and electrically coupled with a DC- terminal, a third patterned metal layer disposed on the surface of the substrate and electrically coupled with the output terminal. The module further includes a first low-side transistor disposed on the first patterned metal layer, a second low-side transistor disposed on the first patterned metal layer, a third low-side transistor disposed on the third patterned metal layer, and a fourth low-side transistor disposed on the third patterned metal layer. The module also includes a conductive clip electrically coupling the first low-side transistor, the second low-side transistor, the third low-side transistor and the fourth low-side transistor with the second patterned metal layer.

[0005] In another general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate and electrically coupled with an output terminal, a second patterned metal layer disposed on the surface of the substrate and electrically coupled with a DC- terminal, and a third patterned metal layer disposed on the surface of the substrate and electrically coupled with the output terminal. The module also includes a first low-side transistor disposed on the first patterned metal layer, a second low-side transistor disposed on the first patterned metal layer, a third low-side transistor disposed on the first patterned metal layer, a fourth low-side transistor disposed on the third patterned metal layer, a fifth low-side transistor disposed on the third patterned metal layer, and a sixth low-side transistor disposed on the third patterned metal layer. The module further includes a first conductive clip electrically coupling the first low-side transistor and the fourth low-side transistor to the second patterned metal layer, a second conductive clip electrically coupling the second low-side transistor and the fifth low-side transistor to the second patterned metal layer, and a third conductive clip electrically coupling the third low-side transistor and the sixth low-side transistor to the second patterned metal layer.

[0006] In another general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate, a second patterned metal layer disposed on the surface of the substrate; and a third patterned metal layer disposed on the surface of the substrate. The module further includes a first high-side transistor disposed on the first patterned metal layer, a second high-side transistor disposed on the first patterned metal layer; a first conductive clip electrically coupling the first high-side transistor with the second patterned metal layer, and a second conductive clip electrically

coupling the second high-side transistor with the second patterned metal layer. The module also includes a first low-side transistor disposed on the second patterned metal layer, a second low-side transistor disposed on the second patterned metal layer, a third conductive clip electrically coupling the first low-side transistor with the third patterned metal layer, and a fourth conductive clip electrically coupling the second low-side transistor with the third patterned metal layer. The module still further includes a DC+ terminal that is electrically coupled with the first patterned metal layer via a first conductive post disposed between the first high-side transistor and the second high-side transistor on the first patterned metal layer. The module also includes a DC- terminal that is electrically coupled with the third patterned metal layer via a second conductive post disposed between the third conductive clip and the fourth conductive clip on the third patterned metal layer.

[0007] In another general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate, a second patterned metal layer disposed on the surface of the substrate, a third patterned metal layer disposed on the surface of the substrate, a fourth patterned metal layer disposed on the surface of the substrate, and a fifth patterned metal layer disposed on the surface of the substrate. The module further includes a first low-side transistor disposed on the first patterned metal layer and electrically coupled with the fifth patterned metal layer via a first conductive clip, a second low-side transistor disposed on the first patterned metal layer and electrically coupled with the fifth patterned metal layer via a second conductive clip, a third low-side transistor disposed on the second patterned metal layer and electrically coupled with the fifth patterned metal layer via the first conductive clip, and a fourth low-side transistor disposed on the second patterned metal layer and electrically coupled with the fifth patterned metal layer via the second conductive clip. The module further includes a first high-side transistor disposed on the third patterned metal layer and electrically coupled with the first patterned metal layer via a third conductive clip, a second high-side transistor disposed on the third patterned metal layer and electrically coupled with the first patterned metal layer via a fourth conductive clip, a third high-side transistor disposed on the fourth patterned metal layer and electrically coupled with the second patterned metal layer via a fifth conductive clip, and a fourth high-side transistor disposed on the fourth patterned metal layer and electrically coupled with the second patterned metal layer via a sixth conductive clip. The module also includes a first DC+ terminal electrically coupled with the third patterned metal layer via a first conductive post disposed between the first high-side transistor and the second high-side transistor on the third patterned metal layer, and a second DC+ terminal electrically

coupled with the fourth patterned metal layer via a second conductive post disposed between the third high-side transistor and the fourth high-side transistor on the fourth patterned metal layer. The module further includes a DC- terminal electrically coupled with the fifth patterned metal layer via a third conductive post disposed between the first conductive clip and the second conductive clip on the fifth patterned metal layer.

[0008] In another general aspect, a method for producing a half-bridge circuit power module includes coupling a first high-side transistor with a first patterned metal layer disposed on a surface of a substrate, and coupling a second high-side transistor with the first patterned metal layer. The method also includes coupling a first low-side transistor with a second patterned metal layer disposed on the surface of the substrate, and coupling a second low-side transistor with the second patterned metal layer. The method further includes, with a first conductive clip, electrically coupling the first high-side transistor with the second patterned metal layer. The method also includes, with a second conductive clip, electrically coupling the second high-side transistor with the second patterned metal layer. The method also further includes, with a third conductive clip, electrically coupling the first low-side transistor with a third patterned metal layer disposed on the surface of the substrate, and with a fourth conductive clip, electrically coupling the second low-side transistor with the third patterned metal layer. The method also includes electrically coupling a DC+ terminal with the first patterned metal layer via a first conductive post disposed between the first high-side transistor and the second high-side transistor on the first patterned metal layer, and electrically coupling a DC- terminal with the third patterned metal layer via a second conductive post disposed between the third conductive clip and the fourth conductive clip on the third patterned metal layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is a block diagram schematically illustrating example electrical interconnections of a half-bridge power module, in accordance with an implementation.

[0010] FIG. 2 is a block diagram schematically illustrating electrical interconnections of a plurality of high-side transistors of a half-bridge power module, in accordance with an implementation.

[0011] FIG. 3 is a diagram showing a front-side perspective view of a power module, in accordance with an implementation.

[0012] FIG. 4 is a diagram illustrating a back-side view of the power module of FIG. 3.

[0013] FIG. 5 is a diagram illustrating a front-side view of an example substrate assembly that can be included in the module of FIG. 3, in accordance with an implementation.

[0014] FIG. 6 is a diagram illustrating a back-side view of the substrate assembly of FIG. 5.

[0015] FIG. 7 is a diagram illustrating a side view of the substrate assembly of FIG. 5.

[0016] FIG. 8 is a diagram illustrating a front-side perspective view of a power module including the substrate assembly of FIGS. 5-7, in accordance with an implementation.

[0017] FIG. 9 is a front-side view of the power module of FIG. 8.

[0018] FIGS. 10A and 10B are diagrams illustrating, respectively, a perspective view and a side view of a high-side transistor clip that can be included in the substrate assembly of FIGS. 5-7 and/or the power module of FIGS. 8 and 9, in accordance with an implementation.

[0019] FIGS. 11A and 11B are diagrams illustrating, respectively, a perspective view and a side view of a low-side transistor clip that can be included in the substrate assembly of FIGS. 5-7 and/or the power module of FIGS. 8 and 9, in accordance with an implementation.

[0020] FIG. 12 is a diagram illustrating a front-side view of another example substrate assembly, in accordance with an implementation.

[0021] FIGS. 13A and 13B are diagrams illustrating, respectively, a perspective view and a side view of a low-side transistor clip that can be included in the substrate assembly of FIG. 12.

[0022] FIG. 14 is a diagram illustrating a front-side view of a power module including the substrate assembly of FIG. 12, in accordance with an implementation.

[0023] FIG. 15 is a diagram illustrating a front-side view of another example substrate assembly, in accordance with an implementation.

[0024] FIG. 16 is a diagram illustrating a front-side perspective view of the substrate assembly of FIG. 15.

[0025] FIGS. 17A and 17B are diagrams illustrating, respectively, a perspective view and a side view of a high-side transistor clip that can be included in the substrate assembly of FIGS. 15 and 16.

[0026] FIG. 18 is a diagram illustrating a front-side view of another example substrate assembly, in accordance with an implementation.

[0027] FIG. 19 is a diagram illustrating a front-side view of a power module including the substrate assembly of FIG. 18, in accordance with an implementation.

[0028] FIG. 20 is a flowchart illustrating a method for producing a power module, such as the power modules of, e.g., FIGs. 3, 4, 8, 9, 14 and 19, in accordance with an implementation.

[0029] FIG. 21 is a diagram illustrating a front-side view of another example substrate assembly, in accordance with an implementation.

[0030] FIG. 22 is a diagram illustrating a front-side view of a power module including the substrate assembly of FIG. 21, in accordance with an implementation.

[0031] FIG. 23 is a diagram illustrating an example leadframe assembly including a plurality of conductive posts, which can be included in the power module of FIG. 22.

[0032] FIG. 24 is a graph illustrating shear strength values for example leadframes and conductive post assemblies.

[0033] Like reference symbols in the various drawings indicate like elements. Reference numbers for some like elements may not be repeated for all such elements. In certain instances, different reference numbers may be used for like, or similar elements. Some reference numbers for certain elements of a given implementation may not be repeated in each drawing corresponding with that implementation. Some reference numbers for certain elements of a given implementation may be repeated in other drawings corresponding with that implementation, but may not be specifically discussed with reference to each corresponding drawing. The drawings are for purposes of illustrating example implementations and may not necessarily be to scale.

DETAILED DESCRIPTION

[0034] This disclosure relates to packaged semiconductor device apparatus, which can be referred to as modules, semiconductor device modules, power semiconductor device modules, such as half-bridge power modules. The approaches illustrated and described herein can be used to implement semiconductor device modules (e.g., half-bridge power modules in the implementations described herein) that operate with improved current sharing (reduced mismatch) between parallel connected devices of a half-bridge circuit implemented in power module. While the approaches described here are generally described for half-bridge power modules, in some implementations power modules implementing other circuits are possible, such as for instance, a full-bridge power module, a 3-phase half-bridge module, a multi-phase half-bridge module, etc.

[0035] In the implementations described herein, mismatch in current sharing between parallel-connected high-side transistors, as well as mismatch in current sharing between

parallel-connected low-side transistors of a half-bridge circuit (power module) can be reduced. That is, the approaches described herein can improve balance of respective switching currents of parallel-connected transistors (e.g., balance respective high-side switching currents and/or balance respective low-side switching currents), which can also improve electrical efficiency of an associated power module.

[0036] In previous power modules, current sharing mismatch results from differences in conduction paths for switching currents, such as respective current path lengths for each parallel connected transistor. These differences in current paths, due to differences in electrical interconnection paths (e.g., overall physical path length, type of interconnects, etc.) of the circuit result in different electrical impedances for each of the parallel-connected transistors (e.g., differences in electrical resistance and/or differences in stray inductance). These electrical impedance differences contribute to and/or cause current mismatch between parallel connected devices, which in turn causes gate signal oscillation and reduces overall power consumption efficiency of the power module. For instance, transistors with longer current conduction paths (at the end of a conductive clip) will observe high impedance (resistance and stray inductance) than transistors with shorter current conduction paths (at the beginning of a conductive clip).

[0037] In the disclosed implementations, reductions in current sharing mismatch can be achieved as a result of more closely matching (physically and electrically) respective current conduction paths of parallel-connected transistors, e.g., by improving conduction path symmetry. Such current conduction path matching will reduce (or eliminate) the impedance differences (electrical resistance and stray inductance) observed by parallel-connected transistors and, as result, improve, or balance current sharing between the parallel-connected transistors.

[0038] The example power module implementations described herein include half-bridge circuits that include high-side (HS) transistors and low-side (LS) transistors. In some implementations, vertical power field-effect transistors (FETs) can be used for the HS and LS transistors of the disclosed half-bridge modules. In some implementations, bipolar transistors such as insulated-gate bipolar transistors (IGBTs) can be used for the HS and LS transistors. For purposes of illustration and discussion, disclosed implementations will be described as being implemented using vertical power FETs.

[0039] FIG. 1 is a block diagram schematically illustrating example electrical interconnections of a half-bridge power module 100, in accordance with an implementation. As shown in FIG. 1, the half-bridge power module 100 includes a HS transistor 110a, a HS

transistor 110b, a HS transistor 110c, and a HS transistor 110d, where each HS transistor can be implemented using a vertical power FET semiconductor die. The HS transistor 110a and the HS transistor 110b are coupled in a common drain configuration with each other via a connection bus 117a, which can be implemented as a patterned metal layer on a substrate, e.g., a direct-bonded-metal (DBM) substrate, such as a direct-bonded-copper (DBC) substrate.

[0040] Similarly, the HS transistor 110c and the HS transistor 110d can be coupled in a common drain configuration with each other via a connection bus 117b, which can also be implemented as a patterned metal layer on the substrate (e.g., separate from first connection bus 117a). In this example, the HS transistor 110a and the HS transistor 110b can each have their drain terminals disposed on the connection bus 117a, while the HS transistor 110c and the HS transistor 110d can each have their drain terminals disposed on the connection bus 117b. In the half-bridge power module 100, the connection bus 117a is electrically coupled with a DC+ terminal 115a, while the second connection bus 117b is electrically coupled with a DC+ terminal 115b. The terminal DC+ terminal 115a and the DC+ terminal 115b can be coupled to a same potential, e.g., a positive battery terminal, during operation of the half-bridge power module 100.

[0041] The half-bridge power module 100 of FIG. 1 further includes a connection bus 130 and a connection bus 140. As shown in FIG. 1, the connection bus 130 is electrically coupled with an output terminal 135 of the half-bridge power module 100, while the connection bus 140 is electrically coupled with a DC- terminal 125 of the half-bridge power module 100. In some implementations, the connection bus 130 and the connection bus 140 can include one or more respective patterned metal layers on a substrate (e.g., such as a DBM substrate). That is, in some implementations, the connection bus 130 and/or the connection bus 140 can each include, respectively, multiple patterned metal layers on a substrate.

[0042] As shown in FIG. 1, the half-bridge power module 100 includes a LS transistor 120a, a LS transistor 120b, a LS transistor 120c, and a LS transistor 120d, where each LS transistor can be implemented using a vertical power FET semiconductor die. In the example of FIG. 1, the LS transistors are coupled with each other in a common drain configuration via the connection bus 130, that is their drain terminals are disposed on and electrically coupled with the connection bus 130. In some implementations, multiple connection busses can be used that each are electrically coupled with the output terminal 135 to define a common drain configuration between all the LS transistors of the half-bridge power module 100.

[0043] As shown in FIG. 1, the half-bridge power module 100 includes a conductive clip 132a that is used to electrically couple a source terminal of the HS transistor 110a to the connection bus 130 and the output terminal 135. Similarly, the half-bridge power module 100 includes a conductive clip 132b, a conductive clip 132c and a conductive clip 132d that are used, respectively to electrically couple corresponding source terminals of the HS transistor 110b, the HS transistor 110c and the HS transistor 110d to the connection bus 130 (and the output terminal 135). Such an approach, e.g., using a separate conductive clip for coupling each HS transistor to the connection bus 130 improves current path symmetry (balances current conduction path length) as compared to previous approaches in which a single conductive clip is used to electrically couple, in a daisy-chained configuration, multiple HS transistors with an output node. Accordingly, because the current paths (lengths) for the HS transistors are balanced (symmetric), gate oscillation and current sharing variation can be reduced.

[0044] As also shown in FIG. 1, the half-bridge power module 100 includes a conductive clip 142a that is used to electrically couple a source terminal of the LS transistor 120a and a source terminal of the LS transistor 120c to the connection bus 140 and the DC-terminal 125. Similarly, the half-bridge power module 100 includes a conductive clip 142b, that is used to electrically couple a source terminal of the LS transistor 120b and a source terminal of the LS transistor 120d to the connection bus 140 and the DC-terminal 125. As with the conductive clips used to connect the HS transistors of the half-bridge power module 100 to the connection bus 117a and the connection bus 117b, use of the conductive clip 142a and the conductive clip 142b for coupling the LS transistors to the connection bus 140 (DC-terminal 125 of the half-bridge power module 100) improves current path symmetry (balances current conduction path length) as compared to previous approaches in which a conductive clip is used, in a daisy-chained configuration, to electrically couple multiple LS transistors with an output node. Accordingly, because the current paths for the LS transistors are balanced (symmetric), gate oscillation and current sharing variation can be reduced.

[0045] FIG. 2 is a block diagram schematically illustrating electrical interconnections of a plurality of LS transistors of a half-bridge power module 200 (HS transistors and associated connections not shown), in accordance with an implementation. While connection of LS transistors is shown in FIG. 2, in some implementations, HS transistors of a half-bridge circuit (or transistors of other circuits) could be interconnected in a similar way. In half-bridge circuits, however, the connection bus to which source terminals of HS transistors

would be coupled would differ (e.g., an output node connection bus instead of a DC- terminal connection bus).

[0046] In FIG. 2, the half-bridge power module 200 includes a LS transistor 220a, a LS transistor 220b, a LS transistor 220c, a LS transistor 220d, a LS transistor 220e, a LS transistor 220f, a LS transistor 220g, and a LS transistor 220h, which can be connected in a common drain configuration. As shown in FIG. 2, the LS transistors 220a-220d (respective source terminals of the LS transistors) are electrically coupled to a connection bus 240 via a conductive clip 242a. In example implementations, the connection bus 240 can then be electrically coupled with a DC- terminal (not shown). Similarly in the half-bridge power module 200, the LS transistors 220e-220h (respective source terminals of those LS transistors) are electrically coupled to the connection bus 240 via a conductive clip 242b. As shown in FIG.2, the conductive clip 242a and the conductive clip 242b balance the current conductive paths (implement balanced, equal, symmetric, etc.) current path lengths for each of the LS transistors 220a-220g to the connection bus 240. This approach can balance current sharing, reduce gate oscillation, and improve electrical performance efficiency of an associated half-bridge power module.

[0047] Also schematically shown in FIG. 2 is a conductive post 241 which can be used for electrically coupling a DC- terminal to the connection bus 240. This can further balance current conduction path lengths for the LS transistors 220a -220g to an associated DC- terminal, as compared to approaches where the DC- terminal is coupled at an end of a corresponding connection bus (e.g., the connection bus 240).

[0048] FIG. 3 is a diagram showing a front-side perspective view of a power module 300 in accordance with an implementation. The power module 300 is shown for purposes of illustration as an example power module configuration that can be used with the example implementations of half-bridge power module implementations described herein, though could be used with other power module configurations. As shown in FIG. 3, the power module 300 includes a molding compound 305 that encapsulates portions of the power module 300, such as a DBM substrate, a plurality of semiconductor die, conductive clips and wire bonds. As shown in FIG. 3, a DC+ terminal 315a, a DC+ terminal 315b, and a DC- terminal 325 of the power module 300 can be exposed through the molding compound 305. The module 300 also includes press-fit pins 350 that can be inserted through corresponding openings in the molding compound 305. The press-fit pins 350 can be used for control signals and monitoring signals for the power module 300. For instance, the press-fit pins 350 can be used for gate control (HS and LS) signals, source sense signals, temperature sense signals,

etc. As further shown in FIG. 3 (and in FIG. 4), the power module 300 includes an output terminal 335 of a half-bridge circuit implemented in the power module 300.

[0049] FIG. 4 is a diagram illustrating a back-side view of the power module 300 of FIG. 3. As shown in FIG. 4, a DBM substrate 405 can be exposed through the molding compound 305. In some implementations, a metal layer can be disposed on a back side of the DBM substrate 405. This back-side metal layer can facilitate thermal energy dissipation for the power module 300. For example, in some implementations, a thermal dissipation appliance can be coupled with such an exposed metal layer of the DBM substrate 405 on the back side of the power module 300.

[0050] FIGs. 5-7 are diagrams illustrating, respectively, a front-side view, a back-side view and a side view of an example substrate assembly 500 implementing a half-bridge circuit that, in some implementations, can be included in a power module, such as the power module 300. As shown in FIGs. 5-7, the substrate assembly 500 includes a DBM substrate 505 and a printed circuit board substrate (PCB 507). In some implementations, the PCB 507 can be physically coupled with the DBM substrate 505, but electrically isolated from the DBM substrate 505 (other than wire bonds from signal traces on the PCB 507 to semiconductor die and conductive clips disposed on the DBM substrate 505). That is, in this example and other implementations described herein, wire bonds to a DBM substrate (e.g., down bonds) can be excluded. This can be beneficial, as no plating on the DBM substrate 505 is used to facilitate wire bonding, which can reduce cost and improve reliability, as such down bonds may present reliability issues (e.g., in thermal cycling).

[0051] In this example, the DBM substrate 505 can have HS and LS transistors, conductive clips, and conductive posts disposed thereon. The PCB 507 can be used to connect signal pins with the half-bridge circuit of the substrate assembly 500, e.g., using wire bonds 550a, 550b, 550c, 550d, 550e, 550f, 550g, and 550h. For instance, in this example, wire bonds 550a and 550h can be used to provide gate control signals from the PCB 507 and corresponding press-fit pins to HS transistors 510. Die to die wire bonding can be used for electrically coupling the gates of the HS transistors 510 to one another, such as shown in FIG. 5. Also in the substrate assembly 500, the wire bonds 550c and 550f can be used for providing gate control signals from the PCB 507 and corresponding press-fit pins to LS transistors 520. As with the HS transistors, die to die wire bonding can be used to connect the gates of the LS transistors 520 to one another, such as shown in FIG. 5.

[0052] In the example of FIG. 5, the DBM substrate 505 has a patterned metal layer 517a, a patterned metal layer 517b, a patterned metal layer 530a, a patterned metal layer

530b, and a patterned metal layer 540 (e.g., separate connections busses). In the example of FIG. 5, a first plurality of HS transistors 510 is disposed (in a common drain configuration) on the patterned metal layer 517a, and a second plurality of HS transistors 510 is disposed (in a common drain configuration) on the patterned metal layer 517b. The patterned metal layer 517a can be coupled with a first DC+ terminal (not shown) via a conductive post 517c, such as a copper post, or other electrically conductive material. The patterned metal layer 517b can be coupled with a second DC+ terminal (not shown) via a conductive post 517d.

[0053] As also in the example of FIG. 5, a first plurality of LS transistors 520 is disposed (in a common drain configuration) on the patterned metal layer 530a, and a second plurality of LS transistors 520 is disposed (in a common drain configuration) on the patterned metal layer 530b. The patterned metal layer 530a and the patterned metal layer 530b can be coupled with an output terminal (not shown), respectively, via a conductive post 530c and 530c.

[0054] As further shown in FIG. 5, each HS transistor 510 of the first plurality of HS transistors disposed on the patterned metal layer 517a can have its source terminal electrically coupled with the patterned metal layer 530a, respectively, using a conductive clip 532. In some implementations, the patterned metal layer 530a can be electrically coupled with an output terminal (not shown) for the associated half-bridge circuit via a conductive post 530c. Likewise, each HS transistor 510 of the second plurality of HS transistors disposed on the patterned metal layer 517b can have its source terminal electrically coupled with the patterned metal layer 530b, respectively, using a conductive clip 532. In some implementations, the patterned metal layer 530b can be electrically coupled with an output terminal (not shown) via a conductive post 530d. In the arrangement shown in FIG. 5, the use of the conductive clips 532 balances the current conduction paths of the HS transistors 510 to an associated output terminal, which can reduce gate oscillation, balance and or reduce stray inductance, and improve operating efficiency of power modules including the substrate assembly 500.

[0055] Further, each LS transistor 520 of the first plurality of LS transistors disposed on the patterned metal layer 530a and a corresponding LS transistor 520 disposed on the patterned metal layer 530b can have their source terminals electrically coupled with the patterned metal layer 540 using a conductive clip 542. That is, the conductive clips 542 are configured to couple source terminals of two LS transistors 520 with a DC- terminal with equal (balanced) current conduction path lengths. In some implementations, the patterned metal layer 540 can be coupled with a DC- terminal (not shown) via a conductive post 540a.

In the arrangement shown in FIGs. 5, the use of the conductive clips 542 balances the current conduction paths of the LS transistors 520 to an associated DC- terminal, which can reduce gate oscillation, balance and or reduce stray inductance, and improve operating efficiency of the power modules including the substrate assembly 500.

[0056] As shown in FIG. 5, the PCB 507 includes through-holes 555 for receiving press-fit pins, such as the press-fit pins 350 of FIG. 3. For instance, the through-holes 555 can include copper holders (rings) that are soldered in the PCB 507 that are configured to receive and retain respective press-fit pins. A back side of the DBM substrate 505 and the PCB 507 are shown in FIG. 6., while the relationship of the conductive post 517d and the conductive post 530d to the DBM substrate 505 and the PCB 507 is shown in FIG. 7.

[0057] FIG. 8 is a diagram illustrating a front-side perspective view of a power module 800 including the substrate assembly of FIGs. 5-7, in accordance with an implementation. As shown in FIG. 8, similar to the power module 300, the power module 800 includes a molding compound 805 (illustrated as transparent to show internal structure of the power module 800), a terminal 815a, a DC+ terminal 815b, a DC- terminal 825, an output terminal 835 and press-fit pins 850. FIG. 8 further illustrates the conductive post 540a and the conductive post 530d (with other conductive posts of the substrate assembly 500 not being visible in FIG. 8). As shown in FIG. 8, the DC- terminal 825 is coupled with the conductive post 540a, while the output terminal 835 is coupled with the conductive post 530d, such as discussed above with reference to FIG. 5. While not visible in FIG. 8, the conductive post 517c can be coupled with DC+ terminal 815a, the conductive post 517d can be coupled with the DC+ terminal 815b, and the conductive post 530c can be coupled with the output terminal 835. FIG. 9 illustrates a front-side, plan view of the power module 800 also with the molding compound 805 shown as transparent.

[0058] FIGs. 10A and 10B are diagrams illustrating, respectively, a perspective view and a side view of a high-side transistor conductive clip that can be included in the substrate assembly 500 of FIGs. 5-7 and/or the power module 800 of FIGs. 8 and 9, in accordance with example implementations. That is, FIGs. 10A and 10B illustrate the conductive clip 532 used in the substrate assembly 500 for connecting source terminals of the HS transistors 510 with the patterned metal layer 530a and the patterned metal layer 530b (for connection to an output terminal). FIG. 10A is a perspective view of the conductive clip 532, while FIG. 10B is a side view of the conductive clip 532.

[0059] As shown in FIG. 10B, the conductive clip 532 includes a contact surface 510a arranged in a plane P1, and a contact surface 510b arranged in a plane P2. In this

example, the plane P2 is parallel with, but non-coplanar with P1, which can account for height differences between the contact surfaces of the patterned metal layers of the DBM substrate 505 and the contact (upper) surfaces of the HS transistors 510. For instance, in this example, for a given HS transistor 510, the contact surface 510a can contact the HS transistors 510 (e.g., source terminals) and the contact surface 510b can contact a connection bus (e.g., patterned metal layer 530a or patterned metal layer 530b).

[0060] FIGs. 11A and 11B are diagrams illustrating, respectively, a perspective view and a side view of a low-side transistor conductive clip that can be included in the substrate assembly 500 of FIGs. 5-7 and/or the power module 800 of FIGs. 8 and 9, in accordance with an implementation. That is, FIGs. 11A and 11B illustrate the conductive clip 542 used in the substrate assembly 500 for connecting source terminals of the LS transistors 520 with the patterned metal layer 540 (for connection to a DC- terminal). FIG. 11A is a perspective view of the conductive clip 542, while FIG. 11B is a side view of the conductive clip 542.

[0061] As shown in FIG. 11B, the conductive clip 542 includes a contact surface 542a arranged in a plane P3, a contact surface 542b arranged in the plane P3 (coplanar with the contact surface 542a), and a contact surface 542c arranged in a plane P4. In this example, the plane P4 is parallel with, but non-coplanar with the plane P3, which can account for height differences between the contact surfaces of the patterned metal layers of the DBM substrate 505 and the contact (upper) surfaces of the LS transistors 520. For instance, in this example, for a given LS transistor 520 of the first plurality of LS transistors disposed on the patterned metal layer 530a and its corresponding LS transistor 520 disposed on the patterned metal layer 530b, the contact surfaces 542a and 542b can respectively contact the LS transistors 520 and the contact surface 542c can contact a connection bus (e.g., patterned metal layer 540).

[0062] FIG. 12 is a diagram illustrating a front-side view of another example substrate assembly 1200, in accordance with an implementation. The substrate assembly 1200, as with the substrate assembly 500 includes a substrate 1205 and a PCB 1207. The substrate 1205 includes similar aspects as the DBM substrate 505 of the substrate assembly 500, such as the interconnection of HS transistors, and the use of conductive posts for coupling DC+ terminals and an output terminal to the substrate assembly 1200. Also similar to the substrate assembly 500, in the substrate assembly 1200 wire bonds from the PCB 1207 can connect signal pins (e.g., press-fit pins) with a half-bridge circuit implemented on the substrate 1205.

[0063] The substrate assembly 1200 differs from the substrate assembly 500 in the interconnection of its LS transistors 1220. That is, in FIG. 12, the LS transistors 1220 are connected using an implementation of the approach of FIG. 2. That is conductive clips 1242 are included, where each conductive clips 1242 couples respective source terminals of four LS transistors 1220 (with equal conduction path lengths) to a patterned metal layer 1240, which can then be coupled with a DC- terminal (not shown in FIG. 12) via a conductive post 1241 that is disposed between the two conductive clips 1242. This arrangement of conductive post 1241 with respect to the conductive clips 1242 further balances the conduction current path lengths for the LS transistors 520 to the DC- terminal. In this example, a post 1240a (conductive or non-conductive) can provide mechanical stability for the associated DC-terminal, but be electrically isolated from the patterned metal layer 1240, as can be seen in FIG. 12.

[0064] FIGs. 13A and 13B are diagrams illustrating, respectively, a perspective view and a side view of a low-side transistor clip that can be included in the substrate assembly 1200 of FIG. 12. That is, FIGs. 13A and 13B illustrate the conductive clip 1242 used in the substrate assembly 1200 for connecting source terminals of the LS transistors 1220 with the patterned metal layer 1240 (for connection to a DC- terminal via the conductive post 1241). FIG. 13A is a perspective view of the conductive clip 1242, while FIG. 13B is a side view of the conductive clip 1242.

[0065] As shown in FIG. 13B, the conductive clip 1242 includes a contact surface 1242a arranged in a plane P5, a contact surface 1242b arranged in the plane P5 (coplanar with the contact surface 1242a), a contact surface 1242c arranged in the plane P5, a contact surface 1242d arranged in the plane P5, and a contact surface 1242e arranged in a plane P6. In this example, the plane P6 is parallel with, but non-coplanar with the plane P5, which can account for height differences between the contact surfaces of the patterned metal layers of the DBM substrate 1205 and the contact (upper) surfaces of the LS transistors 1220. For instance, in this example, for a group of four LS transistors 1220 (two on the left of patterned metal layer 1240 and a corresponding two on the right of patterned metal layer 1240), the contact surfaces 1242a-1242d respectively contact the LS transistors 1220 (e.g., source terminals) and the contact surface 1242e can contact a connection bus (e.g., patterned metal layer 1240).

[0066] FIG. 14 is a diagram illustrating a front-side view of a power module 1400 including the substrate assembly 1200 of FIG. 12, in accordance with an implementation. Similar to the power module 800 and the substrate assembly 500, the substrate assembly

1200 includes the substrate 1205 and the PCB 1207, implementing a half-bridge circuit. As shown in FIG. 14, the module 1400 includes a DC+ terminal 1415a, a DC+ terminal 1415b, and an output terminal 1435, which can be electrically coupled with the substrate assembly 1200 using corresponding conductive posts, such as described herein, e.g., with respect to the power module 800 and FIG. 8. As shown in FIG. 14, a DC- terminal 1425 can include an extension 1425a that electrically couples the DC- terminal 1425 with the conductive post 1241 of the substrate assembly 1200. Again, a post 1240a can provide mechanical support for the DC- terminal 1425.

[0067] FIG. 15 is a diagram illustrating a front-side view of another example substrate assembly 1500, in accordance with an implementation. The substrate assembly 1500, as with the substrate assembly 500 and the substrate assembly 1200 includes a substrate 1505 and a PCB 1507. The substrate 1505 includes similar aspects as the DBM substrate 505 of the substrate assembly 500 and the substrate 1205 of the substrate assembly 1200, such as the interconnection of HS transistors, and the use of conductive posts for coupling DC+ terminals and an output terminal to the substrate assembly 1500. The substrate assembly 1500 however, includes only four HS transistors (connected using clips 532), two on the left and two on the right. Also, the substrate assembly 1500 includes only four LS transistors 1520, two to the left of a patterned metal layer 1540 (for connection to a DC- terminal) and two to the right of the patterned metal layer 1540. Also similar to the substrate assembly 500 and the substrate assembly 1200, in the substrate assembly 1500, wire bonds from the PCB 1507 can connect signal pins (e.g., press-fit pins) with a half-bridge circuit implemented on the substrate 1505.

[0068] The substrate assembly 1500 also differs from the substrate assembly 500 and 1200 in, at least, a conductive clip 1542 used to connect source terminals of the four LS transistors 1520 to the patterned metal layer 1540. That is, in FIG. 15, all four of the LS transistors 1520 are connected to the patterned metal layer 1540 using the conductive clip 1542, where the conductive clip 1542 includes an opening 1543, in which a conductive post 1541 for connecting a DC- terminal is disposed in this example, as well as a post 1540a for mechanical support of the DC- terminal. The substrate assembly 1500 further includes a conductive post 1517c for connection of a first DC+ terminal to the substrate assembly 1500, and a conductive post 1517d for connection of a second DC+ terminal to the substrate assembly 1500. The substrate assembly 1500 also includes conductive posts 1530c and 1530d for connecting an output terminal with the substrate assembly 1500. FIG. 16 is a diagram illustrating a front-side perspective view of the substrate assembly 1500 of FIG. 15, which

illustrates the arrangement of the conductive posts and their relationship to other elements of the substrate assembly 1500.

[0069] FIGs. 17A and 17B are diagrams illustrating, respectively, a perspective view and a side view of a high-side transistor clip 1542 that can be included in the substrate assembly of FIGs. 15 and 16. As shown in FIGs. 17A and 17B, the conductive clip 1542 includes a contact surface 1542a arranged in a plane P7, a contact surface 1542b arranged in the plane P7 (coplanar with the contact surface 1542a), a contact surface 1542c arranged in the plane P7, a contact surface 1542d arranged in the plane P7, a contact surface 1542e arranged in a plane P8, and a contact surface 1542f arranged in the plane P8. In this example, the plane P8 is parallel with, but non-coplanar with the plane P7, which can account for height differences between the contact surfaces of the patterned metal layers of the DBM substrate 1505 and the contact (upper) surfaces of the LS transistors 1520. For instance, in this example, for the four LS transistors 1520, the contact surfaces 1542a-1542d respectively contact the LS transistors 1520 (e.g., source terminals) and the contact surfaces 1542e and 1542f can contact a connection bus (e.g., patterned metal layer 1240) on opposite sides of the opening 1543, as shown in FIGs. 12 and 13A.

[0070] FIG. 18 is a diagram illustrating a front-side view of another example substrate assembly 1800, in accordance with an implementation. The substrate assembly 1800, as with other substrate assemblies described herein, includes a substrate 1805 and a PCB 1807. The substrate 1805 includes similar aspects as the DBM substrate 505 of the substrate assembly 500, such as the interconnection of HS transistors 1810 using conductive clips 532 and connecting LS transistors 1820 using conductive clips 1842 that are similar to the conductive clips 542 of the substrate assembly 500.

[0071] The substrate assembly 1800 includes six HS transistors, three on the left and three on the right. Also, the substrate assembly 1800 includes six LS transistors 1820, three to the left of a patterned metal layer 1840 (for connection to a DC- terminal) and three to the right of the patterned metal layer 1840. Similar to the substrate assembly 500, the substrate assembly 1200 and the substrate assembly 1500, in the substrate assembly 1800, wire bonds from the PCB 1807 can connect signal pins (e.g., press-fit pins) with a half-bridge circuit implemented on the substrate 1805.

[0072] In the substrate assembly 1800, a DC- terminal (not shown in FIG. 18) can be coupled with the patterned metal layer 1840 via a conductive post 1841a that is disposed between the top conductive clip 1842 and the middle conductive clip 1842, as well as a conductive post 1841b that is disposed between the middle conductive clip 1842 and the

bottom conductive clip 1842. In the example of FIG. 18, as the conductive post 1841b can be closer to an associated DC- terminal, the conductive post 1841b can have a smaller size than the conductive post 1841a, e.g., to facilitate current sharing balance and stray inductance balance and/or reduction. That is, this arrangement of conductive posts 1841a and 1841b with respect to the conductive clips 1842 further balances the conduction current path lengths for the LS transistors 1820 to the associated DC- terminal. In this example, a post 1840a (conductive or non-conductive) can provide mechanical stability for the associated DC- terminal, but be electrically isolated from the patterned metal layer 1840.

[0073] FIG. 19 is a diagram illustrating a front-side view of a power module 1900 including the substrate assembly 1800 of FIG. 18, in accordance with an implementation. Similar to the substrate assemblies 500, 1200 and 1500, the substrate assembly 1800 includes the substrate 1805 and the PCB 1807, and implements a half-bridge circuit. As shown in FIG. 19, the module 1900 includes a DC+ terminal 1915a, a DC+ terminal 1915b, and an output terminal 1935, which can be electrically coupled with the substrate assembly 1800 using corresponding conductive posts, such as described herein, e.g., with respect to the power module 800 and FIG. 8. As shown in FIG. 19, a DC- terminal 1925 can include an extension 1925a that electrically couples the DC- terminal 1925 with the conductive posts 1841a and 1841b of the substrate assembly 1800. Again, a post 1840a can provide mechanical support for the DC- terminal 1925.

[0074] FIG. 20 is a flowchart illustrating a method 2000 for producing a power module, such as the power modules described herein, in accordance with an implementation. At block 2005, the method 2000 includes performing a sintering operation to couple semiconductor die (e.g., HS and LS transistors) with a substrate, such as DBM substrate. At block 2010, the method 2000 includes performing a soldering operation to attach conductive clips and, in some implementations, a negative temperature coefficient (NTC) thermal sensor and a second substrate, such as a PCB to the (DBM) substrate. At block 2015, the method 2000 includes a flux cleaning to remove solder flux from the operation of block 2010. At block 2020, wire bonding is performed, e.g., to connect a PCB with the conductive clips and semiconductor die, such as described herein. At block 2025, the method 2000 includes soldering leadframe components (e.g., DC+, DC- and output terminals) and copper holders for press-fit pins. At block 2030, the method 2000 includes another flux cleaning operation. At block 2035, a plasma cleaning and plating of the terminals is performed. At blocks 2040, 2045, 2050 and 2055, the method 2000 includes, respectively molding (encapsulation) and curing of the module, deflashing to remove excess molding compound, trimming and forming

terminals, and insertion of press-fit pins. At block 2060, the module is electrically tested for proper functionality.

[0075] As described herein, turn-on switching events of either a low-side transistor or a high-side transistor, for example metal-oxide field-effect transistors (MOSFETs) in a half-bridge module, can produce high-frequency oscillations that appear between gate-to-source potentials of the ideal switch. These high frequency oscillations, originating within the half-bridge module, can be transmitted to an external gate-driver sub-system, which can lead to system level failures and/or can increase overall electromagnetic interference (EMI), for example, increases in conducted and radiated emissions in an associated system.

[0076] Such high frequency oscillations can be directly related to switching transients, such as respective derivatives of drain-to-source current (dI_{DS}/dt) and/or drain-to-source voltage (dV_{DS}/dt), in combination with parasitic impedances of the half-bridge, for example, resistance (R), inductance (L), and/or capacitance (C). The interaction of switching transients and parasitic impedances of gate-source loops for parallel-connected MOSFET semiconductor die can produce such high frequency oscillations.

[0077] For instance, one phenomenon that can significantly contribute to such oscillations is to body diode oscillation associated with reverse recovery currents between parallel SiC MOSFET die. For instance, such parallel-connected MOSFETs can attain peak reverse recovery current (I_{RR}) at a phase lag, which is dictated by differences in their respective body diode forward voltages (V_{AK}), and can arise as a consequence of imbalance in the parasitic path inductances between individual die, for example, source terminal to phase /AC terminal for high-side transistors, and individual die source terminal to DC-/N terminal for low-side transistors. Because of the increased switch speed of silicon carbide (SiC) MOSFETs, such as compared to silicon MOSFETs, switching transients can also increase, which can result in increased switching oscillation.

[0078] FIG. 21 is a diagram illustrating a front-side view of another example substrate assembly 2100, in accordance with an implementation. The substrate assembly 2100 can further reduce the effects of switching transients by improving current sharing between parallel-connected high-side transistors of a half-bridge circuit module. That is, in this example, power tabs, e.g., DC+ power tabs or DC+ terminals are connected to drains of the high-side transistors of the substrate assembly 2100 similar to the DC-terminal connections to the source terminals of the low-side transistors of the power module 1900 (and the low-side transistors of the substrate assembly 2100).

[0079] FIG. 21 is a diagram illustrating a front-side view of another example substrate assembly 2100, in accordance with an implementation. The substrate assembly 2100, as with other substrate assemblies described herein, includes a substrate 2105 and a PCB 2107. The substrate 2105 includes similar aspects as the DBM substrate 505 of the substrate assembly 500, such as the interconnection of HS transistors 2110 using conductive clips (such as conductive clips 532) and connecting LS transistors of the substrate assembly 2100 (not referenced in FIG. 21) using conductive clips that are similar to the conductive clips 542 of the substrate assembly 500.

[0080] The substrate assembly 2100, as with the substrate assembly 1800, includes six HS transistors, three in a column on the left and three in a column on the right. Also, the substrate assembly 2100 includes six LS transistors, in two columns of three that are disposed between the left and right columns of HS transistors. Similar to the substrate assembly 500, the substrate assembly 1200, the substrate assembly 1500, and the substrate assembly 1800, in the substrate assembly 2100, wire bonds 2120 from the PCB 2107 can connect signal pins (e.g., press-fit pins) with a half-bridge circuit implemented on the substrate 2105.

[0081] In the substrate assembly 2100, a DC- terminal (not shown in FIG. 21) can be coupled with a patterned metal layer via a conductive post 2141a that is disposed between a top conductive clip and a middle conductive clip, as well as a conductive post 2141b that is disposed between the middle conductive clip and a bottom conductive clip. In the example of FIG. 21, as with the example of FIG. 18, as the conductive post 2141b can be closer to an associated DC- terminal, the conductive post 2141b can have a smaller size than the conductive post 2141a, e.g., to facilitate current sharing balance and stray inductance balance and/or reduction. That is, this arrangement of conductive posts 2141a and 2141b with respect to the corresponding conductive clips further balances the conduction current path lengths for the LS transistors to the associated DC- terminal. In this example, a post 2140 (conductive or non-conductive) can provide mechanical stability for the associated DC- terminal, but be electrically isolated from the patterned metal layer on which the conductive post 2141a and the conductive post 2141b are disposed.

[0082] Further in the substrate assembly 2100, a first DC+ terminal (not shown in FIG. 21) can be coupled with a patterned metal layer via a conductive post 2118a that is disposed between a top HS transistor and a middle HS transistor in the left column of HS transistors in FIG. 21, as well as a conductive post 2118b that is disposed between the middle HS transistors and a bottom HS transistor in the left column. This arrangement of conductive posts 2118a and 2118b with respect to the corresponding HS transistors further balances the

conduction current path lengths for the HS transistors to the associated DC+ terminal. In this example, a post 2117a (conductive or non-conductive) can provide mechanical stability for the associated DC+ terminal, but be electrically isolated from the patterned metal layer on which the conductive post 2118a and the conductive post 2118b are disposed.

[0083] Further in the substrate assembly 2100, similar to the left column of HS transistors, a second DC+ terminal (not shown in FIG. 21) can be coupled with a patterned metal layer via a conductive post 2119a that is disposed between a top HS transistor and a middle HS transistor in the right column of HS transistors in FIG. 21, as well as a conductive post 2119b that is disposed between the middle HS transistors and a bottom HS transistor in the right column. This arrangement of conductive posts 2119a and 2119b with respect to the corresponding HS transistors further balances the conduction current path lengths for the HS transistors to the associated DC+ terminal. In this example, a post 2117b (conductive or non-conductive) can provide mechanical stability for the associated DC+ terminal, but be electrically isolated from the patterned metal layer on which the conductive post 2119a and the conductive post 2119b are disposed.

[0084] FIG. 22 is a diagram illustrating a front-side view of a power module 2200 including the substrate assembly 2100 of FIG. 21, in accordance with an implementation. The power module 2200 includes the substrate 2105 and the PCB 2107, and implements a half-bridge circuit. As shown in FIG. 22, the module 2200 includes a DC+ terminal 2215a, a DC+ terminal 2215b, and an output terminal 2235, which can be electrically coupled with the substrate assembly 2100 using corresponding conductive posts, such as described herein. For instance, in this example, the DC+ terminal 2215a is electrically coupled with the substrate 2105, for example, via the conductive post 2118a and the conductive post 2118b of FIG. 21, while the DC+ terminal 2215b is electrically coupled with the substrate 2105, for example, via the conductive post 2119a and the conductive post 2119b of FIG. 21. Further in this example, the DC- terminal 2225 is electrically coupled with the substrate 2105, for instance, via the conductive posts 2141a and 2141b of the substrate assembly 2100. Again, posts 2140, 2117a and 2117b can provide mechanical support, respectively, for the DC- terminal 2225, the DC+ terminal 2215a, and the DC- terminal 2215b.

[0085] In some implementations, using a same material for power terminals, output terminals and associated conductive posts can result in shear strengths for mechanical and electrical bonds between the posts and terminals that do not meet desired mechanical strength properties. In some implementations, such bonds can be welded bonds, for example, ultrasonic welded bonds. FIG. 23 is a diagram illustrating an example leadframe assembly

2300 including power and output terminals that are made from a first material, and also includes a plurality of conductive posts that are made from a second, different material. In an example implementation, the leadframe assembly 2300 can be included in the power module 2200 of FIG. 22. However, it is noted that similar arrangements can be implemented in other power modules, such as those described herein. For purposes of discussion, and by way of example, the elements of the leadframe assembly 2300 are referenced using the same reference numbers used in FIGs. 21 and 22.

[0086] As shown in FIG. 23, the leadframe assembly 2300 includes the DC+ terminal 2215a, the DC+ terminal 2215b, the DC- DC- terminal 2225 and the output terminal 2235, which, in this example can be made of a metal material. In some implementations, the metal material can be pure copper, for example, copper that is greater than or equal to 99.99 % pure. In contrast, the conductive post 2118a, 2118b, 2119a, 2119b, 2141a and 2141b, as well as conductive posts coupled with the output terminal 2235, can be made of an alloy of the metal material from which the power terminals and output terminal are made. For instance, the conductive posts can be an alloy of copper, where the alloy includes at least one of iron or phosphorus. In some implementation, such a copper alloy can have an iron content of 0.20 percent or less, and/or a phosphorous content of 0.05 percent or less. In some implementations, other metals and/or alloys can be used. For instance, an alloy can include elements that are chemically and physically similar to copper, iron /and or phosphorus.

[0087] Shear strength values can also be affected by conductive post size, for example, an area of a conductive post that is coupled with an associated power terminal. That is, smaller post contact area can correspond with lower shear strength. As smaller posts allow for reduction of material costs and/or reduction substrate area, such size reductions are desirable. One approach for reducing post size is to bevel or chamfer the corners of the posts, such as shown for the posts in FIG. 23. Such beveled corners can facilitate improvements in median shear strength, though can increase shear strength variability.

[0088] FIG. 24 is a graph 2400 illustrating a comparison of shear strengths for various posts and associated terminals. For instance, a data group 2401 illustrates shear strength for posts of pure copper that are ultrasonically welded to pure copper terminals, a data group 2402 illustrates shear strength for posts of pure copper with beveled corners that are ultrasonically welded to pure copper terminals (output and power terminals), and a data group 2403 illustrates shear strength for posts of a copper alloy with beveled corners that are ultrasonically welded to pure copper terminals. Normalized shear strength values for the data groups 2401, 2402 and 2403 are shown in the y-axis of the graph 2400. As can be seen FIG.

24, the data group 2402 shows a nominal increase in median shear strength (approximately 10 percent), while the data group 2403 shows an improvement in median shear strength of more than 400 percent.

[0089] In a general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate, a second patterned metal layer disposed on the surface of the substrate, and a third patterned metal layer disposed on the surface of the substrate. The module also includes a first high-side transistor disposed on the first patterned metal layer, a second high-side transistor disposed on the first patterned metal layer, a first conductive clip electrically coupling the first high-side transistor with the second patterned metal layer, and a second conductive clip electrically coupling the second high-side transistor with the second patterned metal layer. The module further includes a first low-side transistor disposed on the second patterned metal layer, a second low-side transistor disposed on the second patterned metal layer, a third conductive clip electrically coupling the first low-side transistor with the third patterned metal layer, and a fourth conductive clip electrically coupling the second low-side transistor with the third patterned metal layer.

[0090] Implementations can include one or more of the following aspects, alone or in combination. For example, the first patterned metal layer can be electrically coupled with a DC+ terminal of the half-bridge circuit power module. The second patterned metal layer can be electrically coupled with an output terminal of the half-bridge circuit power module. The third patterned metal layer can be electrically coupled with a DC- terminal of the half-bridge circuit power module.

[0091] The first conductive clip can electrically couple a source terminal of the first high-side transistor with the output terminal. The second conductive clip can electrically couple a source terminal of the second high-side transistor with the output terminal. The third conductive clip can electrically couple a source terminal of the first low-side transistor with the DC- terminal. The fourth conductive clip can electrically couple a source terminal of the second low-side transistor with the DC- terminal.

[0092] The DC+ terminal can be a first DC+ terminal. The substrate can include a fourth patterned metal layer disposed on the surface of the substrate. The fourth patterned metal layer can be electrically coupled with a second DC+ terminal. The half-bridge circuit power module can include a third high-side transistor having a drain terminal disposed on the fourth patterned metal layer, a fourth high-side transistor having a drain terminal disposed on the fourth patterned metal layer, a fifth conductive clip electrically coupling a source terminal

of the third high-side transistor with the output terminal; and a sixth conductive clip electrically coupling the fourth high-side transistor with the output terminal.

[0093] The first DC+ terminal can be electrically coupled with the first patterned metal layer via a first conductive post; and the second DC+ terminal is electrically coupled with the fourth patterned metal layer via a second conductive post.

[0094] The third conductive clip can electrically couple the source terminal of the third high-side transistor with the output terminal via a fifth patterned metal layer disposed on the surface of the substrate.

[0095] The output terminal can be electrically coupled with the second patterned metal layer via a first conductive post, and electrically coupled with the fourth patterned metal layer via a second conductive post.

[0096] The substrate can include a fourth patterned metal layer electrically coupled with the output terminal. The half-bridge circuit power module can include a third low-side transistor disposed on the fourth patterned metal layer, and a fourth low-side transistor disposed on the fourth patterned metal layer. The third conductive clip can electrically couple the third low-side transistor to the third patterned metal layer. The fourth conductive clip can electrically couple the fourth low-side transistor to the third patterned metal layer.

[0097] The DC- terminal can be electrically coupled to the third patterned metal layer via a conductive post. The conductive post can be disposed between the third conductive clip and the fourth conductive clip.

[0098] The half-bridge circuit power module can include a fifth low-side transistor disposed on the first patterned metal layer, a sixth low-side transistor disposed on the fourth patterned metal layer, a seventh low-side transistor disposed on the first patterned metal layer; and an eighth low-side transistor disposed on the fourth patterned metal layer. The third conductive clip can further electrically couple the fifth low-side transistor and the sixth low-side transistor to the third patterned metal layer. The fourth conductive clip further electrically couple the sixth low-side transistor and the seventh low-side transistor to the third patterned metal layer.

[0099] Respective drain terminals of the first high-side transistor and the second high-side transistor can be disposed on and electrically coupled with the first patterned metal layer. Respective drain terminals of the first low-side transistor and the second low-side transistor can be disposed on and electrically coupled with the second patterned metal layer.

[00100] In another general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate and

electrically coupled with an output terminal, a second patterned metal layer disposed on the surface of the substrate and electrically coupled with a DC- terminal, a third patterned metal layer disposed on the surface of the substrate and electrically coupled with the output terminal. The module further includes a first low-side transistor disposed on the first patterned metal layer, a second low-side transistor disposed on the first patterned metal layer, a third low-side transistor disposed on the third patterned metal layer, and a fourth low-side transistor disposed on the third patterned metal layer. The module also includes a conductive clip electrically coupling the first low-side transistor, the second low-side transistor, the third low-side transistor and the fourth low-side transistor with the second patterned metal layer.

[00101] Implementations can include one or more of the following features, alone or in combination. For example, the conductive clip can include an opening through which the second patterned metal layer is exposed. The DC- terminal can be electrically coupled with the second patterned metal layer via a conductive post disposed within the opening of the conductive clip.

[00102] The output terminal can be coupled with the first patterned metal layer via a first conductive post. The output terminal can be coupled with the third patterned metal layer via a second conductive post.

[00103] The substrate can include a fourth patterned metal layer disposed on the surface of the substrate, and a fifth patterned metal layer disposed on the surface of the substrate. The can include a first high-side transistor disposed on the fourth patterned metal layer; a second high-side transistor disposed on the fourth patterned metal layer; a third high-side transistor disposed on the fifth patterned metal layer, and a fourth high-side transistor disposed on the fifth patterned metal layer. The module can include a second conductive clip electrically coupling the first high-side transistor with the first patterned metal layer, a third conductive clip electrically coupling the second high-side transistor with the first patterned metal layer, a fourth conductive clip electrically coupling the third high-side transistor with the third patterned metal layer, and a fifth conductive clip electrically coupling the fourth high-side transistor with the third patterned metal layer.

[00104] The fourth patterned metal layer can be electrically coupled with a first DC+ terminal via a first conductive post. The fifth patterned metal layer can be electrically coupled with a second DC+ terminal via a second conductive post.

[00105] In another general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate and electrically coupled with an output terminal, a second patterned metal layer disposed on the

surface of the substrate and electrically coupled with a DC- terminal, and a third patterned metal layer disposed on the surface of the substrate and electrically coupled with the output terminal. The module also includes a first low-side transistor disposed on the first patterned metal layer, a second low-side transistor disposed on the first patterned metal layer, a third low-side transistor disposed on the first patterned metal layer, a fourth low-side transistor disposed on the third patterned metal layer, a fifth low-side transistor disposed on the third patterned metal layer, and a sixth low-side transistor disposed on the third patterned metal layer. The module further includes a first conductive clip electrically coupling the first low-side transistor and the fourth low-side transistor to the second patterned metal layer, a second conductive clip electrically coupling the second low-side transistor and the fifth low-side transistor to the second patterned metal layer, and a third conductive clip electrically coupling the third low-side transistor and the sixth low-side transistor to the second patterned metal layer.

[00106] Implementations can include one or more of the following aspects, alone or in combination. For example, the second patterned metal layer can be electrically coupled with a DC- terminal.

[00107] The DC- terminal can be electrically coupled with the second patterned metal layer via a first conductive post and disposed on the second patterned metal layer between the first conductive clip and the second conductive clip, and a second conductive post disposed on the second patterned metal layer between third second conductive clip and the third conductive clip. The second conductive clip can be closer to the DC- terminal than the first conductive clip. The third conductive clip can be closer to the DC- terminal than the second conductive clip.

[00108] A surface of the second conductive post coupled with the second patterned metal layer can have an area that is smaller than an area of a surface of the first conductive post coupled with the second patterned metal layer.

[00109] In another general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate, a second patterned metal layer disposed on the surface of the substrate; and a third patterned metal layer disposed on the surface of the substrate. The module further includes a first high-side transistor disposed on the first patterned metal layer, a second high-side transistor disposed on the first patterned metal layer; a first conductive clip electrically coupling the first high-side transistor with the second patterned metal layer, and a second conductive clip electrically coupling the second high-side transistor with the second patterned metal layer. The module

also includes a first low-side transistor disposed on the second patterned metal layer, a second low-side transistor disposed on the second patterned metal layer, a third conductive clip electrically coupling the first low-side transistor with the third patterned metal layer, and a fourth conductive clip electrically coupling the second low-side transistor with the third patterned metal layer. The module still further includes a DC+ terminal that is electrically coupled with the first patterned metal layer via a first conductive post disposed between the first high-side transistor and the second high-side transistor on the first patterned metal layer. The module also includes a DC- terminal that is electrically coupled with the third patterned metal layer via a second conductive post disposed between the third conductive clip and the fourth conductive clip on the third patterned metal layer.

[00110] Implementations can include one or more of the following features, alone or in combination. For example, the second patterned metal layer can be electrically coupled with an output terminal of the half-bridge circuit power module via a third conductive post.

[00111] The first conductive clip can electrically couple a source terminal of the first high-side transistor with the output terminal. The second conductive clip can electrically couple a source terminal of the second high-side transistor with the output terminal. The third conductive clip can electrically couple a source terminal of the first low-side transistor with the DC- terminal. The fourth conductive clip can electrically couple a source terminal of the second low-side transistor with the DC- terminal.

[00112] The DC+ terminal, the DC- terminal and the output terminal can include a first conductive material. The first conductive post, the second conductive post, and the third conductive post can include a second conductive material different from the first conductive material. The first conductive material can be a metal, and the second conductive material can be an alloy of the metal. The first conductive material can be pure copper; and the second conductive material can be an alloy of copper including at least one of iron, or phosphorus.

[00113] The DC+ terminal can be a first DC+ terminal. The substrate can include a fourth patterned metal layer disposed on the surface of the substrate, and a fifth patterned metal layer disposed on the surface of the substrate. The module can include a third high-side transistor having a drain terminal disposed on the fourth patterned metal layer, a fourth high-side transistor having a drain terminal disposed on the fourth patterned metal layer, a fifth conductive clip electrically coupling a source terminal of the third high-side transistor with the fifth patterned metal layer, and a sixth conductive clip electrically coupling the fourth high-side transistor with the fifth patterned metal layer. The module can include a second DC+ terminal that is electrically coupled with the fourth patterned metal layer via a third

conductive post disposed between the third high-side transistor and the fourth high-side transistor.

[00114] The module can include an output terminal that is electrically coupled with the second patterned metal layer via a fourth conductive post, and electrically coupled with the fifth patterned metal layer via a fifth conductive post.

[00115] The substrate can include a fourth patterned metal layer disposed on the surface of the substrate. The module can include a third low-side transistor disposed on the fourth patterned metal layer, and a fourth low-side transistor disposed on the fourth patterned metal layer. The third conductive clip can electrically couple the third low-side transistor to the third patterned metal layer. The fourth conductive clip can electrically couple the fourth low-side transistor to the third patterned metal layer.

[00116] The module can include a fifth low-side transistor disposed on the second patterned metal layer, a sixth low-side transistor disposed on the fourth patterned metal layer, and a fifth conductive clip electrically coupling the fifth low-side transistor and the sixth low-side transistor with the third patterned metal layer. The DC- terminal can be electrically coupled with the third patterned metal layer via a third conductive post disposed between the fourth conductive clip and the fifth conductive clip on the third patterned metal layer.

[00117] The DC+ terminal can be a first DC+ terminal. The substrate can include a fifth patterned metal layer disposed on the surface of the substrate. The module further can include a third high-side transistor disposed on the first patterned metal layer, a sixth conductive clip electrically coupling the third high-side transistor with the second patterned metal layer, a fourth high-side transistor disposed on the fifth patterned metal layer, a seventh conductive clip electrically coupling the fourth high-side transistor with the fourth patterned metal layer, a fifth high-side transistor disposed on the fifth patterned metal layer, an eighth conductive clip electrically coupling the fifth high-side transistor with the fourth patterned metal layer, a sixth high-side transistor disposed on the fifth patterned metal layer, and a ninth conductive clip electrically coupling the sixth high-side transistor with the fourth patterned metal layer. The module can include a second DC+ terminal that is electrically coupled with fifth patterned metal layer via a third conductive post disposed between the fourth high-side transistor and the fifth high-side transistor on the fifth patterned metal layer; and a fourth conductive post disposed between the fifth high-side transistor and the sixth high-side transistor on the fifth patterned metal layer. The first DC+ terminal can be electrically coupled with the first patterned metal layer via fifth conductive post disposed between the second high-side transistor and the third high-side transistor on the first patterned metal layer.

[00118] Respective drain terminals of the first high-side transistor and the second high-side transistor can be disposed on and electrically coupled with the first patterned metal layer. Respective drain terminals of the first low-side transistor and the second low-side transistor can be disposed on and electrically coupled with the second patterned metal layer.

[00119] In another general aspect, a half-bridge circuit power module includes a substrate having a first patterned metal layer disposed on a surface of the substrate, a second patterned metal layer disposed on the surface of the substrate, a third patterned metal layer disposed on the surface of the substrate, a fourth patterned metal layer disposed on the surface of the substrate, and a fifth patterned metal layer disposed on the surface of the substrate. The module further includes a first low-side transistor disposed on the first patterned metal layer and electrically coupled with the fifth patterned metal layer via a first conductive clip, a second low-side transistor disposed on the first patterned metal layer and electrically coupled with the fifth patterned metal layer via a second conductive clip, a third low-side transistor disposed on the second patterned metal layer and electrically coupled with the fifth patterned metal layer via the first conductive clip, and a fourth low-side transistor disposed on the second patterned metal layer and electrically coupled with the fifth patterned metal layer via the second conductive clip. The module further includes a first high-side transistor disposed on the third patterned metal layer and electrically coupled with the first patterned metal layer via a third conductive clip, a second high-side transistor disposed on the third patterned metal layer and electrically coupled with the first patterned metal layer via a fourth conductive clip, a third high-side transistor disposed on the fourth patterned metal layer and electrically coupled with the second patterned metal layer via a fifth conductive clip, and a fourth high-side transistor disposed on the fourth patterned metal layer and electrically coupled with the second patterned metal layer via a sixth conductive clip. The module also includes a first DC+ terminal electrically coupled with the third patterned metal layer via a first conductive post disposed between the first high-side transistor and the second high-side transistor on the third patterned metal layer, and a second DC+ terminal electrically coupled with the fourth patterned metal layer via a second conductive post disposed between the third high-side transistor and the fourth high-side transistor on the fourth patterned metal layer. The module further includes a DC- terminal electrically coupled with the fifth patterned metal layer via a third conductive post disposed between the first conductive clip and the second conductive clip on the fifth patterned metal layer.

[00120] Implementations can include one or more of the following features or aspects, alone or in combination. For instance, the module can include an output terminal that is

coupled with the first patterned metal layer via a fourth conductive post, and coupled with the second patterned metal layer via a fifth conductive post.

[00121] The first DC+ terminal, the second DC+ terminal and the output terminal can include pure copper. The first conductive post, the second conductive post, the third conductive post, the fourth conductive post, and the fifth conductive post can include an alloy of copper. The alloy of copper can include at least one of iron or phosphorus.

[00122] The module can include a fifth low-side transistor disposed on the first patterned metal layer and electrically coupled with the fifth patterned metal layer via a seventh conductive clip, and a sixth low-side transistor disposed on the second patterned metal layer and electrically coupled with the fifth patterned metal layer via the seventh conductive clip. The module can include a fifth high-side transistor disposed on the third patterned metal layer and electrically coupled with the first patterned metal layer via an eighth conductive clip, and a sixth high-side transistor disposed on the fourth patterned metal layer and electrically coupled with the second patterned metal layer via a sixth conductive clip. The first DC+ terminal can be electrically coupled with the third patterned metal layer via a fourth conductive post disposed between the second high-side transistor and the fifth high-side transistor on the third patterned metal layer. The second DC+ terminal can be electrically coupled with the fourth patterned metal layer via a fifth conductive post disposed between the fourth high-side transistor and the sixth high-side transistor on the fourth patterned metal layer. The DC- terminal can be electrically coupled with the fifth patterned metal layer via a sixth conductive post disposed between the second conductive clip and the third conductive clip on the fifth patterned metal layer.

[00123] In another general aspect, a method for producing a half-bridge circuit power module includes coupling a first high-side transistor with a first patterned metal layer disposed on a surface of a substrate, and coupling a second high-side transistor with the first patterned metal layer. The method also includes coupling a first low-side transistor with a second patterned metal layer disposed on the surface of the substrate, and coupling a second low-side transistor with the second patterned metal layer. The method further includes, with a first conductive clip, electrically coupling the first high-side transistor with the second patterned metal layer. The method also includes, with a second conductive clip, electrically coupling the second high-side transistor with the second patterned metal layer. The method also further includes, with a third conductive clip, electrically coupling the first low-side transistor with a third patterned metal layer disposed on the surface of the substrate, and with a fourth conductive clip, electrically coupling the second low-side transistor with the third

patterned metal layer. The method also includes electrically coupling a DC+ terminal with the first patterned metal layer via a first conductive post disposed between the first high-side transistor and the second high-side transistor on the first patterned metal layer, and electrically coupling a DC- terminal with the third patterned metal layer via a second conductive post disposed between the third conductive clip and the fourth conductive clip on the third patterned metal layer.

[00124] Implementations can include one or more of the following feature or aspects. For example, the method can include electrically coupling an output terminal with the second patterned metal layer via a third conductive post.

[00125] The DC+ terminal can be a first DC+ terminal, and the method can include coupling a third high-side transistor with a fourth patterned metal layer disposed on the surface of the substrate, coupling a fourth high-side transistor with the fourth patterned metal layer, coupling a third low-side transistor with a fifth patterned metal layer on the surface of the substrate, and coupling a fourth low-side transistor with the fifth patterned metal layer. The method can include, with a fifth conductive clip, electrically coupling the third high-side transistor with the fifth patterned metal layer and, with a sixth conductive clip, electrically coupling the fourth high-side transistor with the fifth patterned metal layer. The method can include electrically coupling a second DC+ terminal with the fourth patterned metal layer via a fourth conductive post disposed between the third high-side transistor and the fourth high-side transistor on the fourth patterned metal layer, and electrically coupling the output terminal with the fifth patterned metal layer via fifth conductive post. The third conductive clip can electrically couple the third low-side transistor with the third patterned metal layer. The fourth conductive clip can electrically couple the fourth low-side transistor with the third patterned metal layer.

[00126] It will be understood that, in the foregoing description, when an element, such as a layer, a region, or a substrate, is referred to as being on, connected to, electrically connected to, coupled to, or electrically coupled to another element, it may be directly on, connected or coupled to the other element, or one or more intervening elements may be present. In contrast, when an element is referred to as being directly on, directly connected to or directly coupled to another element or layer, there are no intervening elements or layers present. Although the terms directly on, directly connected to, or directly coupled to may not be used throughout the detailed description, elements that are shown as being directly on, directly connected or directly coupled can be referred to as such. The claims of the

application may be amended to recite exemplary relationships described in the specification or shown in the figures.

[00127] As used in this specification, a singular form may, unless definitely indicating a particular case in terms of the context, include a plural form. Spatially relative terms (e.g., over, above, upper, under, beneath, below, lower, top, bottom, and so forth) are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. In some implementations, the relative terms above and below can, respectively, include vertically above and vertically below. In some implementations, the term adjacent can include laterally adjacent to or horizontally adjacent to.

[00128] Some implementations may be implemented using various semiconductor processing and/or packaging techniques. Some implementations may be implemented using various types of semiconductor device processing techniques associated with semiconductor substrates including, but not limited to, for example, silicon (Si), silicon carbide (SiC), gallium arsenide (GaAs), gallium nitride (GaN), and/or so forth.

[00129] While certain features of the described implementations have been illustrated as described herein, many modifications, substitutions, changes and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the scope of the implementations. It should be understood that they have been presented by way of example only, not limitation, and various changes in form and details may be made. Any portion of the apparatus and/or methods described herein may be combined in any combination, except mutually exclusive combinations. The implementations described herein can include various combinations and/or sub-combinations of the functions, components and/or features of the different implementations described.

CLAIMS

What is claimed is:

1. A half-bridge circuit power module (800) comprising:
a substrate (505) including:
a first patterned metal layer (517a) disposed on a surface of the substrate;
a second patterned metal layer (530a) disposed on the surface of the substrate;
and
a third patterned metal layer (540) disposed on the surface of the substrate;
a first high-side transistor (510) disposed on the first patterned metal layer;
a second high-side transistor (510) disposed on the first patterned metal layer;
a first conductive clip (532) electrically coupling the first high-side transistor with the second patterned metal layer;
a second conductive clip (532) electrically coupling the second high-side transistor with the second patterned metal layer;
a first low-side transistor (520) disposed on the second patterned metal layer;
a second low-side transistor (520) disposed on the second patterned metal layer;
a third conductive clip (542) electrically coupling the first low-side transistor with the third patterned metal layer; and
a fourth conductive clip (542) electrically coupling the second low-side transistor with the third patterned metal layer.
2. The half-bridge circuit power module of claim 1, wherein:
the first patterned metal layer is electrically coupled with a DC+ terminal (815a) of the half-bridge circuit power module;
the second patterned metal layer is electrically coupled with an output terminal (835) of the half-bridge circuit power module;
the third patterned metal layer is electrically coupled with a DC- terminal (825) of the half-bridge circuit power module.
3. The half-bridge circuit power module of claim 2, wherein:
the first conductive clip electrically couples a source terminal of the first high-side transistor with the output terminal;

the second conductive clip electrically couples a source terminal of the second high-side transistor with the output terminal;

the third conductive clip electrically couples a source terminal of the first low-side transistor with the DC- terminal; and

the fourth conductive clip electrically couples a source terminal of the second low-side transistor with the DC- terminal.

4. The half-bridge circuit power module of claim 2, wherein:

the DC+ terminal is a first DC+ terminal; and

the substrate further includes a fourth patterned metal layer (517b) disposed on the surface of the substrate, the fourth patterned metal layer being electrically coupled with a second DC+ terminal (815b),

the half-bridge circuit power module further comprising:

a third high-side transistor (510) having a drain terminal disposed on the fourth patterned metal layer;

a fourth high-side transistor (510) having a drain terminal disposed on the fourth patterned metal layer;

a fifth conductive clip (532) electrically coupling a source terminal of the third high-side transistor with the output terminal; and

a sixth conductive clip (532) electrically coupling the fourth high-side transistor with the output terminal.

5. The half-bridge circuit power module of claim 4, wherein:

the first DC+ terminal is electrically coupled with the first patterned metal layer via a first conductive post (517c); and

the second DC+ terminal is electrically coupled with the fourth patterned metal layer via a second conductive post (517d).

6. The half-bridge circuit power module of claim 4, wherein:

the fifth conductive clip (532) electrically couples a source terminal of the third high-side transistor with the output terminal via a fifth patterned metal layer (530b) disposed on the surface of the substrate.

7. The half-bridge circuit power module of claim 5, wherein the output terminal is:

electrically coupled with the second patterned metal layer via a first conductive post (530c); and

electrically coupled with the fifth patterned metal layer via a second conductive post (530d).

8. The half-bridge circuit power module of claim 2, wherein the substrate further includes a fourth patterned metal layer (530b) electrically coupled with the output terminal, the half-bridge circuit power module further comprising:

a third low-side transistor (520) disposed on the fourth patterned metal layer;

and

a fourth low-side transistor (520) disposed on the fourth patterned metal layer, the third conductive clip further electrically coupling the third low-side transistor to the third patterned metal layer, and

the fourth conductive clip further electrically coupling the fourth low-side transistor to the third patterned metal layer.

9. The half-bridge circuit power module of claim 8, where the DC- terminal is electrically coupled to the third patterned metal layer via a conductive post (1841a), the conductive post being disposed between the third conductive clip and the fourth conductive clip.

10. The half-bridge circuit power module of claim 8, further comprising:

a fifth low-side transistor (1220) disposed on the first patterned metal layer;

a sixth low-side transistor (1220) disposed on the fourth patterned metal layer;

a seventh low-side transistor (1220) disposed on the first patterned metal layer; and

an eighth low-side transistor (1220) disposed on the fourth patterned metal layer;

the third conductive clip (1242) further electrically coupling the fifth low-side transistor and the sixth low-side transistor to the third patterned metal layer, and

the fourth conductive clip (1242) further electrically coupling the sixth low-side transistor and the seventh low-side transistor to the third patterned metal layer.

11. The half-bridge circuit power module of claim 1, wherein:
respective drain terminals of the first high-side transistor and the second high-side transistor are disposed on and electrically coupled with the first patterned metal layer; and
respective drain terminals of the first low-side transistor and the second low-side transistor are disposed on and electrically coupled with the second patterned metal layer.
12. A half-bridge circuit power module (1500) comprising:
a substrate (1505) including:
a first patterned metal layer disposed on a surface of the substrate and electrically coupled with an output terminal;
a second patterned metal layer disposed on the surface of the substrate and electrically coupled with a DC- terminal;
a third patterned metal layer disposed on the surface of the substrate and electrically coupled with the output terminal;
a first low-side transistor (1520) disposed on the first patterned metal layer;
a second low-side transistor (1520) disposed on the first patterned metal layer;
a third low-side transistor (1520) disposed on the third patterned metal layer;
a fourth low-side transistor (1520) disposed on the third patterned metal layer;
a conductive clip (1542) electrically coupling the first low-side transistor, the second low-side transistor, the third low-side transistor and the fourth low-side transistor with the second patterned metal layer.
13. The half-bridge circuit power module of claim 12, wherein:
the conductive clip includes an opening (1543) through which the second patterned metal layer is exposed; and
the DC- terminal is electrically coupled with the second patterned metal layer via a conductive post (1541) disposed within the opening of the conductive clip.
14. The half-bridge circuit power module of claim 12, wherein:
the output terminal is coupled with the first patterned metal layer via a first conductive post (1530c); and
the output terminal is coupled with the third patterned metal layer via a second conductive post (1530d).

15. The half-bridge circuit power module of claim 12, wherein the substrate further includes:

a fourth patterned metal layer disposed on the surface of the substrate; and

a fifth patterned metal layer disposed on the surface of the substrate;

the half-bridge circuit power module further comprising:

a first high-side transistor disposed on the fourth patterned metal layer;

a second high-side transistor disposed on the fourth patterned metal layer;

a third high-side transistor disposed on the fifth patterned metal layer;

a fourth high-side transistor disposed on the fifth patterned metal layer;

a second conductive clip electrically coupling the first high-side transistor with the first patterned metal layer;

a third conductive clip electrically coupling the second high-side transistor with the first patterned metal layer;

a fourth conductive clip electrically coupling the third high-side transistor with the third patterned metal layer; and

a fifth conductive clip electrically coupling the fourth high-side transistor with the third patterned metal layer.

16. The half-bridge circuit power module of claim 15, wherein:

the fourth patterned metal layer is electrically coupled with a first DC+ terminal via a first conductive post (1517c); and

the fifth patterned metal layer is electrically coupled with a second DC+ terminal via a second conductive post (1517d).

17. A half-bridge circuit power module (1800) comprising:

a substrate (1805) including:

a first patterned metal layer disposed on a surface of the substrate and electrically coupled with an output terminal (1935);

a second patterned metal layer disposed on the surface of the substrate and electrically coupled with a DC- terminal (1925);

a third patterned metal layer disposed on the surface of the substrate and electrically coupled with the output terminal;

a first low-side transistor (1820) disposed on the first patterned metal layer;

a second low-side transistor (1820) disposed on the first patterned metal layer;

a third low-side transistor (1820) disposed on the first patterned metal layer;
a fourth low-side transistor (1820) disposed on the third patterned metal layer;
a fifth low-side transistor (1820) disposed on the third patterned metal layer;
a sixth low-side transistor (1820) disposed on the third patterned metal layer;
a first conductive clip (1842) electrically coupling the first low-side transistor and the fourth low-side transistor to the second patterned metal layer;
a second conductive clip (1842) electrically coupling the second low-side transistor and the fifth low-side transistor to the second patterned metal layer; and
a third conductive clip (1842) electrically coupling the third low-side transistor and the sixth low-side transistor to the second patterned metal layer.

18. The half-bridge circuit power module of claim 17, wherein the second patterned metal layer is electrically coupled with a DC- terminal a conductive post (1841a, 1841b).

19. The half-bridge circuit power module of claim 18, wherein the DC- terminal is electrically coupled with the second patterned metal layer via:

a first conductive post (1841a) disposed on the second patterned metal layer between the first conductive clip and the second conductive clip, the second conductive clip being closer to the DC- terminal than the first conductive clip; and

a second conductive post (1841b) disposed on the second patterned metal layer between third second conductive clip and the third conductive clip, the third conductive clip being closer to the DC- terminal than the second conductive clip.

20. The half-bridge circuit power module of claim 19, wherein a surface of the second conductive post coupled with the second patterned metal layer has an area that is smaller than an area of a surface of the first conductive post coupled with the second patterned metal layer.

21. A half-bridge circuit power module (2200) comprising:

a substrate (2105) including a first patterned metal layer, a second patterned metal layer, and a third patterned metal layer disposed on a surface of the substrate;

a first high-side transistor (2110) and a second high-side transistor (2210) disposed on the first patterned metal layer;

a first conductive clip electrically coupling the first high-side transistor with the second patterned metal layer;

a second conductive clip electrically coupling the second high-side transistor with the second patterned metal layer;

a first low-side transistor and a second low-side transistor disposed on the second patterned metal layer;

a third conductive clip electrically coupling the first low-side transistor with the third patterned metal layer;

a fourth conductive clip electrically coupling the second low-side transistor with the third patterned metal layer;

a DC+ terminal (2215a) that is electrically coupled with the first patterned metal layer via a first conductive post (2118a) disposed between the first high-side transistor and the second high-side transistor on the first patterned metal layer; and

a DC- terminal (2225) that is electrically coupled with the third patterned metal layer via a second conductive post (2141a) disposed between the third conductive clip and the fourth conductive clip on the third patterned metal layer.

22. The half-bridge circuit power module of claim 21, wherein the second patterned metal layer is electrically coupled with an output terminal (2235) of the half-bridge circuit power module via a third conductive post.

23. The half-bridge circuit power module of claim 22, wherein:

the first conductive clip electrically couples a source terminal of the first high-side transistor with the output terminal;

the second conductive clip electrically couples a source terminal of the second high-side transistor with the output terminal;

the third conductive clip electrically couples a source terminal of the first low-side transistor with the DC- terminal; and

the fourth conductive clip electrically couples a source terminal of the second low-side transistor with the DC- terminal.

24. The half-bridge circuit power module of claim 22, wherein:
the DC+ terminal, the DC- terminal and the output terminal include a first conductive material; and
the first conductive post, the second conductive post, and the third conductive post include a second conductive material different from the first conductive material.
25. The half-bridge circuit power module of claim 24, wherein:
the first conductive material is a metal; and
the second conductive material is an alloy of the metal.
26. The half-bridge circuit power module of claim 24, wherein:
the first conductive material is pure copper; and
the second conductive material is an alloy of copper including at least one of iron, or phosphorus.
27. The half-bridge circuit power module of claim 21, wherein:
the DC+ terminal is a first DC+ terminal; and
the substrate further includes:
a fourth patterned metal layer disposed on the surface of the substrate; and
a fifth patterned metal layer disposed on the surface of the substrate,
the half-bridge circuit power module further comprising:
a third high-side transistor having a drain terminal disposed on the fourth patterned metal layer;
a fourth high-side transistor having a drain terminal disposed on the fourth patterned metal layer;
a fifth conductive clip electrically coupling a source terminal of the third high-side transistor with the fifth patterned metal layer;
a sixth conductive clip electrically coupling the fourth high-side transistor with the fifth patterned metal layer;
a second DC+ terminal (2215) that is electrically coupled with the fourth patterned metal layer via a third conductive post (2119a) disposed between the third high-side transistor and the fourth high-side transistor.

28. The half-bridge circuit power module of claim 27, further comprising an output terminal (2235) that is:

electrically coupled with the second patterned metal layer via a fourth conductive post; and
electrically coupled with the fifth patterned metal layer via a fifth conductive post.

29. The half-bridge circuit power module of claim 21, wherein the substrate further includes a fourth patterned metal layer disposed on the surface of the substrate, the half-bridge circuit power module further comprising:

a third low-side transistor disposed on the fourth patterned metal layer; and
a fourth low-side transistor disposed on the fourth patterned metal layer,
the third conductive clip further electrically coupling the third low-side transistor to the third patterned metal layer,
the fourth conductive clip further electrically coupling the fourth low-side transistor to the third patterned metal layer.

30. The half-bridge circuit power module of claim 29, further comprising:
a fifth low-side transistor disposed on the second patterned metal layer;
a sixth low-side transistor disposed on the fourth patterned metal layer; and
a fifth conductive clip electrically coupling the fifth low-side transistor and the sixth low-side transistor with the third patterned metal layer,
the DC- terminal being further electrically coupled with the third patterned metal layer via a third conductive post (2141b) disposed between the fourth conductive clip and the fifth conductive clip on the third patterned metal layer.

31. The half-bridge circuit power module of claim 30, wherein:
the DC+ terminal is a first DC+ terminal; and
the substrate further includes a fifth patterned metal layer disposed on the surface of the substrate,
the half-bridge circuit power module further comprising:
a third high-side transistor disposed on the first patterned metal layer;
a sixth conductive clip electrically coupling the third high-side transistor with the second patterned metal layer;
a fourth high-side transistor disposed on the fifth patterned metal layer;

a seventh conductive clip electrically coupling the fourth high-side transistor with the fourth patterned metal layer;
a fifth high-side transistor disposed on the fifth patterned metal layer;
an eighth conductive clip electrically coupling the fifth high-side transistor with the fourth patterned metal layer;
a sixth high-side transistor disposed on the fifth patterned metal layer;
a ninth conductive clip electrically coupling the sixth high-side transistor with the fourth patterned metal layer; and
a second DC+ terminal (2215b) that is electrically coupled with fifth patterned metal layer via:
a third conductive post (2119a) disposed between the fourth high-side transistor and the fifth high-side transistor on the fifth patterned metal layer;
and
a fourth conductive post (2119b) disposed between the fifth high-side transistor and the sixth high-side transistor on the fifth patterned metal layer,
the first DC+ terminal being further electrically coupled with the first patterned metal layer via fifth conductive post disposed between the second high-side transistor and the third high-side transistor on the first patterned metal layer.

32. The half-bridge circuit power module of claim 21, wherein:
respective drain terminals of the first high-side transistor and the second high-side transistor are disposed on and electrically coupled with the first patterned metal layer; and
respective drain terminals of the first low-side transistor and the second low-side transistor are disposed on and electrically coupled with the second patterned metal layer.

33. A half-bridge circuit power module (2200) comprising:
a substrate (2105) including a first patterned metal layer, a second patterned metal layer, a third patterned metal layer, a fourth patterned metal layer, and a fifth patterned metal layer disposed on a surface of the substrate;
a first low-side transistor disposed on the first patterned metal layer and electrically coupled with the fifth patterned metal layer via a first conductive clip;
a second low-side transistor disposed on the first patterned metal layer and electrically coupled with the fifth patterned metal layer via a second conductive clip;

a third low-side transistor disposed on the second patterned metal layer and electrically coupled with the fifth patterned metal layer via the first conductive clip;

a fourth low-side transistor disposed on the second patterned metal layer and electrically coupled with the fifth patterned metal layer via the second conductive clip;

a first high-side transistor (2110) disposed on the third patterned metal layer and electrically coupled with the first patterned metal layer via a third conductive clip;

a second high-side transistor (2110) disposed on the third patterned metal layer and electrically coupled with the first patterned metal layer via a fourth conductive clip;

a third high-side transistor (2110) disposed on the fourth patterned metal layer and electrically coupled with the second patterned metal layer via a fifth conductive clip;

a fourth high-side transistor (2110) disposed on the fourth patterned metal layer and electrically coupled with the second patterned metal layer via a sixth conductive clip;

a first DC+ terminal (2215a) electrically coupled with the third patterned metal layer via a first conductive post (2118a) disposed between the first high-side transistor and the second high-side transistor on the third patterned metal layer;

a second DC+ terminal (2215b) electrically coupled with the fourth patterned metal layer via a second conductive post (2119a) disposed between the third high-side transistor and the fourth high-side transistor on the fourth patterned metal layer; and

a DC- terminal (2225) electrically coupled with the fifth patterned metal layer via a third conductive post (2141a) disposed between the first conductive clip and the second conductive clip on the fifth patterned metal layer.

34. The half-bridge circuit power module of claim 33, further comprising an output terminal (2235) that is:

coupled with the first patterned metal layer via a fourth conductive post; and
coupled with the second patterned metal layer via a fifth conductive post.

35. The half-bridge circuit power module of claim 34, wherein:
the first DC+ terminal, the second DC+ terminal and the output terminal include pure copper; and
the first conductive post, the second conductive post, the third conductive post, the fourth conductive post, and the fifth conductive post include an alloy of copper.

36. The half-bridge circuit power module of claim 35, wherein the alloy of copper includes at least one of iron or phosphorous.

37. The half-bridge circuit power module of claim 33, further comprising:
a fifth low-side transistor disposed on the first patterned metal layer and electrically coupled with the fifth patterned metal layer via a seventh conductive clip;
a sixth low-side transistor disposed on the second patterned metal layer and electrically coupled with the fifth patterned metal layer via the seventh conductive clip;
a fifth high-side transistor (211) disposed on the third patterned metal layer and electrically coupled with the first patterned metal layer via an eighth conductive clip;
a sixth high-side transistor (2110) disposed on the fourth patterned metal layer and electrically coupled with the second patterned metal layer via a sixth conductive clip,
the first DC+ terminal being further electrically coupled with the third patterned metal layer via a fourth conductive post (2118b) disposed between the second high-side transistor and the fifth high-side transistor on the third patterned metal layer;
the second DC+ terminal being further electrically coupled with the fourth patterned metal layer via a fifth conductive post (2119b) disposed between the fourth high-side transistor and the sixth high-side transistor on the fourth patterned metal layer, and
the DC- terminal is further electrically coupled with the fifth patterned metal layer via a sixth conductive post (2141b) disposed between the second conductive clip and the third conductive clip on the fifth patterned metal layer.

38. A method (2000) for producing a half-bridge circuit power module (2200), method comprising:

coupling (2005) a first high-side transistor (2110) and a second high-side transistor (2110) with a first patterned metal layer disposed on a surface of a substrate;

coupling (2005) a first low-side transistor and a second low-side transistors with a second patterned metal layer disposed on the surface of the substrate;

with a first conductive clip, electrically coupling (2010) the first high-side transistor with the second patterned metal layer;

with a second conductive clip, electrically coupling (2010) the second high-side transistor with the second patterned metal layer;

with a third conductive clip, electrically coupling (2010) the first low-side transistor with a third patterned metal layer disposed on the surface of the substrate;

with a fourth conductive clip, electrically coupling (2010) the second low-side transistor with the third patterned metal layer;

electrically coupling (2025) a DC+ terminal (2215a) with the first patterned metal layer via a first conductive post (2118a) disposed between the first high-side transistor and the second high-side transistor on the first patterned metal layer; and

electrically coupling (2025) a DC- terminal (2225) with the third patterned metal layer via a second conductive post (2141a) disposed between the third conductive clip and the fourth conductive clip on the third patterned metal layer.

39. The method of claim 38, further comprising electrically coupling (2025) an output terminal (2235) with the second patterned metal layer via a third conductive post.

40. The method of claim 39, wherein the DC+ terminal is a first DC+ terminal, the method further comprising:

coupling (2005) a third high-side transistor with a fourth patterned metal layer disposed on the surface of the substrate;

coupling (2005) a fourth high-side transistor with the fourth patterned metal layer;

coupling (2005) a third low-side transistor with a fifth patterned metal layer on the surface of the substrate;

coupling (2005) a fourth low-side transistor with the fifth patterned metal layer;

with a fifth conductive clip, electrically coupling (2025) the third high-side transistor with the fifth patterned metal layer;

with a sixth conductive clip, electrically coupling (2025) the fourth high-side transistor with the fifth patterned metal layer; and

electrically coupling a second DC+ terminal (2215b) with the fourth patterned metal layer via a fourth conductive post (2119a) disposed between the third high-side transistor and the fourth high-side transistor on the fourth patterned metal layer; and

further electrically coupling the output terminal with the fifth patterned metal layer via fifth conductive post,

the third conductive clip further electrically coupling the third low-side transistor with the third patterned metal layer, and

the fourth conductive clip further electrically coupling the fourth low-side transistor with the third patterned metal layer.