

MEMORY, CONTROL APPARATUS, CLOCK PROCESSING METHOD, AND ELECTRONIC DEVICE

ABSTRACT

A memory, a control apparatus, a clock processing method, and an electronic device are provided. A clock processing circuit in the memory includes: a duty cycle module, configured to adjust a duty cycle of a data clock signal to output an internal clock signal; a first clock generation module, configured to receive the internal clock signal, and output a first read clock signal based on the internal clock signal, the first read clock signal being a pulse signal; a second clock generation module, configured to generate and output a second read clock signal, the second read clock signal having only one level state change edge; and a selection module, configured to receive the first read clock signal and the second read clock signal, and output one of the first read clock signal and the second read clock signal as a target read clock signal.

[Fig. 4]