The invention relates to an integrated circuit arrangement for separating the composite synchronous signal and the video program system (VPS) data from a composite colour signal according to the preamble of Patent Claim 1.

A composite colour signal used for television image transmission is composed of at least one synchronization pulse or composite synchronous signal for synchronizing the sending end and receiving end, a colour burst as reference for decoding the colour information of the image and the image information. Transmitted inter alia in line 16 of the image information of the composite colour signal in the form of the video program system (VPS) data is a code for the remote control of a video recorder. This code contains data on the date, that is to say day and month, hours and minutes, the program source and the sound status, for example mono or stereo.

Signal separation of the individual items of information is necessary so that it is possible for the items of information contained in the composite colour signal to be further processed correctly. In terms of circuitry, this means that the composite colour signal must firstly be referred with the aid of a clamp circuit to a uniform signal level, and that the actual signal separation is then performed with the aid of at least one comparator. Since the separated items of signal information which are conditioned to form digital levels have to be further processed logically in a complicated manner, particular importance attaches to obtaining the clamping level and the various separation levels.

Separating the composite synchronous signal and the VPS data in television line 16 from the composite colour signal has previously been realized within the framework of a 2-chip system having an analog integrated circuit and known under the name of a video processor or data slicer. Current video processor types are, for example, the SAA 5230 module from the Valvo company or the SL 9100 module from the Plessey company.

From the economic point of view, only Very Large

Scale Integrated (VLSI) technologies, for example CMOS or single-channel MOS technologies, are sensible for the logically complicated further processing of the separated digital signal information.

It is the object of the invention to specify an MOS circuit, capable of integration, for separating the composite synchronous signal and the video program system (VPS) data in television line 16 from the composite colour signal, so that high yield quotas are guaranteed and mass production is rendered possible despite fluctuations in technical parameters due to assembly.

According to the invention, this object is achieved in a circuit arrangement of the type mentioned at the beginning by means of the features of the characterizing part of Patent Claim 1.

The circuit arrangement according to the invention has the advantage that it can be realized using the same technology as the digital evaluation logic for the separated signal information, and that it is therefore easy to produce 1-chip systems with a low external outlay on security. Moreover, the circuit arrangement according to the invention offers the advantage that it is possible to produce integrated MOS circuits with a very low power loss requirement.

Further embodiments of the invention are characterized in subclaims.

The invention is explained in more detail below with the aid of exemplary embodiments represented in the figures of the drawing, in which identical elements are provided with identical reference symbols, and

Figure 1 shows an exemplary embodiment of a clamp circuit according to the invention designed as a component circuit,

Figure 2 shows an exemplary embodiment of a circuit arrangement according to the invention with a detailed component circuit of a clamp circuit and a separation circuit for the synchronization pulses,

Figure 3 shows characteristic signals of the component

circuit in accordance with Figure 2,

Figure 4 shows an exemplary embodiment of a detailed component circuit for separating the digital VPS data in accordance with the invention, and

Figure 5 shows characteristic signals of the component circuit in accordance with Figure 4.

A composite colour signal coupled preferably capacitively into a circuit arrangement of the generic type must firstly be clamped at, that is to say referred to, a fixed reference level, since otherwise there is no sense in determining separation levels for signal components.

The clamp circuit in accordance with Figure 1, which is designed as a component circuit of a circuit according to the invention, comprises in the exemplary embodiment an MOS inverter amplifier composed of the transistor T1 and the load transistor T2, whose output A is connected to the input E via two transistors T3 and T4 connected as diodes. The transistor T1 is connected to the reference potential -VS, and the transistor T2 is connected to the supply potential +VS. The circuit in accordance with Figure 1 further contains a resistor R1, which is connected from the input E against the reference potential -VS, preferably has a high resistance and forms a bleed resistor against the reference potential. All the transistors are designed as MOS transistors.

The clamp circuit in accordance with Figure 1 represented [sic] an analog amplifier which is set at a fixed working point. The high-resistance bleed resistor R1 at the input E of the circuit firstly attempts to set the level of the reference potential -VS, to which a high voltage level would correspond at the output A, at the gate of the transistor T1, that is to say at the input of the inverter amplifier formed from the transistors T1 and T2. Because of the then high voltage difference between the output A and the input E, however, there flows through the two MOS diodes T4 and T3, which are connected in series and are preferably realized by these field-effect transistors, a powerful compensating current which

raises the gate potential of the transistor T1 until the voltage difference from output A to input E corresponds precisely to the sum of the threshold voltages of the two diodes T4 and T3. The clamp circuit thus comes into a stable state in which the voltage at the input E is set to be small by comparison with the threshold voltage of the transistor T1 and the output level is situated approximately 2 diode threshold voltages above the input level.

A periodic signal, such as the composite colour signal, which is capacitively coupled onto the input E is always formed at the input E of the clamp circuit in accordance with Figure 1 such that the most negative signal level coincides with the static quiescent input level. In the event of a deviation in the negative direction, the diode compensating current flowing through the transistors T4 and T3 recharges the input coupling capacitor (not illustrated in Figure 1). In the event of a deviation in the positive direction, the high-resistance bleed resistor R1 slowly draws capacitor energy from the coupling capacitor connected upstream of the input E, without being corrected by the current flowing through the transistors T4 and T3. In the case of a coupling capacitor connected upstream of the input E, this charging and discharging cycle is always active, since the bleed resistor R always dissipates energy from the coupling capacitor, if only to a slight extent.

Figure 3a shows a characteristic composite colour signal which comprises a composite synchronous signal or synchronization pulse SI, a colour burst FB and the image information BI, and which is referred by means of a clamp circuit in accordance with Figure 1 to the quiescent input level VEO as the most negative signal level. The composite colour signal clamped in this way onto the quiescent input level appears amplified in an inverted fashion at the output of the clamp circuit in accordance with Figure 3b, it being the case that because of the clamping principle the top amplitudes of the amplified composite synchronous signal or of the amplified

synchronization pulse SI does not rise above the quiescent output level VAO at the output A of the clamp circuit. The circuit arrangement according to the invention presupposes a minimum amplitude value of the synchronization pulses, which appear amplified at the output A.

Figure 2 shows a circuit arrangement according to the invention with a detailed component circuit of a clamp circuit, and a separation circuit for the composite synchronous signal. The circuit in accordance with Figure 2 contains integrated circuit elements SIA and DSA is [sic] separated by a dashed line and the terminal ICA of an integrated circuit from non-integrated circuit elements composed of a coupling capacitor C1 and the high-resistance bleed resistor R1. The clamp circuit in accordance with Figure 1 is basically contained in Figure 2 as the clamp circuit KI having the elements T1 to T4. By contrast with Figure 1, the tie point of the output circuit of the transistor T3 is connected, on the one hand, to the gate of the transistor T1 and, on the other hand, to the resistor R1 and the coupling capacitor C1 via the resistor R2 and the terminal ICA of the integrated circuit. The high-resistance bleed resistor R1 is connected, as in Figure 1, to the reference potential -VS, and the free terminal of the coupling capacitor is connected to the signal input EE. As a further difference from Figure 1, a capacitor C2 is arranged between the gate terminal and the drain terminal of the transistor T1.

Furthermore, there is connected to the terminal ICA a component circuit DSA which serves to separate the video program system (VPS) data. In terms of alternating voltage, an MOS signal amplifier SV is connected via a coupling capacitor CK to the clamp circuit KI, and its working point is adjusted with the aid of an MOS reference amplifier RV with a bleed resistor R and a gate circuit T. The outputs of the MOS signal amplifier or MOS reference amplifier are connected to a second MOS comparator K2. The component circuit DSA is described in

detail with the aid of Figure 4.

The detailed component circuit in accordance with Figure 2 contains, furthermore, an MOS reference inverter RI composed of the MOS transistors T7 to T11 and the resistor R7. By contrast with Figure 1 and the clamp circuit KI of Figure 2, the reference inverter RI contains three transistors T9 to T11, which are connected as diodes with their output circuits in series and are connected between the gate terminal of the transistor T7 and the output of the inverter circuits formed from the transistors T7 and T8. The reference inverter RI preferably has dimensions identical to those of the clamp inverter KI.

Connected downstream of the MOS reference inverter RI is a source follower composed of the MOS transistor T6 and the three series-connected resistors R4 to R6 which form an ohmic voltage divider. The reference inverter RI and the downstream source follower SF can be used to produce an output level which corresponds in a satisfactorily precise manner to the quiescent output level of the clamp inverter KI.

In the exemplary embodiment of Figure 2, the output A of the clamp circuit KI or of the MOS inverter amplifier composed of T1 and T2 is connected to the non-inverting input, and the tie point of the resistors R4 and R5 is connected as output of the source follower SF to the inverting input of an MOS comparator K1. Situated between the two inputs of the comparator K1 is the parallel circuit composed of the resistor R3 and the capacitor C3. The output of the comparator K1 forms the output of the detailed component circuit in accordance with Figure 2 and is connected to the output terminal SA. Likewise controlled by the output of the comparator K1 is an MOS transistor T5 whose output circuit is connected in parallel with the resistor R6.

The source follower load formed as an ohmic voltage divider from the resistors R4 to R6 is dimensioned such that the reference potential which is situated at the inverting input of the comparator K1 and

determines the separation level for the composite colour signal, which is situated clamped at the output A of the clamp circuit KI and amplified, is always located in the voltage range between the maximum level of the colour burst signal or of the image information signal and the minimum possible level of the synchronization pulse SI at the output A of the clamp circuit KI.

In accordance with the configuration of the exemplary embodiment according to Figure 2, it is advantageous that the resistor R6 can be bridged by an MOS switch T5, so that a hysteresis is superimposed on the optimum separation level. Of course, the separation level realized with the aid of the hysteresis is also situated between the maximum colour burst signal or image information signal and the minimum possible level of the synchronization pulse. The respectively applicable separation level is controlled with the aid of the transistor T5 by the output of the comparator K1, which compares the output of the clamp circuit KI with the separation level. If the output SA of the comparator K1 is situated at a high potential, that is to say the output signal of the clamp circuit KI is greater than the separation level, the separation level is switched to the lower hysteresis value. The latter is denoted in Figure 3c by the level VSU. As soon as the comparator K1 is switched over to the lower output potential, the separation level changes to the higher hysteresis value VSO in accordance with Figure 3c. It is achieved in this way that relatively small signal disturbances, in particular in the signal edges, do not cause the comparator K1 to change over. In accordance with Figure 3d, the separated composite synchronous signal or the separated synchronization pulse appear with the output level VSA at the comparator output SA.

In order to increase the noise immunity of the circuit in accordance with Figure 2, it is advantageous to incorporate further interference suppression measures, in particular for radio frequency interference. In accordance with the detailed component circuit of

Figure 2, for this purpose the first step is to provide a Miller capacitor, enlarged with the aid of the capacitor C2, of the clamp circuit KI, in order to dampen higher frequencies more strongly. Secondly, a capacitive coupling of two comparator inputs of the comparator K1 is provided with the aid of the capacitor C3, in order to achieve coupling between the two comparator inputs for high frequency components. In order to increase the effectiveness of the first measure, it is advantageous to provide the resistor R2 between the terminal ICA and the gate of the transistor T1, in order to increase the internal resistance of the composite colour signal source from the point of view of the clamp circuit KI. In the case of the second measure, it is advantageous for the resistor R3 to be connected in parallel with the capacitor C3 between the comparator inputs, in order to be able to set the frequency-dependent coupling factor by varying the time constants.

The detailed component circuit in accordance with Figure 4 exhibits an integrated circuit DSA for separating the video program system data in line 16 of the composite colour signal. In accordance with Figure 4 or Figure 2, the signal input EE is connected via a coupling capacitor C1 to the terminal ICA of an integrated circuit, on the one hand, and via the resistor R1 to the reference potential -VS, on the other hand. A detailed component circuit SIA in accordance with Figure 2 is connected downstream of the terminal ICA. Likewise connected to the terminal ICA is the component circuit DSA in accordance with Figure 4, which leads via a coupling capacitor CK to the input I of an MOS signal amplifier SV formed from the MOS transistors T20 and T21. The output O of the MOS signal amplifier SV is applied, on the one hand, to the inverting input of a second comparator K2 and, on the other hand, to the reference potential -VS via an MOS transistor T22, connected as a diode, and a downstream resistor R20.

Necessarily serving in accordance with Figure 4 as MOS reference amplifier RV in the data separation

circuit DSA is an inverter amplifier which has dimensions identical to those of the MOS signal amplifier SV and is composed of the MOS transistors T23 and T24 and is fed back from its output to its input via an MOS transistor T25 connected as a diode. Like the feedback transistors T3, T4 and T9 to T11, the transistor T22 and the feedback transistor T25 are preferably field-effect transistors. Furthermore, the reference amplifier has a high-resistance bleed resistor R21 from the input to the reference potential -VS. The input gate voltage of the reference amplifier RV is fed in a high-resistance manner to the gate of the MOS signal amplifier SV via the resistor R22 and the recharging gate formed by the MOS transfer transistor T26. The gate terminal of the transfer transistor T26 is connected by means of a terminal LE to a logic unit (not illustrated) which drives the recharging gate or the transistor T26 in a manner yet to be described. Also performed at the tie point of the output circuit of the transistor T26 and the gate terminal of the transistor T20 is the capacitive feeding via the coupling capacitor CK of the internal composite colour signal already clamped for obtaining the synchronization signal. The output of the reference amplifier RV is led to the non-inverting input of the second MOS comparator K2, whose output DA forms the output terminal for the separated data signal.

A precondition for the separation and conditioning of the video program system data is signal clamping of the composite colour signal in the clamp circuit KI and the temporal information, obtained from the composite synchronous signal with the aid of the separated synchronization signal, for the occurrence of the signal in line 16 of the composite colour signal. In accordance with the specification of the video program system data, the data signal is present in Manchester II code (biphase code), that is to say on average over each bit the signal is situated 50% at a high potential and 50% at a low potential. Because of this fact, digitization of the VPS data is prepared according to the invention in a very

simple manner with the aid of the component circuit DSA, which is coupled to an AC voltage, by providing in parallel with the MOS signal amplifier SV the MOS reference amplifier RV which holds its own working point constant and adjusts that of the signal amplifier.

The data signal amplified with respect to the working point of the MOS signal amplifier and the quiescent working point, corresponding to the arithmetic mean of the biphase code, of the reference amplifier RV are fed to the second MOS comparator K2 which then ensures optimum data separation. It is assumed in this case that setting and adjusting the working point of the MOS signal amplifier SV may only be performed if there really are VPS data present for amplification. This information is derived logically from the synchronized instant obtained by separating the composite synchronous signal, or the composite colour signal, and fed to the recharging gate circuit, formed from the MOS transistor T26, for the working point. The derivation of the information for opening the recharging gate is not illustrated in Figure 4, but follows with the aid of means familiar to the person skilled in the art.

Recharging the coupling capacitor CK for the working point is performed with the aid of the recharging gate circuit of the transistor T26 and of the upstream logic unit LE only if data have been detected in line 16 of the composite colour signal, or if it is possible for the data to be accepted during [sic] the region defined for it inside the line 16. This circuit measure according to the invention renders it possible simultaneously to store an optimum working point of the MOS signal amplifier SV from one line 16 signal to the next line 16 signal. If data are not correctly detected within a line 16 signal of a composite colour signal, the working point control remains active nevertheless, although it may be that only noise is being amplified. In any case, the working point for the next separation cycle is prepared in this way. Periodic noise occurring at field or frame frequency, such as system hum, for example, is also

largely eliminated with the aid of the circuit arrangement according to the invention.

For reasons of symmetry, the elements T22 and R20 are used to offer the MOS signal amplifier SV load conditions identical to those for the MOS reference amplifier RV, that is to say from the output of the amplifier the negative feedback diode and the downstream bleed resistor to the reference potential -VS [sic]. Since the MOS signal amplifier and the MOS reference amplifier statically see the identical gate voltage at the input and their outputs see identical load conditions, the two component amplifiers also transmit the identical quiescent output level.

A few characteristic signals are recorded in accordance with Figure 5. Figure 5a shows the clamped composite colour signal, which is referred to a quiescent input level of the clamp circuit KI and can be tapped at the terminal ICA of the circuit according to the invention. Figure 5b shows the clamped signal, reduced by the voltage difference UCK across the coupling capacitor CK, at the input I of the MOS signal amplifier SV. This capacitively coupled signal at the input of the MOS amplifier leads to optimum deflections above the quiescent output level VOO at the output O or at the inverting input of the second MOS comparator K2 in accordance with Figure 5c. Since the quiescent output level of the reference inverter corresponds to the quiescent output level VOO, it is possible for the separated video program system data to be tapped in accordance with Figure 5d in digital form at the output DA of the second MOS comparator K2.

The data separation circuit according to the invention also permits teletext data to be separated when the opening of the recharging gate is applied for adjusting the working point in the teletext lines and is limited to the time of the runin, that is to say a uniform 1/0 data bit sequence for synchronizing the data clock pulse generator.

The circuit arrangement according to the

invention which is described in the exemplary embodiment in accordance with Figures 1 to 5 is described in single-channel NMOS technology only by way of example. The circuit can be realized just as advantageously in complementary MOS technology or in PMOS technology.

Patent claims

1. Integrated circuit arrangement for separating the composite synchronous signal and the video program system (VPS) data from a composite colour signal, having a clamp circuit for the composite colour signal and at least one comparator for determining a separation level, characterized in that the clamp circuit (T1 to T4, R1; KI) contains an MOS inverter amplifier (T1, T2), the input (E) of which can be connected in a high-resistance manner (R1) to a reference potential (-VS) and is connected to the output of the MOS inverter amplifier (T1, T2) via MOS transistors (T3, T4) connected as diodes, and the output (A) of which, like the output of an MOS reference inverter (RI), is connected in each case to one input (+, -) of a first MOS comparator (K1), the output (SA) of which supplies the composite synchronous signal, and in that in terms of alternating voltage, an MOS signal amplifier (SV) is coupled to the input (E) of the MOS inverter amplifier (T1, T2) of the clamp circuit (T1 to T4, R1; KI) to which an MOS reference amplifier (RV) is connected for adjusting the working point, and the output (O) of the MOS signal amplifier (SV), like the output of the MOS reference amplifier (RV), is applied in each case to an input (+, -) of a second MOS comparator (K2), the output (DA) of which supplies the video program system (VPS) data.

2. Arrangement according to Claim 1, characterized in that the input of the MOS reference inverter (RI) is connected in a high-resistance manner (R7) to the reference potential (-VS), and to the output of the MOS reference inverter (RI) via MOS transistors (T9) to (T11) connected as diodes.

3. Arrangement according to Claim 1 or 2, characterized in that the elements of the MOS reference inverter (RI) and of the clamp circuit (T1 to T4, R1; KI) have identical dimensions.

4. Arrangement according to Claim 1 to 3, characterized in that connected downstream of the MOS reference inverter (RI) is an MOS source follower (SF), the source

follower load of which is designed as an ohmic voltage divider (R4, to R6).

5. Arrangement according to Claim 1 to 4, characterized in that a resistor (R6) of the ohmic voltage divider (R4 to R6) of the MOS source follower (SF) can be bridged by an MOS switch (T5) controlled by the output (SA) of the first MOS comparator (K1).

6. Arrangement according to Claim 1 to 5, characterized in that a capacitor (C2, C3) is provided in each case between input (E) and output (A) of the clamp circuit (T1 to T4, R1; KI) and between the inputs of the first MOS comparator (K1).

7. Arrangement according to Claim 1 to 6, characterized in that on the input side a series resistor (R2) is connected upstream of the clamp circuit (T1 to T4; KI) and a parallel resistor (R3) is connected upstream of the first MOS comparator (K1).

8. Arrangement according to one of Claims 1 to 7, characterized in that the MOS signal amplifier (SV) and the MOS reference amplifier (RV) are connected via a MOS gate circuit (T26) which, with the aid of a logic circuit, opens during a band of the composite colour signal defined for data signals.

9. Arrangement according to Claim 1 to 8, characterized in that the MOS signal amplifier (SV) and the MOS reference amplifier (RV) have the same load (T22, R20, T25, R21) in each case.

10. Arrangement according to Claim 1 to 9, characterized in that the MOS reference amplifier (RV) operates in an inverting manner and its input is connected in a high-resistance manner (R21, R22) both to the reference potential (-VS) and also via the MOS gate circuit (T26) to the input (E) of the MOS signal amplifier (SV), and via at least one MOS transistor (T25) connected as a diode to its output.