

ELECTROSTATIC CHUCK WITH HIGH-DENSITY PLASMA BARRIER COATING

BACKGROUND

[0001] Plasma-enhanced chemical vapor deposition (PECVD) is a technique used for depositing thin films or coatings onto substrates. A precursor gas is introduced into a vacuum chamber in which a plasma is formed. The precursor gas is then converted to reactive chemical species by the plasma. The reactive chemical species can adsorb to a substrate surface to form a solid film on the substrate.

[0002] PECVD often uses a capacitively coupled plasma formed between a showerhead and a pedestal of a PECVD tool. A related film deposition method known as high-density plasma (HDP) CVD increases an ion flux density to which a substrate is exposed compared to conventional PECVD by using an inductively coupled plasma. The higher ion flux can result in the formation of a denser film on the substrate.

SUMMARY

[0003] This Summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used to limit the scope of the claimed subject matter. Furthermore, the claimed subject matter is not limited to implementations that solve any or all disadvantages noted in any part of this disclosure.

[0004] Examples are disclosed that relate to protecting a substrate from contamination from an electrostatic chuck during a high-density plasma (HDP) chemical vapor deposition (CVD) process. One example provides an electrostatic chuck comprising a substrate-facing surface comprising one or more substrate contact areas. The electrostatic chuck further comprises a HDP barrier coating on at least a portion of the one or more substrate contact areas.

[0005] In some such examples, the HDP barrier coating comprises one or more of silicon oxide, fluorine-doped silicon oxide, silicon oxynitride, silicon oxycarbide, silicon oxycarbonitride, or silicon carbide.

[0006] Additionally or alternatively, in some such examples, the HDP barrier coating has a thickness of 3 microns to 5 microns.

[0007] Additionally or alternatively, in some such examples, a peak-to-peak variation of a thickness of the HDP barrier coating is less than or equal to 10% of an average value of the thickness.

[0008] Additionally or alternatively, in some such examples, the electrostatic chuck comprises aluminum nitride.

[0009] Another example provides a method of operating a vapor deposition tool. The method comprises placing a substrate on an electrostatic chuck comprising a HDP barrier coating. The method further comprises depositing an HDP film on the substrate using HDP-CVD.

[0010] In some such examples, depositing the HDP film on the substrate using HDP-CVD comprises forming an oxide layer in a fully depleted silicon-on-insulator substrate fabrication process.

[0011] Additionally or alternatively, in some such examples, the HDP barrier coating comprises one or more of silicon oxide, fluorine-doped silicon oxide, silicon oxynitride, silicon oxycarbide, silicon oxycarbonitride, or silicon carbide.

[0012] Additionally or alternatively, in some such examples, the HDP barrier coating has a thickness of 3 microns to 5 microns.

[0013] Additionally or alternatively, in some such examples, the method comprises, after depositing HDP oxide films on a plurality of substrates including the substrate, removing the pre-coating and the HDP barrier coating, and then applying a new pre-coating and a new HDP barrier coating on the electrostatic chuck.

[0014] Additionally or alternatively, in some such examples, removing the pre-coating and the HDP barrier coating comprises removing the pre-coating and the HDP barrier coating using a fluoride plasma.

[0015] Additionally or alternatively, in some such examples, applying the HDP barrier coating to the electrostatic chuck using the vapor deposition tool.

[0016] Additionally or alternatively, in some such examples, the method comprises adjusting a processing gas mixture before applying the HDP barrier coating.

[0017] Another example provides a method of operating a HDP-CVD tool. The method comprises applying an HDP barrier coating to the electrostatic chuck.

[0018] In some such examples, the method comprises, before applying the HDP barrier coating to the electrostatic chuck, covering a top surface of one or more substrate contact areas of the electrostatic chuck with a protective cover, applying a pre-coating

to surfaces within a processing chamber of the HDP-CVD tool, and then uncovering the top surface of the one or more substrate contact areas of the electrostatic chuck.

[0019] Additionally or alternatively, in some such examples, the method comprises adjusting a processing gas mixture between applying the pre-coating and applying the HDP barrier coating to the electrostatic chuck.

[0020] Additionally or alternatively, in some such examples, the HDP barrier coating comprises one or more of silicon oxide, fluorine-doped silicon oxide, silicon oxynitride, silicon oxycarbide, silicon oxycarbonitride, or silicon carbide.

[0021] Additionally or alternatively, in some such examples, depositing the HDP barrier coating comprises depositing an HDP barrier coating having a thickness of 3 microns to 5 microns.

[0022] Additionally or alternatively, in some such examples, the method comprises, removing the HDP barrier coating, and then applying a new HDP barrier coating on the electrostatic chuck.

[0023] Additionally or alternatively, in some such examples, removing the HDP barrier coating comprises removing the HDP barrier coating using a fluoride plasma.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] FIG. 1 shows an example of an HDP-CVD (high-density plasma chemical vapor deposition) tool.

[0025] FIG. 2 shows a flow diagram depicting an example method of forming an HDP barrier coating on an electrostatic chuck.

[0026] FIG. 3 shows a flow diagram depicting an example method of operating a HDP-CVD tool.

[0027] FIG. 4 shows a flow diagram depicting another example method of operating a HDP-CVD tool.

[0028] FIGS. 5A-5F schematically show a cross-sectional view of a substrate at various stages in an example HDP-CVD process.

[0029] FIG. 6 shows an example of a silicon-on-insulator (SOI) wafer and an fully depleted SOI (FDSOI) device that can be produced using the HDP-CVD tool of FIG. 1.

[0030] FIG. 7 shows a chart illustrating example Al contamination levels of a HDP-CVD film deposited using an uncoated electrostatic chuck compared to an HPD-CVD film deposited using an coated with an HDP-CVD barrier coating.

[0031] FIG. 8 shows a flow diagram depicting another example method of operating a HDP-CVD tool.

[0032] FIG. 9 shows a schematic diagram of an example computing system.

DETAILED DESCRIPTION

[0033] The term “chemical vapor deposition” (CVD) generally represents a process in which a solid phase film is formed on a substrate by directing a flow of one or more precursor gases over the substrate surface under conditions configured to cause the chemical conversion of the precursor gases to the solid phase film. The term “plasma-enhanced chemical-vapor deposition” (PECVD) generally represents a CVD process in which a plasma is used to facilitate the chemical conversion of one or more precursor gases to a solid phase film on a substrate. The term “high-density plasma CVD” (HDP-CVD) generally represents a CVD process that uses an inductively coupled plasma to form a higher-density plasma than conventional PECVD. The terms “growth”, “deposition”, and variants thereof, also may be used to refer to film formation.

[0034] The term “electrostatic chuck” generally represents a physical structure configured to securely hold a substrate during a process by application of an electrostatic force.

[0035] The term “flow control hardware” generally represents components configured to place one or more chemical sources in fluid connection with a processing chamber. Flow control hardware may comprise one or more mass flow controllers and/or valves, for example.

[0036] The term “fully depleted silicon-on-insulator” (FDSOI) generally represents a semiconductor process technology utilizing a substrate with a base silicon layer, a thin “buried” oxide layer, and a top silicon layer covering the buried oxide layer. FDSOI transistor devices include channels built above the buried oxide layer. Due to the buried oxide layer, the channels can be undoped. The term “silicon-on-insulator” (SOI) refers generally to a substrate comprising a base silicon layer, a buried oxide layer, and a top silicon layer.

[0037] The term “HDP barrier coating” generally represents a film applied by HDP-CVD onto an electrostatic chuck. Example HDP barrier coatings include SiO₂, fluorine doped SiO₂, silicon oxynitride (SiO_xN_y), silicon oxycarbide (SiO_xC_y), silicon oxycarbonitride (SiO_xC_yN_z), and silicon carbide (SiC).

[0038] The term “HDP film” generally represents a film deposited using HDP-CVD. HDP films have higher densities than similar films formed using PECVD with a capacitively coupled plasma.

[0039] The term “oxide layer” generally represents a material layer comprising oxygen and an oxidized species. Examples of oxide layers comprise SiO₂, SiO_xN_y, SiO_xC_y, SiO_xC_yN_z, and metal oxides (e.g., hafnium oxide (HfO_x), titanium oxide (TiO_x), tungsten oxide (WO_x), tin oxide (SnO_x), and molybdenum oxide (MoO_x)).

[0040] The term “plasma generator” generally represents a device configured to generate a plasma to provide reactive species and/or energetic ions for substrate processing in a processing chamber.

[0041] The term “pre-coating” generally represents a process for depositing a film on surfaces of a processing chamber before performing substrate processing. Example films that can be deposited during pre-coating include SiO₂, fluorine-doped SiO₂, SiO_xN_y, SiO_xC_y, SiO_xC_yN_z, and SiC.

[0042] The term “processing chamber” generally represents an enclosure in which chemical and/or physical processes are performed on substrates. The pressure, temperature and atmospheric composition within a processing chamber are controllable to perform chemical and/or physical processes.

[0043] The term “protective cover” generally represents a structure that is placed over an electrostatic chuck during a pre-coating process to protect substrate contact areas of the electrostatic chuck from the pre-coating process.

[0044] The term “substrate” generally represents any object on which a film can be deposited.

[0045] As introduced above, PECVD is a technique used for depositing thin films or coatings onto a substrate. Conventional PECVD can utilize a capacitively coupled plasma formed between a showerhead and a substrate in a processing chamber to provide energy for the CVD process. HDP-CVD increases plasma density relative to conventional PECVD by using an inductively coupled plasma. The inductively coupled plasma can provide for a higher ion flux at the substrate surface than a capacitively coupled plasma. This can result in formation of a denser film on the substrate than

conventional PECVD. HDP-CVD can also result in a film of higher uniformity and conformality than conventional PECVD. As one example, HDP-CVD can be used to produce a uniform thin oxide film ($< 250 \text{ \AA}$ in thickness) on a base silicon substrate for use as a buried oxide layer in a silicon-on-insulator (SOI) substrate. Such substrates can be used to fabricate fully-depleted silicon-on-insulator (FDSOI) devices.

[0046] Contamination in a processing chamber can cause problems during a semiconductor device fabrication process. Possible sources of contamination can include chamber materials. To help prevent contamination of a substrate during a film deposition process, surfaces within a processing chamber can be precoated with a pre-coat film prior to performing HDP-CVD. The pre-coat film can help to prevent substrate contamination arising from processing chamber material.

[0047] Typically, an electrostatic chuck (ESC) within the processing chamber is covered with a protective cover during the pre-coat process in an HDP-CVD processing tool. The protective cover helps to prevent the pre-coat material from coating substrate contact areas on the ESC. Substrate contact areas of the ESC thus are in direct contact with a substrate held on the ESC during an HDP-CVD process. Due to the direct contact between the substrate and the ESC, ESC materials can potentially migrate into the substrate from the ESC during an HDP process. For example, some ESCs include aluminum nitride substrate contact areas. As such, aluminum can potentially migrate into a substrate during an HDP process. This can potentially lead to contamination of a SOI substrate being fabricated, for example. Further, uncoated portions of the ESC also can be sputter etched during an HDP CVD process. This also can pose a risk of contamination of a substrate being processed.

[0048] Accordingly, examples are disclosed that relate to helping prevent substrate contamination from ESC materials during an HDP-CVD process. Briefly, embodiments of the disclosed invention describe ESCs with HDP barrier coatings, and the application of HDP barrier coatings to ESCs. The HDP barrier coating is a denser layer than the pre-coat layers deposited on other surfaces of the chamber. The HDP barrier coating can help to reduce a rate of electromigration of ESC materials into the substrate without unfavorably impacting substrate clamping force. The HDP barrier coating also can help to prevent contamination from sputter etching of ESC materials during an HDP deposition process. This can provide further protection against contamination from ESC materials.

[0049] In some examples, an HDP barrier coating on an ESC comprises a silicon oxide coating. Example silicon oxide coatings include SiO₂, doped SiO₂ (e.g., fluorine-doped SiO₂), SiO_xN_y, SiO_xC_y, and/or SiO_xC_yN_z. In other examples, the HDP barrier coating comprises any other suitable material. Another example of a suitable HDP barrier coating material includes SiC.

[0050] In some examples, an HDP barrier coating has a thickness in a range of 1-5 microns. In some more specific examples, the thickness is in a range of 3-5 microns. In yet more specific examples, the thickness is in a range of 3-4.2 microns. In other examples, the HDP barrier coating has any other suitable thickness. Other examples include thicknesses greater than 5 microns and less than 1 micron. Such thicknesses of the HDP barrier coating may help to reduce metal contamination of an HDP film being deposited on a substrate, such as an HDP-CVD film deposited using an HDP-CVD tool while still providing for suitable substrate clamping force.

[0051] The thickness of an HDP barrier coating can be highly uniform across a substrate-facing surface of the ESC. In some examples, the thickness can have a peak-to-peak variation of less than or equal to 10% of an average value of the thickness. In some more specific examples, the thickness can vary by 250 Å or less when the average value of the thickness is 4000 Å. In other examples, the peak-to-peak variation is less than or equal to 1% of the average value of the thickness. In this manner, the HDP barrier coating provides suitably uniform protection across an entire substrate. Such HDP barrier coatings, and methods of forming the HDP barrier coatings, are discussed in more detail below.

[0052] FIG. 1 shows a schematic view of an example HDP-CVD tool 100 for depositing an HDP barrier coating and/or an HDP film as disclosed. The HDP-CVD tool 100 comprises a processing chamber 102. The processing chamber 102 encloses various other components of the reactor and serves to contain the plasma. The HDP-CVD tool 100 further comprises an ESC 104 for holding a substrate during an HDP-CVD process. While described herein in the context of HDP-CVD, it will be appreciated that an HDP-CVD-coated ESC can be used in any other suitable tool. Other examples of suitable tools include ALD and non-plasma-enhanced CVD tools.

[0053] The ESC 104 comprises a moveable pedestal 108. In some examples, a bipolar electrode of the ESC 104 provides clamp capability using an inner and outer electrode. Temperature uniformity can be tuned by adjusting offset voltage. In this manner, the ESC 104 can control a temperature of the substrate 106 and the ESC 104.

[0054] The HDP-CVD tool 100 further comprises a gas ring 110 for introducing processing gases into the processing chamber. The HDP-CVD tool 100 alternatively or additionally can comprise other processing gas inlets than the gas ring 110. The processing tool 100 further comprises flow control hardware 112. The flow control hardware 112 connects processing gas source(s) to the processing chamber 102. In the depicted example, the flow control hardware 112 connects a silicon-containing precursor source 114, an oxidizing agent source 116, an optional hydrogen-containing gas source 118, an inert gas source 120, and an optional additive source 122 to the processing chamber 102. The flow control hardware 112 can include any suitable components. Examples include mass flow controllers, valves, and conduits.

[0055] The Si-containing precursor source 114 comprises any suitable Si-containing precursor material. Some examples of suitable Si-containing precursor materials include silane and disilane. In other examples, the Si-containing precursor source comprises SiF_4 , which results in formation of a fluorine-doped silicon oxide layer.

[0056] The oxidizing agent source 116 can comprise any suitable oxidizing agent that can be introduced into a processing chamber to oxidize the Si-containing precursor. Examples include water, molecular oxygen (O_2), and oxygen-containing organic molecules, such as alcohols. Example alcohols include methanol, ethanol, 1-propanol, 2-propanol, isobutanol, tert-butanol, 1-butanol, and 2-butanol. In some examples, an oxidizing agent can be in a condensed phase at standard pressure and temperature. In such examples, the oxidizing agent source 116 can comprise a flow-over vapor delivery system, a vaporizer delivery system, charged volume delivery system, a mole delivery device, or other suitable delivery system to volatilize the condensed phase oxidizing agent.

[0057] The optional hydrogen-containing gas source 118 can be used to form reducing environments for a plasma treatment. Example hydrogen-containing gases include molecular hydrogen (H_2) and ammonia (NH_3).

[0058] The inert gas source 120 can comprise any suitable inert gas. Examples include He, Ne, Ar, Kr, and Xe. In some examples, one or more additional inert gas sources can be included, each providing a different inert gas.

[0059] The optional additive source 122 can comprise any suitable additive. Examples include F_2 and volatile metal-containing precursors that can be used to deposit a doped HDP film. In other examples, the additive source 122 comprises a

nitrogen-containing gas source, such as N₂ or N₂O. A nitrogen-containing gas can be used to form a nitride or nitrogen-doped HDP film.

[0060] The HDP-CVD tool 100 of FIG. 1 comprises two plasma sources: a top RF coil 124 and a side RF coil 126. The top RF coil 124 is a medium frequency (MFRF) coil and the side RF coil 126 is a low frequency (LFRF) coil. Power applied using the LFRF coil may aid in ionization of precursor gases to initiate plasma formation. In some examples, the LF power comprises frequencies in a range of 300-400 kHz. In some more specific examples, the LF power comprises frequencies in a range of 325-375 kHz. In further more specific examples, the LF power comprises frequencies in a range of 340-370 kHz. In some examples, the LF power is applied at 0.5 – 8 kW. In some more specific examples, the LF power is applied at 5 kW.

[0061] Power applied using the MFRF coil can create a magnetic field to confine and control the plasma. This results in higher plasma densities and higher ionization efficiency than conventional PECVD. In some examples, the MF power comprises frequencies in a range of 400-500 kHz. In some more specific examples, the MF power comprises frequencies in a range of 425-475 kHz. In further more specific examples, the MF power comprises frequencies in a range of 430 to 470 kHz. In some examples, the MF power is applied at 0.5 – 5 kW. In some more specific examples, the MF power is applied at 5 kW. However, the methods and apparatus disclosed herein are not limited to operation in reaction chambers with dual sources, these frequencies, or RF plasma sources. Any suitable plasma source or sources may be used.

[0062] A high frequency (HFRF) source 128 serves to electrically bias substrate 106 and draw charged reactant species onto the substrate for the deposition reaction. Electrical energy from the HFRF source 128 is coupled to substrate 106 using an electrode or capacitive coupling, for example. In some examples, the HF power comprises frequencies in a range of 10 MHz to 10 GHz. In some more specific examples, the HF power comprises a frequency of 10-15 MHz. In some examples, the HF power is applied at 0.5 – 10 kW. In some more specific examples, the HF power is applied above 10 kW. Note that the bias applied to the substrate need not be an RF bias. Other frequencies and DC biases may be used as well.

[0063] Injectors may be connected to the primary gas ring 110 to direct at least some of the gases or gas mixtures into the processing chamber 102 and toward the ESC 104. In other examples, any other suitable process gas delivery system may be employed.

[0064] In some examples, the process gas is additionally or alternatively introduced using one or more inlets 130. The component gases of the process gas may be premixed or not. In some examples, the process gas is introduced through a gas supply inlet mechanism including orifices. In some examples, at least some of the orifices orient the process gas along an axis of injection intersecting an exposed surface of the substrate at an acute angle.

[0065] Process gases exit chamber 102 through an outlet 123. A vacuum pump (e.g., a turbomolecular pump) typically draws process gases out and maintains a suitably low pressure within the reactor.

[0066] The HDP-CVD tool 100 further comprises a robot 132 for moving substrates 106 into and out of the processing chamber 102. The robot 132 is configured to transfer substrates 106 without contaminating the substrates 106 or the processing chamber 102.

[0067] The HDP-CVD tool 100 further comprises a controller 134. The controller 134 is operatively coupled to the moveable pedestal 108, the flow control hardware 112, the LFRF source 126, the MFRF source 124, and/or the HFRF source 128. The controller 134 is configured to control various functions of the HDP-CVD tool 100 to perform a thin film deposition process, such as HDP-CVD. For example, the controller 134 is configured to operate a height of the moveable pedestal 108 to maintain the ESC 104 and/or the substrate 106 at a desired temperature. The controller 134 also is configured to operate the flow control hardware 112 to flow a selected gas or mixture of gases at a selected rate into the processing chamber 102. The controller 134 is further configured to remove gases from processing chamber 102 by controlling exhaust flow through outlet 123. The controller 134 is further configured to operate the top RF coil 124, the side RF coil 126, and the HFRF source 128.

[0068] The controller 134 can include one or more memory devices and one or more processors. A processor can include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc. The controller 134 can comprise any suitable computing system. Example computing systems are described below with reference to FIG. 9.

[0069] The controller 134 can control all of the activities of the deposition apparatus. The system controller 134 executes system control software, including sets of instructions for controlling the timing, mixture of processing chemicals, chamber pressure, chamber temperature, substrate temperature, radio frequency (RF) power

levels for plasma pre-treatments, substrate chuck or pedestal position, and other parameters of a particular process. Other computer programs stored on memory devices associated with the controller 134 can be employed in some examples.

[0070] In some examples, the controller 134 comprises a user interface. The user interface can include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0071] The controller parameters relate to process conditions. Examples of such process conditions include process gas composition and flow rates, temperature, pressure, cooling gas pressure, substrate temperature, and chamber wall temperature. These parameters are provided to the user in the form of a recipe, and can be entered utilizing the user interface. Signals for monitoring the process can be provided by analog and/or digital input connections of the system controller 134. The signals for controlling the process are output on analog and digital output connections of the processing tool 100.

[0072] The system software can be designed or configured in many different ways. For example, various chamber component subroutines or control objects can be written to control operation of the chamber components necessary to carry out pre-coating and HDP-CVD barrier coating of an ESC in accordance with the methods and processes described herein. Examples of programs or sections of programs for this purpose include substrate positioning code, process gas control code, pressure control code, and heater control code. Example hardware for controller 134 is described below with regard to FIG. 9.

[0073] FIG. 2 shows a flow diagram depicting an example method 200 of operating a HDP-CVD tool, such as the HDP-CVD tool 100 of FIG. 1. Method 200 optionally comprises depositing a pre-coating in the chamber before forming the HDP barrier coating on the ESC. In such examples, at 202, the method 200 can comprise covering an ESC within a processing chamber of the HDP-CVD tool to protect substrate contact areas of the ESC from the pre-coating process. This is illustrated in FIG. 5A, which schematically shows a cross-sectional view of an example processing chamber 500. The processing chamber 500 comprises an ESC 502. A protective cover 504 is positioned over a substrate-facing surface 506 of the ESC 502. The protective cover 504 can be placed on the ESC 502, for example, by a robot prior to performing the pre-coating process. The ESC 502 comprises a dielectric material with a finite resistance.

In some examples, the dielectric material can comprise aluminum nitride (AlN). An electric current conducted through the bipolar electrode and the substrate creates a charge layer at the dielectric-substrate interface. This charge layer creates an attractive electrostatic force to clamp the substrate to substrate contact areas 507 of the ESC. In some examples, the protective cover 504 is clamped in a similar manner. In other examples, the protective cover 504 is held in place by gravity, without an electrostatic clamping force. In some examples, other protective mechanism(s) can be used to shield the top surface of the substrate contact areas 507.

[0074] Referring again to FIG. 2, in examples that include optionally applying a pre-coating, after covering the ESC at 202, the method 200 comprises, at 204, applying the pre-coating to surfaces within a processing chamber of the HDP-CVD tool. For example, FIG. 5B schematically illustrates a pre-coating 508 within the processing chamber 500 of FIG. 5A. In the example of FIG. 5B, the pre-coating 508 is deposited on interior chamber surfaces, including exposed surfaces of the ESC 502 and the protective cover 504. The pre-coating 508 also is deposited on walls of the processing chamber 500, as well as other structures within the processing chamber.

[0075] The pre-coating 508 can be formed by introducing suitable precursor gases into the processing chamber while a plasma is ignited. In some examples, the pre-coating comprises one or more of SiO₂, fluorine-doped SiO₂, SiO_xN_y, SiO_xC_y, SiO_xC_yN_z, and/or SiC. The pre-coating is configured to prevent contamination of a substrate by materials from components of the processing chamber. As a more specific example, an SiO₂ pre-coating can be formed by introducing a Si-containing precursor gas (e.g., silane) in an oxygen-containing plasma.

[0076] Referring again to FIG. 2, after depositing the pre-coating, the method 200 comprises uncovering the electrostatic chuck at 206. FIG. 5C shows the processing tool 500 after pre-coating with the protective cover 504 removed. As illustrated in the example of FIG. 5C, the protective cover 504 prevents the pre-coating 508 from depositing on the substrate contact areas (SCAs) 507 of the ESC 502.

[0077] At 208, the method 200 of FIG. 1 comprises applying a HDP barrier coating to an electrostatic chuck of the HDP-CVD tool. FIG. 5D shows an example of a HDP barrier coating 510 on the substrate-facing surface of the ESC 502. In some examples, the HDP barrier coating 510 comprises a silicon oxide. Example silicon oxides include SiO₂, doped SiO₂ (e.g., fluorine-doped SiO₂), SiO_xN_y, SiO_xC_y, and/or

$\text{SiO}_x\text{C}_y\text{N}_z$. In other examples, the HDP barrier coating 510 comprises any other suitable material. Another example of a suitable HDP barrier coating material includes SiC.

[0078] In some examples, the finished HDP barrier coating 510 has a thickness 512 in a range of 1-5 microns. In some more specific examples, the thickness 512 is in a range of 3-5 microns. In yet more specific examples, the thickness 512 is in a range of 3-4.2 microns. In other examples, the HDP barrier coating 510 has any other suitable thickness. Other examples include thicknesses greater than 5 microns and less than 1 micron. A relatively thinner HDP barrier coating (e.g., less than 2.7 microns) may allow more metal contamination of a film being deposited on a substrate than a relatively thicker HDP barrier coating. Thus, a level of contaminants introduced into a substrate in HDP-CVD processing by the ESC may scale with HDP barrier coating thickness. However, the contaminant level may plateau once a threshold thickness (e.g., 5 microns) has been reached. Thus, increasing thickness beyond such a threshold thickness may provide little or no additional benefit for contamination protection. Furthermore, formation of a relatively thicker HDP barrier coating on the ESC takes more time than the formation of a relatively thinner HDP barrier coating on the ESC. If significant degradation rate is observed on the HDP barrier, having a thickness greater than 5 microns might be justified in certain applications.

[0079] The thickness 512 can be uniform across the substrate-facing surface 506. In some examples, the thickness 512 can have a peak-to-peak variation of less than or equal to 10% of an average value of the thickness 512. In some more specific examples, the thickness 512 can vary by 250 Å or less when the average value of the thickness 512 is 4000 Å. In other examples, the peak-to-peak variation is less than or equal to 1% of the average value of the thickness 512. In this manner, the HDP barrier coating 510 provides suitably uniform protection across an entire substrate when the substrate sits on the ESC 502. The uniform thickness of the HDP barrier coating also results in suitably uniform clamping force across the surface of the ESC 502.

[0080] As described above, HDP-CVD uses an inductively coupled plasma that provides for a higher ion flux at a substrate surface than a capacitively coupled plasma. As a result, the HDP barrier coating 510 can be denser than a film of similar composition deposited using a capacitively coupled plasma. In this manner, the HDP barrier coating 510 reduces/prevents diffusion or migration of metals from the ESC that could otherwise contaminate the substrate.

[0081] The HDP barrier coating 510 can be formed using any suitable process conditions. For example, depending upon a target thickness for the HDP barrier coating 510, the deposition of the HDP barrier coating can have a duration within a range of 10 seconds to 10 minutes. All ranges stated herein are inclusive of the endpoints. Further, in some examples, deposition of the HDP barrier coating 510 can take place at a pressure of about 10 millitorr (mTorr) including an inert gas in addition to the precursor gases for the HDP barrier coating. Example inert gases include helium (He), neon (Ne), argon (Ar), krypton (Kr), and/or xenon (Xe). In other examples, an inert gas is omitted.

[0082] In some examples, the HDP barrier coating 510 has a different composition and/or different physical properties than the pre-coating 508. This can be achieved by adjusting processing conditions between applying the pre-coating 508 and applying the HDP barrier coating 510 to the electrostatic chuck. Processing conditions that can be adjusted include the HF, MF, and LF RF power, substrate temperature, processing gas mixture composition, pressure, and gas flow rates. For example, the HDP barrier coating 510 can be formed in the presence of a higher concentration of Ar than the pre-coating 508. Ar is a relatively heavy gas. Argon ions in the plasma can impact the growing HDP barrier coating 510 with more kinetic energy than, for example, helium atoms. Bombarding the surface of the growing HDP barrier coating can increase the density of the HDP barrier coating. Thus, the use of a higher concentration of Ar for forming the HDP barrier coating 510 than for forming the pre-coat can form a higher density film for the HDP barrier coating 510 than for the pre-coating 508.

[0083] FIG. 3 shows a flow diagram depicting an example method 300 for processing a substrate. In some examples, the substrate is processed in the same tool (e.g., the HDP-CVD tool 100 of FIG. 1) that is used to deposit the HDP barrier coating. In other examples, the substrate is processed in a different tool at a same site or a different site than that used to deposit the HDP barrier coating.

[0084] At 310, the method 300 comprises placing a substrate on an ESC comprising an HDP barrier coating. The substrate can be placed on the ESC by a robot, such as robot 132. The method 300 further comprises, at 312, depositing an HDP film on the substrate using HDP-CVD. FIG. 5E shows an example of a substrate 514 on the ESC 502 of FIGS. 5A-5D. In the example of FIG. 5F, a HDP film 516 is deposited on the substrate 514.

[0085] In some examples, the substrate 514 comprises a base layer of an SOI wafer. In some such examples, the HDP film 516 comprises an oxide layer of the SOI wafer. FIG. 6 shows an example of an SOI wafer 600 that can be produced using the methods and processing tools described herein. FIG. 6 also shows an example of an FD-SOI device 602 that can be produced from the SOI wafer 600. The FD-SOI device 602 comprises a device layer 604 and an insulating layer 606 on a substrate 608. The device layer 604 comprises a source 610 and a drain 612 separated by a fully depleted channel region 614. The FD-SOI device 602 further comprises a gate 616 and a gate insulator 618. The insulating layer 606 can be silicon oxide formed using HDP-CVD, for example.

[0086] Referring again to FIG. 5F, in some examples, the HDP film 516 has a different composition and/or different physical properties (e.g., thickness, density, and/or electrical permittivity) than the HDP barrier coating 510 and/or the pre-coating 508. Some examples of suitable materials for the HDP film 516 include SiO₂ and fluorine-doped SiO₂. As described above, the different composition of the HDP film 516 can be achieved by adjusting the processing gas mixture between applying the pre-coating 508 and the HDP barrier coating 510.

[0087] In experiments, the presence of the HDP barrier coating resulted in a five-fold reduction in aluminum (Al) contamination in the HDP film from an AlN ESC relative to an HDP film deposited in the presence of a bare ESC. FIG. 7 shows an example chart of Al contents of an HDP film. As illustrated in FIG. 7, an HDP film deposited using a bare ESC had higher backside an in-film Al contamination than that deposited using an ESC with an HDP barrier coating.

[0088] Referring again to FIG. 3, steps 310 and 312 of the method 300 can be repeated for any suitable number of cycles 314 to deposit HDP films on a plurality of substrates. After a number of depositions of HDP films on substrates, the pre-coating and the HDP barrier coating can be removed and reapplied.

[0089] FIG. 4 shows a flow diagram depicting an example method 400 of operating a HDP-CVD tool, such as the HDP-CVD tool 100 of FIG. 1, to remove and reapply a HDP barrier coating. The method 400 comprises, at 416, removing the pre-coating and the HDP barrier coating after depositing an HDP film on a plurality of substrates. In some examples, the pre-coating and the HDP barrier coating are removed using a fluoride plasma. In other examples, any other suitable cleaning process can be used. Other examples of suitable cleaning processes include oxygen plasma cleaning

and hydrogen plasma cleaning. After the pre-coating and the HDP barrier coating are removed, a pre-coating and a new HDP barrier coating can be applied to the ESC.

[0090] The cleaning process used to remove the HDP barrier coating can also remove the pre-coating from the processing chamber. Accordingly, at 418, the method 400 comprises covering the ESC. At 420, the method 400 comprises optionally applying a new pre-coating. After applying the new pre-coating, the method 400 comprises forming a new HDP barrier coating at step 422. In this manner, the ESC can be cleaned and renewed for additional cycle(s) of substrate processing.

[0091] FIG. 8 shows a flow diagram depicting an example method 800 for operating an HDP-CVD device. The following description of the method 800 is provided with reference to FIGS. 1-7 above. It will be appreciated that the method 800 also can be performed in other contexts.

[0092] In some examples, at 802, the method 800 comprises, before applying an HDP barrier coating to an electrostatic chuck, covering the electrostatic chuck with a protective cover, applying a pre-coating to surfaces within a processing chamber of the HDP-CVD tool, and then uncovering the electrostatic chuck. For example, the ESC 502 of FIG. 5A is covered by protective cover 504. The protective cover 504 prevents accumulation of pre-coating 508 on substrate-contacting surfaces of the ESC 502.

[0093] At 804, in some examples, the method 800 comprises adjusting a processing gas mixture between applying the pre-coating and applying an HDP barrier coating to the electrostatic chuck. For example, the HDP barrier coating may be deposited using a more Ar-rich processing gas mixture than the pre-coating. This results in a heavier processing gas mixture and a denser HDP film.

[0094] The method 800 further comprises, at 806, applying a HDP barrier coating to the electrostatic chuck of the HDP-CVD tool. For example, the ESC 502 of FIG. 5D is coated with the HDP barrier coating 510. In some examples, at 808, the HDP barrier coating comprises one or more of silicon oxide, fluorine-doped silicon oxide, silicon oxynitride, silicon oxycarbide, silicon oxycarbonitride, or silicon carbide. This helps to prevent sputtering or migration of the ESC material during processing.

[0095] At 810, in some examples, depositing the HDP barrier coating comprises depositing an HDP barrier coating having a thickness of 3 microns to 5 microns. For example, the thickness 512 of the HDP barrier coating 510 of FIG. 5D can be in the range of 3 to 5 microns. A relatively thick HDP barrier coating may allow for production of a higher-purity product than the relatively thin HDP barrier coating.

However, the purity may plateau with increasing thickness (e.g., at a thickness of greater than 5 microns).

[0096] The method 800 further comprises, at 812, placing a substrate on the electrostatic chuck comprising the HDP barrier coating. For example, FIG. 5E shows an example of a substrate 514 provided on the ESC 502 and the HDP barrier coating 510.

[0097] At 814, the method 800 further comprises depositing an HDP film on the substrate using HDP-CVD. FIG. 5F shows an example HDP film 516 deposited on the substrate 514.

[0098] In some examples, at 816, depositing the HDP film on the substrate using HDP-CVD comprises forming an oxide layer in an SIO wafer fabrication process. For example, FIG. 6 shows an example of an FD-SOI device that includes an insulating layer 606. The insulating layer 606 can be formed by the processes and tools disclosed herein.

[0099] At 818, the method 800 optionally comprises, after depositing HDP oxide films on a plurality of substrates including the substrate, removing the pre-coating and the HDP-CVD barrier coating, and then applying a new pre-coating and a new HDP barrier coating on the electrostatic chuck. For example, the pre-coating and the HDP barrier coating 510 can be removed, the processing chamber 500 can be cleaned, and the pre-coating and the HDP barrier coating 510 can be rebuilt on the ESC 502.

[00100] In some examples, at 820, removing the HDP barrier coating comprises removing the HDP barrier coating using a fluoride plasma. In other examples, any other suitable cleaning technique can be used. For example, the processing chamber 102 of FIG. 1 can be cleaned using an oxygen plasma or a hydrogen plasma.

[00101] FIG. 9 schematically shows a non-limiting example of a computing system 900 that can enact one or more of the methods and processes described above. Computing system 900 is shown in simplified form. Computing system 900 can take the form of one or more personal computers, workstations, computers integrated with substrate processing tools, and/or network accessible server computers. %

[00102] Computing system 900 includes a logic machine 902 and a storage machine 904. Computing system 900 can optionally include a display subsystem 906, input subsystem 908, communication subsystem 910, and/or other components not shown in FIG. 9. Controller 134 is an example of computing system 900.

[00103] Logic machine 902 includes one or more physical devices configured to execute instructions. For example, the logic machine can be configured to execute instructions that are part of one or more applications, services, programs, routines, libraries, objects, components, data structures, or other logical constructs. Such instructions can be implemented to perform a task, implement a data type, transform the state of one or more components, achieve a technical effect, or otherwise arrive at a desired result.

[00104] The logic machine can include one or more processors configured to execute software instructions. Additionally or alternatively, the logic machine can include one or more hardware or firmware logic machines configured to execute hardware or firmware instructions. Processors of the logic machine can be single-core or multi-core, and the instructions executed thereon can be configured for sequential, parallel, and/or distributed processing. Individual components of the logic machine optionally can be distributed among two or more separate devices, which can be remotely located and/or configured for coordinated processing. Aspects of the logic machine can be virtualized and executed by remotely accessible, networked computing devices configured in a cloud-computing configuration.

[00105] Storage machine 904 includes one or more physical devices configured to hold instructions 912 executable by the logic machine to implement the methods and processes described herein. When such methods and processes are implemented, the state of storage machine 904 can be transformed—e.g., to hold different data.

[00106] Storage machine 904 can include removable and/or built-in devices. Storage machine 904 can include optical memory (e.g., CD, DVD, HD-DVD, Blu-Ray Disc, etc.), semiconductor memory (e.g., RAM, EPROM, EEPROM, etc.), and/or magnetic memory (e.g., hard-disk drive, floppy-disk drive, tape drive, MRAM, etc.), among others. Storage machine 904 can include volatile, nonvolatile, dynamic, static, read/write, read-only, random-access, sequential-access, location-addressable, file-addressable, and/or content-addressable devices.

[00107] It will be appreciated that storage machine 904 includes one or more physical devices. However, aspects of the instructions described herein alternatively can be propagated by a communication medium (e.g., an electromagnetic signal, an optical signal, etc.) that is not held by a physical device for a finite duration.

[00108] Aspects of logic machine 902 and storage machine 904 can be integrated together into one or more hardware-logic components. Such hardware-logic

components can include field-programmable gate arrays (FPGAs), program- and application-specific integrated circuits (ASIC / ASICs), program- and application-specific standard products (PSSP / ASSPs), system-on-a-chip (SOC), and complex programmable logic devices (CPLDs), for example.

[00109] When included, display subsystem 906 can be used to present a visual representation of data held by storage machine 904. This visual representation can take the form of a graphical user interface (GUI). As the herein described methods and processes change the data held by the storage machine, and thus transform the state of the storage machine, the state of display subsystem 906 can likewise be transformed to visually represent changes in the underlying data. Display subsystem 906 can include one or more display devices utilizing virtually any type of technology. Such display devices can be combined with logic machine 902 and/or storage machine 904 in a shared enclosure, or such display devices can be peripheral display devices.

[00110] When included, input subsystem 908 can comprise or interface with one or more user-input devices such as a keyboard, mouse, or touch screen. In some examples, the input subsystem can comprise or interface with selected natural user input (NUI) componentry. Such componentry can be integrated or peripheral, and the transduction and/or processing of input actions can be handled on- or off-board. Example NUI componentry can include a microphone for speech and/or voice recognition, and an infrared, color, stereoscopic, and/or depth camera for machine vision and/or gesture recognition.

[00111] When included, communication subsystem 910 can be configured to communicatively couple computing system 900 with one or more other computing devices. Communication subsystem 910 can include wired and/or wireless communication devices compatible with one or more different communication protocols. As non-limiting examples, the communication subsystem can be configured for communication using a wireless telephone network, or a wired or wireless local- or wide-area network. In some examples, the communication subsystem can allow computing system 900 to send and/or receive messages to and/or from other devices using a network such as the Internet.

[00112] This disclosure is presented by way of example and with reference to the associated drawing figures. Components, process steps, and other elements that can be substantially the same in one or more of the figures are identified coordinately and are described with minimal repetition. It will be noted, however, that elements

identified coordinately can also differ to some degree. It will be further noted that some figures can be schematic and not drawn to scale. The various drawing scales, aspect ratios, and numbers of components shown in the figures can be purposely distorted to make certain features or relationships easier to see.

[00113] “And/or” as used herein is defined as the inclusive or $\vee$, as specified by the following truth table:

A	B	$A \vee B$
True	True	True
True	False	True
False	True	True
False	False	False

[00114] The terminology “one or more of A or B” as used herein comprises A, B, or a combination of A and B. The terminology “one or more of A, B, or C” is equivalent to A, B, and/or C. As such, “one or more of A, B, or C” as used herein comprises A individually, B individually, C individually, a combination of A and B, a combination of A and C, a combination of B and C, or a combination of A, B and C.

[00115] It will be understood that the configurations and/or approaches described herein are example in nature, and that these specific examples or examples are not to be considered in a limiting sense, because numerous variations are possible. The specific routines or methods described herein can represent one or more of any number of strategies. As such, various acts illustrated and/or described can be performed in the sequence illustrated and/or described, in other sequences, in parallel, or omitted. Likewise, the order of the above-described processes can be changed.

[00116] The subject matter of the present disclosure includes all novel and non-obvious combinations and sub-combinations of the various processes, systems and configurations, and other features, functions, acts, and/or properties disclosed herein, as well as any and all equivalents thereof.

CLAIMS:

1. An electrostatic chuck, comprising:
a substrate-facing surface comprising one or more substrate contact areas; and
a high-density plasma (HDP) barrier coating on at least a portion of the one or more substrate contact areas.
2. The electrostatic chuck of claim 1, wherein the HDP barrier coating comprises one or more of silicon oxide, fluorine-doped silicon oxide, silicon oxynitride, silicon oxycarbide, silicon oxycarbonitride, or silicon carbide.
3. The electrostatic chuck of claim 1, wherein the HDP barrier coating has a thickness of 3 microns to 5 microns.
4. The electrostatic chuck of claim 1, wherein a peak-to-peak variation of a thickness of the HDP barrier coating is less than or equal to 10% of an average value of the thickness.
5. The electrostatic chuck of claim 1, wherein the electrostatic chuck comprises aluminum nitride.
6. A method of operating a vapor deposition tool, the method comprising:
placing a substrate on an electrostatic chuck comprising a high-density plasma (HDP) barrier coating; and
depositing an HDP film on the substrate using high-density plasma chemical vapor deposition (HDP-CVD).
7. The method of claim 6, wherein depositing the HDP film on the substrate using HDP-CVD comprises forming an oxide layer in a fully depleted silicon-on-insulator substrate fabrication process.
8. The method of claim 6, wherein the HDP barrier coating comprises one or more of silicon oxide, fluorine-doped silicon oxide, silicon oxynitride, silicon oxycarbide, silicon oxycarbonitride, or silicon carbide.

9. The method of claim 6, wherein the HDP barrier coating has a thickness of 3 microns to 5 microns.
10. The method of claim 6, further comprising, after depositing HDP oxide films on a plurality of substrates including the substrate, removing the pre-coating and the HDP barrier coating, and then applying a new pre-coating and a new HDP barrier coating on the electrostatic chuck.
11. The method of claim 10, wherein removing the pre-coating and the HDP barrier coating comprises removing the pre-coating and the HDP barrier coating using a fluoride plasma.
12. The method of claim 6, further comprising applying the HDP barrier coating to the electrostatic chuck using the vapor deposition tool.
13. The method of claim 12, further comprising adjusting a processing gas mixture before applying the HDP barrier coating.
14. A method of operating a high-density plasma (HDP) chemical vapor deposition (CVD) tool, the method comprising:
applying an HDP barrier coating to the electrostatic chuck.
15. The method of claim 14, further comprising, before applying the HDP barrier coating to the electrostatic chuck, covering a top surface of one or more substrate contact areas of the electrostatic chuck with a protective cover, applying a pre-coating to surfaces within a processing chamber of the HDP-CVD tool, and then uncovering the top surface of the one or more substrate contact areas of the electrostatic chuck.
16. The method of claim 15, further comprising adjusting a processing gas mixture between applying the pre-coating and applying the HDP barrier coating to the electrostatic chuck.

17. The method of claim 14, wherein the HDP barrier coating comprises one or more of silicon oxide, fluorine-doped silicon oxide, silicon oxynitride, silicon oxycarbide, silicon oxycarbonitride, or silicon carbide.

18. The method of claim 14, wherein depositing the HDP barrier coating comprises depositing an HDP barrier coating having a thickness of 3 microns to 5 microns.

19. The method of claim 14, further comprising removing the HDP barrier coating, and then applying a new HDP barrier coating on the electrostatic chuck.

20. The method of claim 19, wherein removing the HDP barrier coating comprises removing the HDP barrier coating using a fluoride plasma.