Description

Memory element for a semiconductor memory device

The invention relates to a memory element for a semiconductor memory device as claimed in the preamble of claim 1.

Memory elements are known for semiconductor memory devices, in which a change is made from the basic structure, comprising a storage capacitor and a selection transistor that is physically isolated from it, for information storage.

In memory elements such as these for semiconductor memory devices, a number of line devices are provided which are essentially electrically insulated from one another in pairs, are formed in a semiconductor substrate of a first conductance type or in a surface area thereof and are at least partially formed and arranged physically separated from one another in pairs by means of an intermediate area of the semiconductor substrate. Furthermore, an isolation area is provided there, which is composed of an essentially electrically insulating material which makes mechanical and electrical contact with the intermediate area, and in each case with an overlap area of each line device. In this case, by applying to the line devices, in particular to their overlap areas, and to the isolation area an electrical potential distribution in the isolation area in accordance with an information unit that is to be stored, it is possible at least temporarily to form at least one area with changed electrical and/or magnetic characteristics.

Conventional memory elements of this type are subject to the problem that the isolation area allows only an

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essentially physically cohesive change to the electrical and/or magnetic characteristics in the isolation area, so that it is impossible to satisfactorily ensure strict physical isolation between the stored information contents, or information contents to be stored, and hence crosstalk between information contents which need to be distinguished, for example a number of bits.

The invention is based on the object of developing a memory element for a semiconductor memory device of the type mentioned initially, so as to ensure adequate discrimination between stored information contents in the memory element, in a simple manner.

In the case of a memory element for a semiconductor memory device of the type mentioned initially, the invention is achieved according to the invention by the distinguishing features of claim 1. Advantageous developments of the memory element according to the invention are the subject matter of the dependent subclaims.

The memory element according to the invention for a semiconductor memory device, in particular a multibit memory cell or the like, is distinguished in that a number of material areas which are isolated from one another are provided in order to form the at least one area with changed or changeable electrical and/or magnetic characteristics in the isolation area, and in that the material areas have essentially free charge carriers, and/or free charge carriers can be formed in the material areas.

One basic idea of the present invention is thus to simplify and to assist the formation of changed electrical and/or magnetic characteristics in the

isolation area by providing a number of material areas in the isolation area, which have free charge carriers and/or in which free charge carriers can be formed. This means that the electrical characteristics or magnetic characteristics can be formed comparatively easily, that is to say with relatively small electrical potentials in the physically isolated material areas. In the process, local application results in the respectively provided information content also remaining in a local manner in the isolation area. Furthermore, further localization and hence avoidance of crosstalk are provided by the isolation of the number of material areas with respect to or from one another, with this isolation being provided, if appropriate, simply by physical separation.

For this purpose, the invention advantageously provides for the material areas to be embedded in the isolation area.

Particularly highly localized structures are obtained if nanodots or the like are provided as the material areas. The expression nanodots means very small islands of a material B in a matrix composed of a material A. Alternatively, it is also feasible for a localized area B to be formed within the material A, with this area B having significantly changed electrical characteristics, for example as a result of severe damage to the material A.

The major characteristic of the material areas in the isolation area is the presence of essentially free charge carriers, or the capability to be able to form essentially free charge carriers in the material of the material areas in the isolation area. It is thus particularly advantageous for the material areas in the isolation area to have a metal, a semiconductor

material, in particular silicon, germanium and/or the like, possibly in an appropriately doped form, or to be formed from such a material.

It is advantageous, but not essential, for the material areas in the isolation area each to be formed essentially identically. This relates both to the geometric characteristics and to the electrical and/or magnetic characteristics of the material areas, and of the material on which these material areas are based.

The material areas in the isolation area may be formed in widely differing ways. For example, it is possible for the material areas of the isolation area to be formed or deposited as material areas which are deposited, but not all the way through, on a first insulator layer of the isolation area, and which are then embedded in a second insulator layer of the isolation area.

On the other hand, the material areas of the isolation area may also be in the form of implantation regions in the isolation area.

If required, it is possible to carry out heat-treatment at comparatively high temperatures after forming the actual material areas in the isolation area, by which means the corresponding material areas can be further reduced in size by means of an appropriate oxidation process, in order in this way to improve the information localization and the crosstalk behavior further.

In principle, it is feasible for the material areas and, in particular, the nanodots to be formed over the entire isolation area. However, it is particularly advantageous, according to a further preferred

embodiment of the memory element according to the invention, for the material areas to be formed in regions or areas of the isolation area which are physically isolated from one another and, in particular, in the immediate physical vicinity of the overlap areas of the respective line devices. This means that the isolation area, and the material areas or nanodots provided there, are accessed only in these areas in the immediate physical vicinity of the overlap areas of the respective line devices, thus allowing local formation, deletion and/or reading of information contents in the isolation area. These characteristics in principle make it possible to form the isolation area with a large number of information units, for example with n bits.

In order to control the writing to, deletion and/or reading from the memory element according to the invention, a control line device is provided which is essentially electrically isolated from the line devices, and control potential distribution can be applied locally or globally to the isolation area by means of the control line device. This measure improves the influence of, and/or increases the possibility of influencing the formation, changing and/or sampling of the electrical and/or magnetic characteristics of the material areas of the isolation area.

In this case, the invention provides in particular for the line devices and, in particular, the overlap areas between them each to form a field effect transistor element in pairs with that section of the intermediate area which is in each case provided between them. The invention furthermore provides in this case for this element combination, as a field effect transistor element, to in each case be controllable by the control line device as the gate connection and the isolation

area as the gate insulation.

It is particularly advantageous for the areas whose electrical and/or magnetic characteristics can be varied to in each case be formed by a cohesive group of material areas, and, in particular by a cohesive group of nanodots. This further improves the localization of the information units, and hence the crosstalk.

In this case, the invention provides in particular for one area of the isolation area to be formed, in each case, for storage of one information unit, that is to say for example of one bit.

The processes of writing to, deletion and/or reading of the information contents or units is particularly advantageous if the areas can be written to, read from and/or deleted by means of high-energy or hot charge carriers with respect to the information unit.

The invention will be explained in more detail in the following text using the following comments:

More bits per cell can be stored in flash memory cells since different charge states are stored or since one bit is in each case stored at physically separate locations.

For the purposes of this invention, an alternative cell concept is proposed for storage of two or more bits at different locations in one memory cell.

Until now, it has been possible to store two bits in one flash cell either by using silicon spacer technology or by using an Si_3N_4 layer in the NROM concept.

Instead of a floating gate all the way through, silicon nanocrystals, which are embedded in a silicon dioxide matrix, are used for storing charge according to the invention. These are normally programmed and deleted by direct tunnels or by Fowler-Nordheim tunnels.

If a cell such as this is programmed using hot electrons, then independent programming can be achieved at both ends of the cell and, for example, it is possible to store two bits per cell.

In contrast to the NROM concept, in which silicon nitride is used as the memory layer, this results in an additional degree of freedom due to the choice of the silicon nanodots. If the size of and separation between the dots are selected appropriately, the lateral charge loss can thus be minimized.

A number of methods are feasible for producing and hence for selecting the size and density of the silicon nanodots. First of all, once a thin oxide has been produced, a silicon layer which does not pass all the way through can be deposited, and can then be covered with a further silicon oxide layer.

The density and the size of the silicon dots are selected by suitable choice of the deposition conditions for the silicon deposition. Alternatively, the entire silicon dioxide layer can be applied, and the silicon islands can then be produced by silicon implantation - the implantation of a different semiconductor, for example of germanium, is also feasible as an alternative. The position and orientation, size and density of silicon dots are selected for example, by means of the appropriate energy, dose and ion flow for the implantation, and by the conditions in the subsequent heat treatment. In

both production versions, the size of the silicon dots is reduced, thus achieving fine tuning, by subsequent thermal oxidation at a low temperature.

The inventive ideas lie in the combination of flash memory cells with silicon nanodots with the programming and deletion method using hot electrons or using hot holes. If the silicon dots can be produced only at the source ends and drain ends of the component, deletion from the silicon dots is alternatively also possible by means of Fowler-Nordheim tunnels.

A further idea is to select the density and size of the nanodots in order to minimize the lateral charge loss and the nonuniform charging of the dots during writing and deletion.

As has already been mentioned, the memory elements according to the invention are programmed by means of hot charge carriers, in particular electrons, and are deleted by means of hot holes. The stored information in the respective memory elements is read in the opposite direction to programming (reverse read).

The following table illustrates by way of example the potential ratios for two-bit cells to be applied during writing, deletion and/or reading:

	S/D connection 1	S/D connection 2	Control Gate
Programme bit #1	0 V	approx. 4-6 V	approx. 9 V
Programme bit #2	approx. 4-6 V	0 V	approx. 9 V
Read bit #1	approx. 1-2 V	0 V	approx. 2-3 V
Read bit #2	0 V	approx. 1-2 V	approx. 2-3 V
Delete bit #1	floating	approx. 9 V	0 V
Delete bit #2	approx. 9 V	floating	0 V
Alternatively			
Delete bit #1	floating	approx. 5 V	-5 V
Delete bit #2	approx. 5 V	floating	-5 V

The invention will be explained in more detail in the following text with reference to a schematic drawing, on the basis of preferred embodiments of the memory element according to the invention.

Figures 1, 2 show, in the form of a cross-sectional view and a plan view, two embodiments of the memory element according to the invention.

Figure 1 shows, in a schematic and side cross-sectional view, a first embodiment of a memory element 1 according to the invention.

A first line device BL1 with an end area SD1 is formed in the area of a surface 20a in a semiconductor substrate 20 with said surface area 20a. A second line device BL2, with an end area SD2 which is opposite the first end area SD1 of the first line device BL1, is provided in the surface area 20a of the semiconductor substrate 20, separated physically and by material by means of an intermediate area K from the end area SD1

of the first line device BL1.

The actual isolation area GOX is formed above the intermediate area K, and thus above the surface area 20a of the semiconductor substrate 20. A number of material areas N are in each case provided in this isolation area GOX, adjacent to the end areas SD1 and SD2, respectively, of the first and second line devices BL1, BL2, the electrical and/or magnetic characteristics of these material areas N can be varied, and, in particular, they are in the form of so called nanodots.

A control connection line G which is itself embedded in an isolation area 30, is formed on the side of the isolation area GOX facing away from the end areas SD1 and SD2 of the first and second line devices BL1 and BL2.

The arrangement which is shown in Figure 1 results in the end areas SD1 and SD2 of the first line device BL1 and of the second line device BL2, which are separated from one another physically and by material by means of the intermediate area K of the semiconductor substrate 20, forming source/drain areas SD1 and SD2 as overlap areas Ü1 and Ü2 with respect to the isolation area GOX, which is used as a gate isolation area or gate oxide. The control line device G thus acts as a gate connection.

Although, in principle, the entire isolation area GOX can be formed using nanodots N, only two areas B1 and B2 in the isolation area GOX are each provided with nanodots N in the embodiment shown in Figure 1, and are used to form corresponding, cohesive nanodot regions or groups N1 and N2. Further nanodots N are indicated by dots in the central area Z of the isolation area GOX.

The information contents in the isolation area GOX can be appropriately programmed or written to, deleted and/or read from by appropriate application of a potential distribution to the line devices BL1, BL2 and G1 respectively as the first and second source/drain connections and as the gate connection. In this case, the regions B1 and B2 each act as a memory area for one bit, namely for a bit 1 and for a bit 2. The above description of the writing, deletion and/or reading processes relates to the arrangement shown in Figure 1.

Figure 2 shows a plan view of another embodiment of a memory element 1 according to the invention.

The control line device G, that is to say the gate connection, is omitted in the view in Figure 2. The figure shows the outline of a square isolation area GOX. This isolation area GOX is accessed by four line devices BL1, ..., BL4. The overlap areas $\ddot{U}1$, ..., $\ddot{U}4$ or source/drain areas SD1, ..., SD4 of the line devices BL1, ..., BL4 are represented by dashed-dotted lines on the edge of the isolation area GOX which overlap with corresponding nanodot regions N1, ..., N4 each of a number of nanodots N, with the latter being used as areas B1, ..., B4 whose electrical and/or magnetic characteristics can be varied and which are themselves suitable for storage of four individual bits, Bit1 to Bit4.

In principle, other arrangements with a number of line devices BL1, ..., BL4 are also feasible, with n being the number of line devices or bit lines. In other words, the most preferred exemplary embodiment of the invention is based on a memory cell with two line devices or connections. However, in general, n line devices BL1, ..., BLn are also possible, where n is ≥ 2

and n may assume the value 4, purely by way of example, or any other magnitude.

List of reference symbols

1	Memory element
20	Semiconductor substrate
20a	Surface area
30	Isolation area
B1-4	Area with variable electrical/magnetic characteristics
BL1-4	Line device, bit line
G	Gate connection, control line device
GOX	Isolation area, gate oxide
K	Intermediate area, channel path
K12-34	Channel path
N	Material area, nanodot
N1-4	Group of material areas, nanodot group
SD1-4	End area, source/drain area
Ü1-4	Overlap area
Z	Additional nanodots

Patent Claims

1. A memory element for a semiconductor memory device, in particular a multibit memory cell or the like,

- having a number of line devices (BL1, ..., BL4), which are essentially electrically insulated from one another in pairs, are formed in a semiconductor substrate (20) of a first conductance type or in a surface area (20a) thereof and are at least partially formed and arranged physically separated from one another in pairs by means of an intermediate area (K) of the semiconductor substrate (20), and
- having an isolation area (GOX) composed of an essentially electrically insulating material, which makes mechanical and electrical contact with the intermediate areas (K) and with in each case one overlap area (Ü1, ..., Ü4) of each line device (BL1, ..., BL4),
- in which, by applying to the line devices (BL1, ..., BL4) in particular to their overlap areas (Ü1, ..., Ü4), and to the isolation area (GOX) an electrical potential distribution in the isolation area (GOX) in accordance with an information unit that is to be stored, it is possible at least temporarily to form at least one area (B1, ..., B4) with changed electrical and/or magnetic characteristics,

wherein

- a number of material areas (N) which are isolated from one another are provided in order to form the at least one area (B1, ..., B4) with changed electrical and/or magnetic characteristics in the isolation area (GOX), and
- each of the material areas (N) has free charge carriers, and/or free charge carriers can be

formed in each of the material areas (N).

2. The memory element as claimed in Claim 1, wherein the material areas (N) are embedded in the isolation area (GOX).

3. The memory element as claimed in one of the preceding claims, wherein the material areas (N) are in the form of nanodots or the like.

4. The memory element as claimed in one of the preceding claims, wherein the material areas (N) have or are formed from a metal, a semiconductor material, in particular silicon, germanium and/or the like, possibly with appropriate doping.

5. The memory element as claimed in one of the preceding claims, wherein the material areas (N) are formed essentially identically.

6. The memory element as claimed in one of the preceding claims, wherein the material areas (N) are in the form of material areas (N) which are deposited, but not all the way through, on a first insulator layer, and are then embedded in a second insulator layer.

7. The memory element as claimed in one of the preceding claims,

wherein
the material areas (N) are in the form of implantation regions in the isolation area (GOX).

8. The memory element as claimed in one of the preceding claims,
wherein
the material areas (N) are formed in regions or areas (B1, ..., B4) of the isolation area (GOX) which are physically isolated from one another, in particular in the immediate physical vicinity of the overlap areas (Ü1, ..., Ü4) of the respective line device (BL1, ..., BL4).

9. The memory element as claimed in one of the preceding claims,
wherein
- a control line device (G) is provided which is essentially electrically isolated from the line devices (BL1, ..., BL4), and
- a control potential distribution can be applied locally or globally to the isolation area (GOX) by means of the control line device (G).

10. The memory element as claimed in one of the preceding claims,
wherein
the line devices (BL1, ..., BL4) and, in particular, the overlap areas (Ü1, ..., Ü4) of them each form a field effect transistor element in pairs with the sections (K12, K13, K14, K23, K34) of the intermediate area (K) which are in each case provided between them, which field effect transistor element can in each case be controlled in particular by the control line device (G) as the gate connection and the isolation area (GOX) as the gate insulation.

11. The memory element as claimed in one of the preceding claims,
wherein
the areas (B1, ..., B4) whose electrical and/or magnetic characteristics can be varied are each formed by a cohesive group (N1, ..., N4) of material areas (N) of the isolation area (GOX) and, in particular, by a number of nanodots.

12. The method as claimed in one of the preceding claims,
wherein
the areas ((B1, ..., B4) of the isolation area (GOX) are each designed to store one information unit, in particular one bit.

13. The method as claimed in Claim 12,
wherein
the areas (B1, ..., B4) of the isolation area (GOX) can be written to, deleted and/or read from by means of high-energy or hot charge carriers with respect to the information unit.