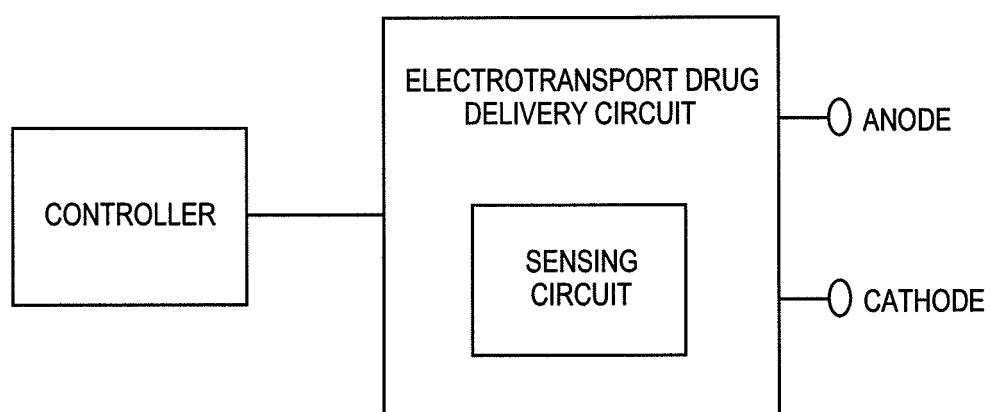
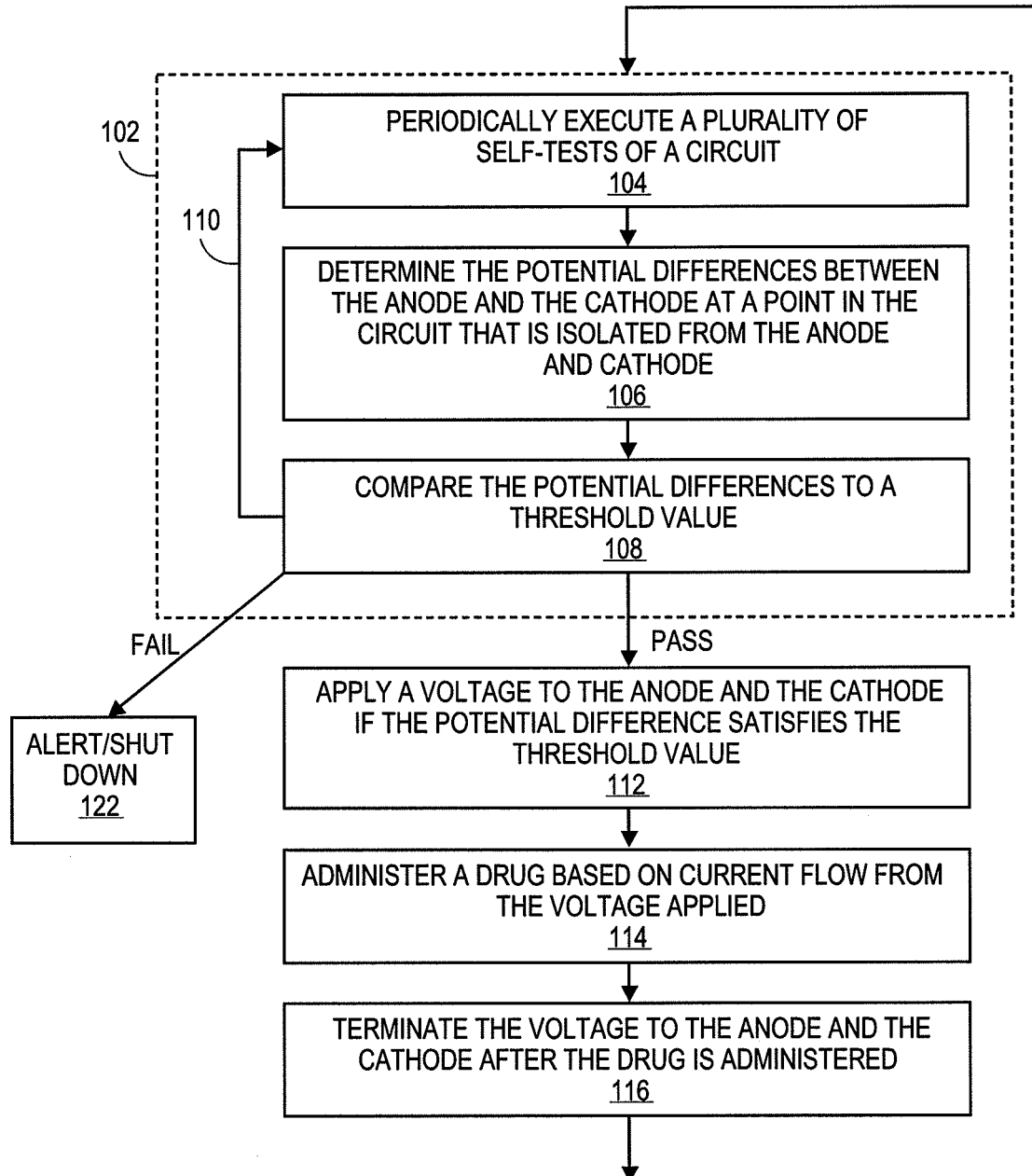


**FIG. 1A**

**FIG. 1B**

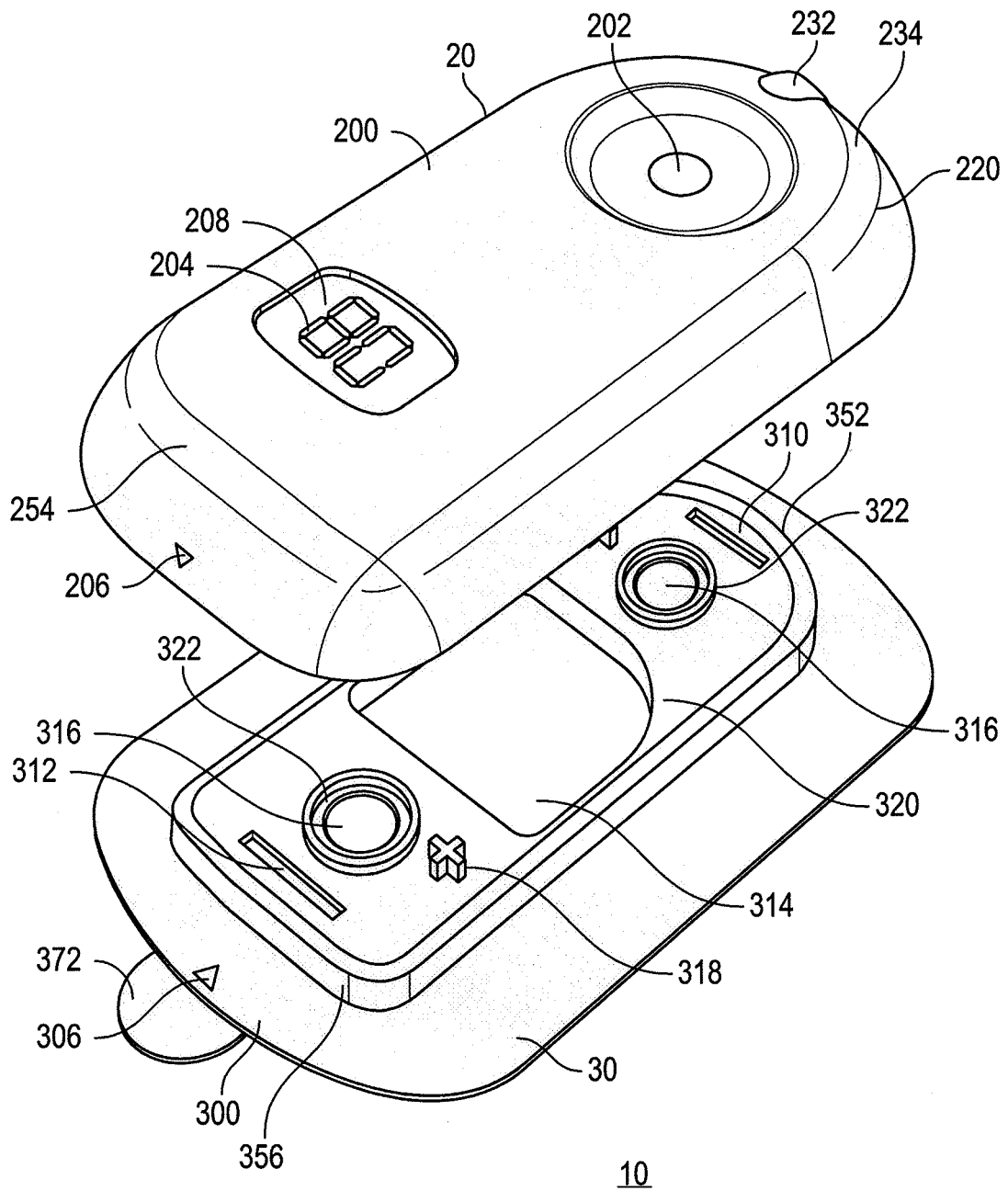


FIG. 2A

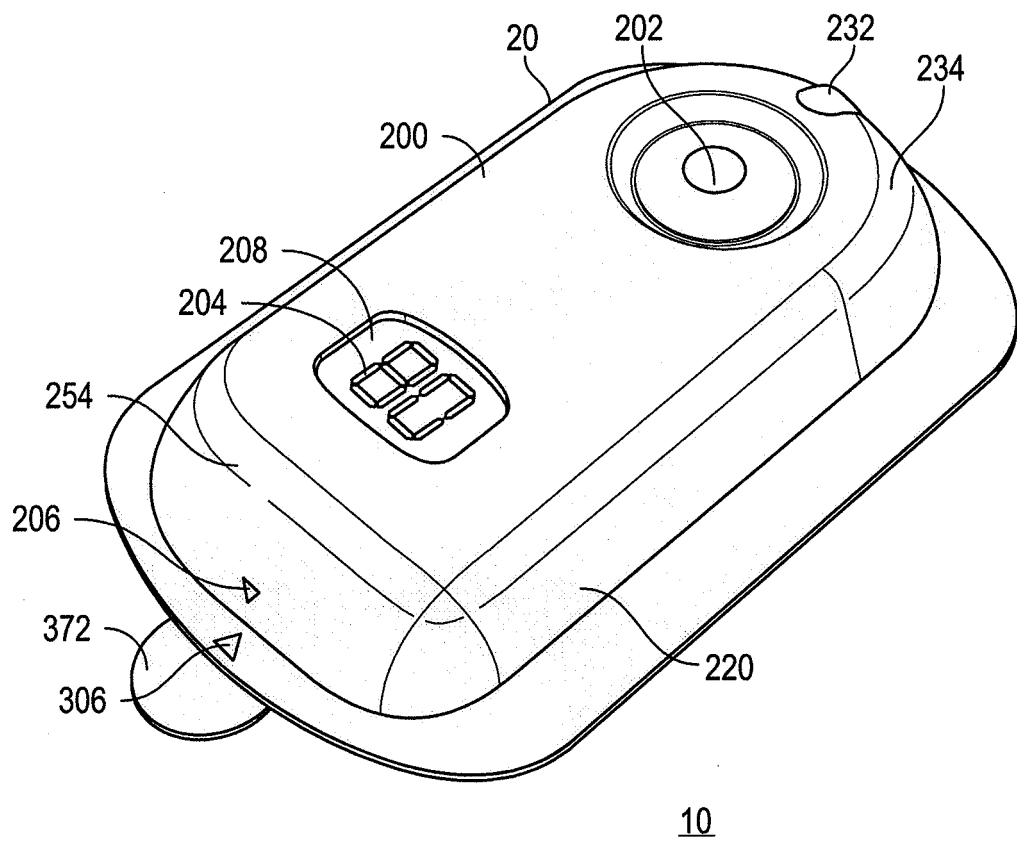


FIG. 2B

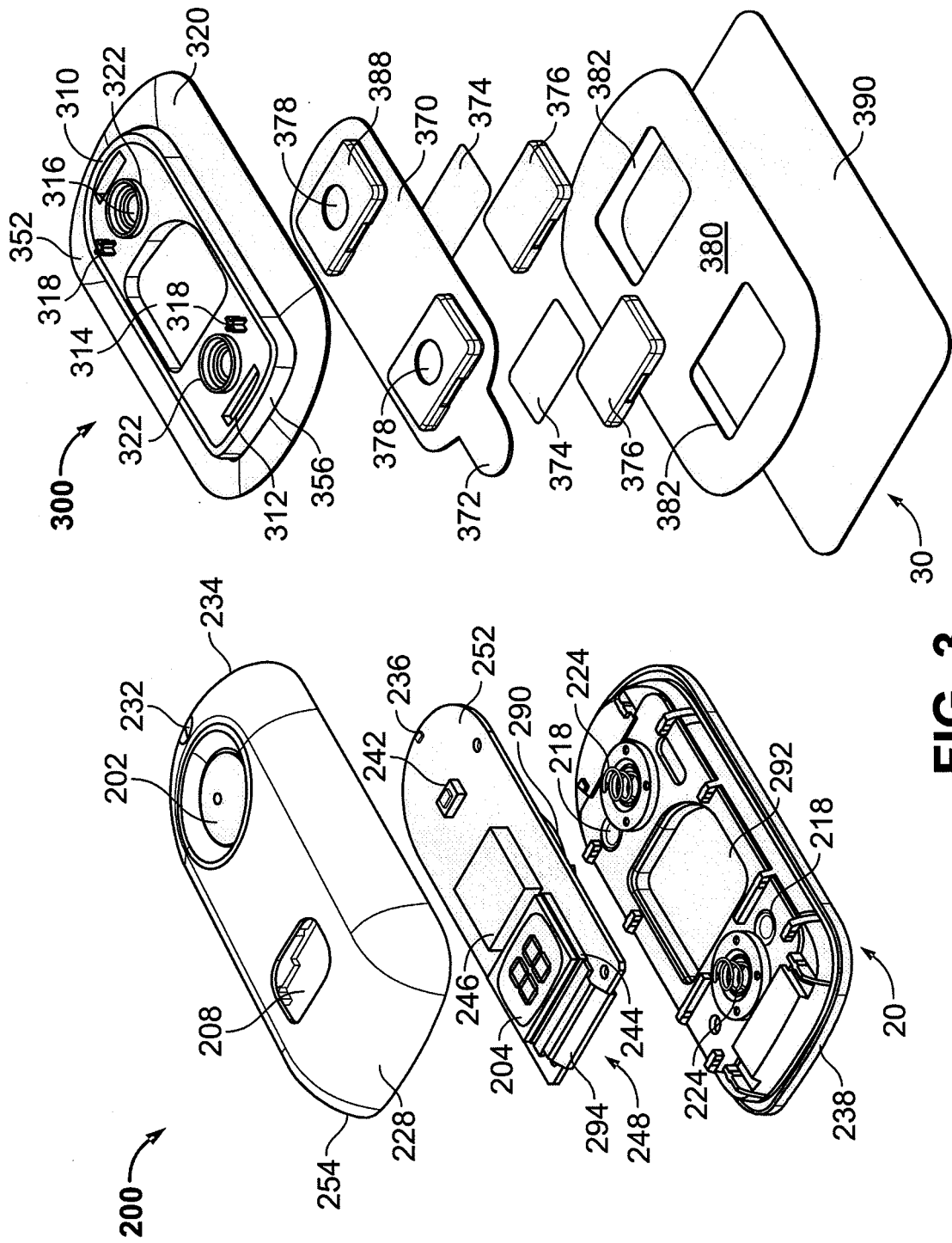


FIG. 3

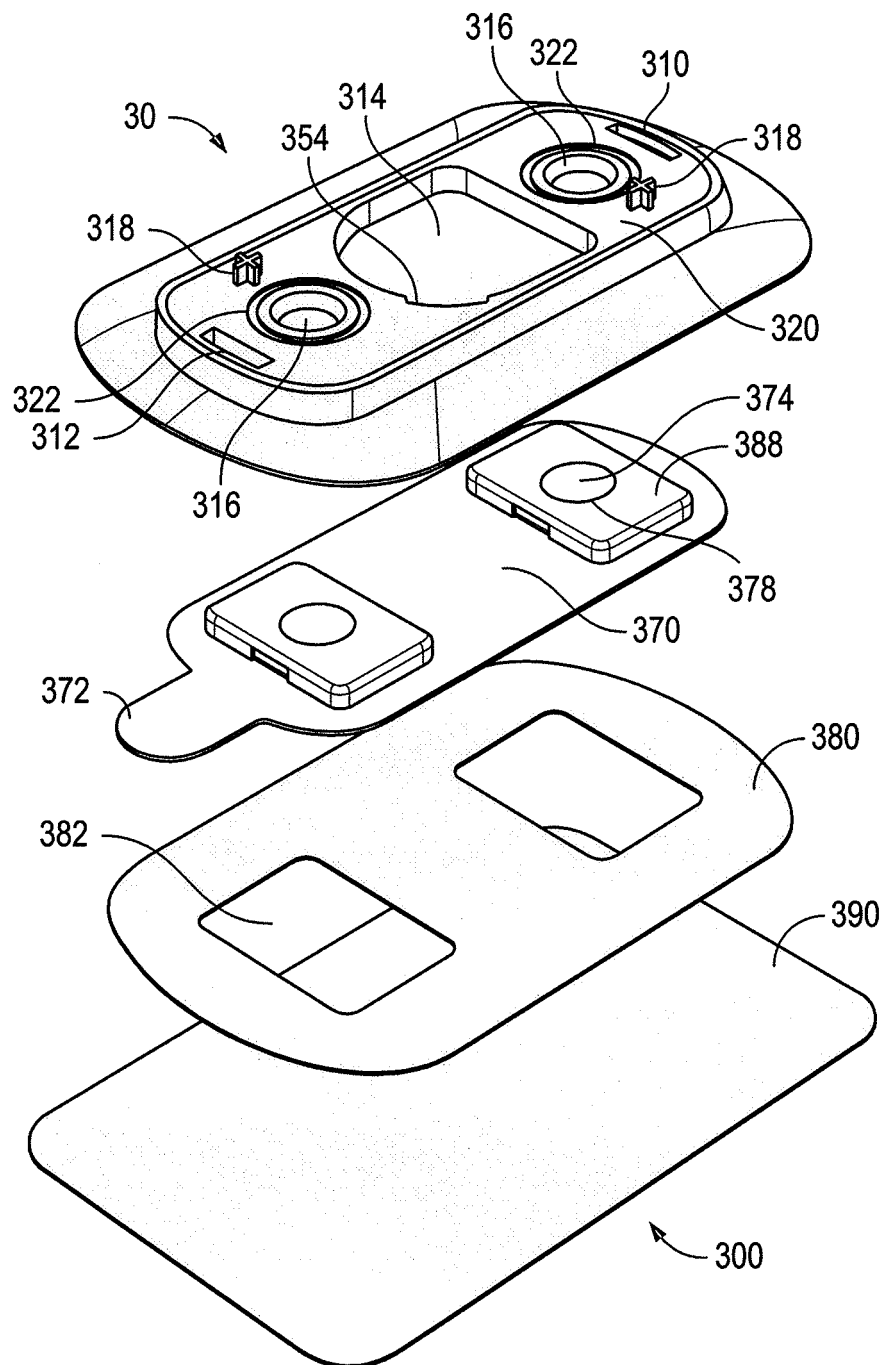


FIG. 4

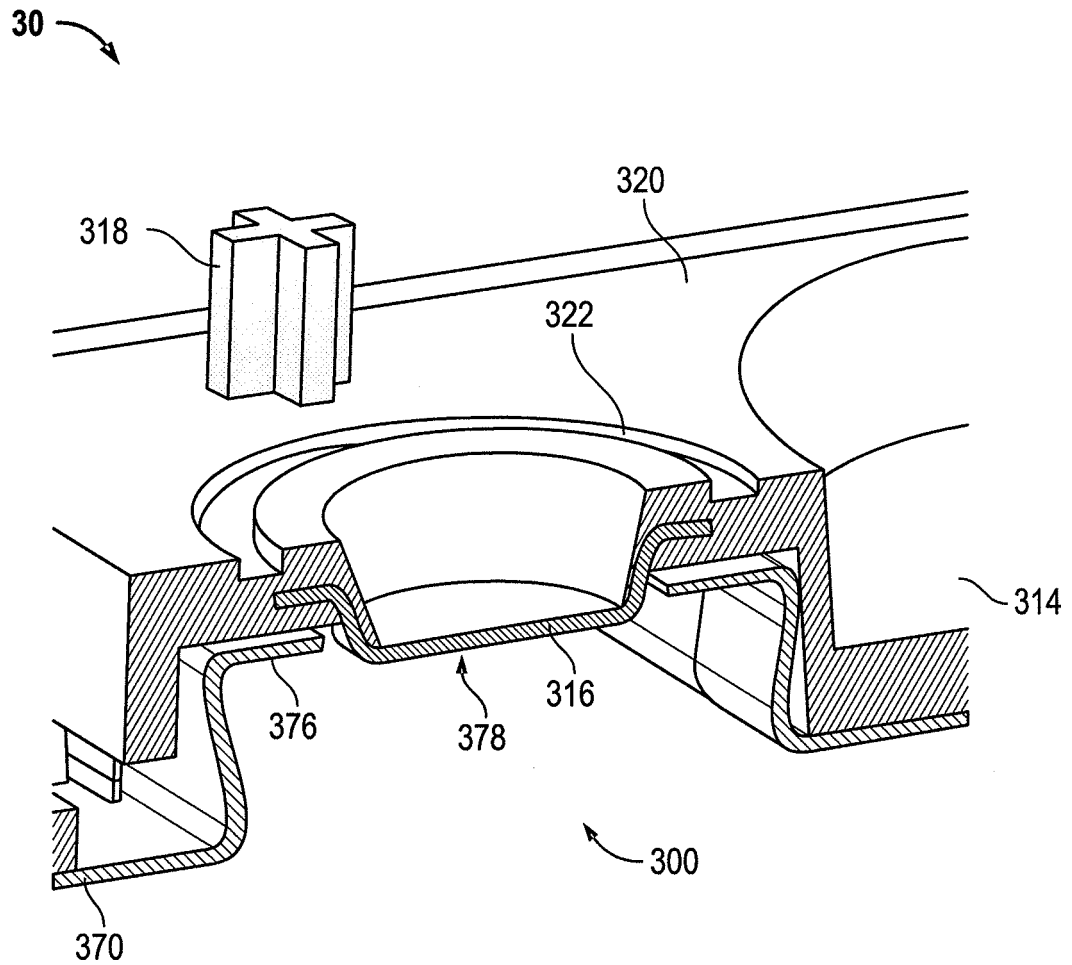


FIG. 5

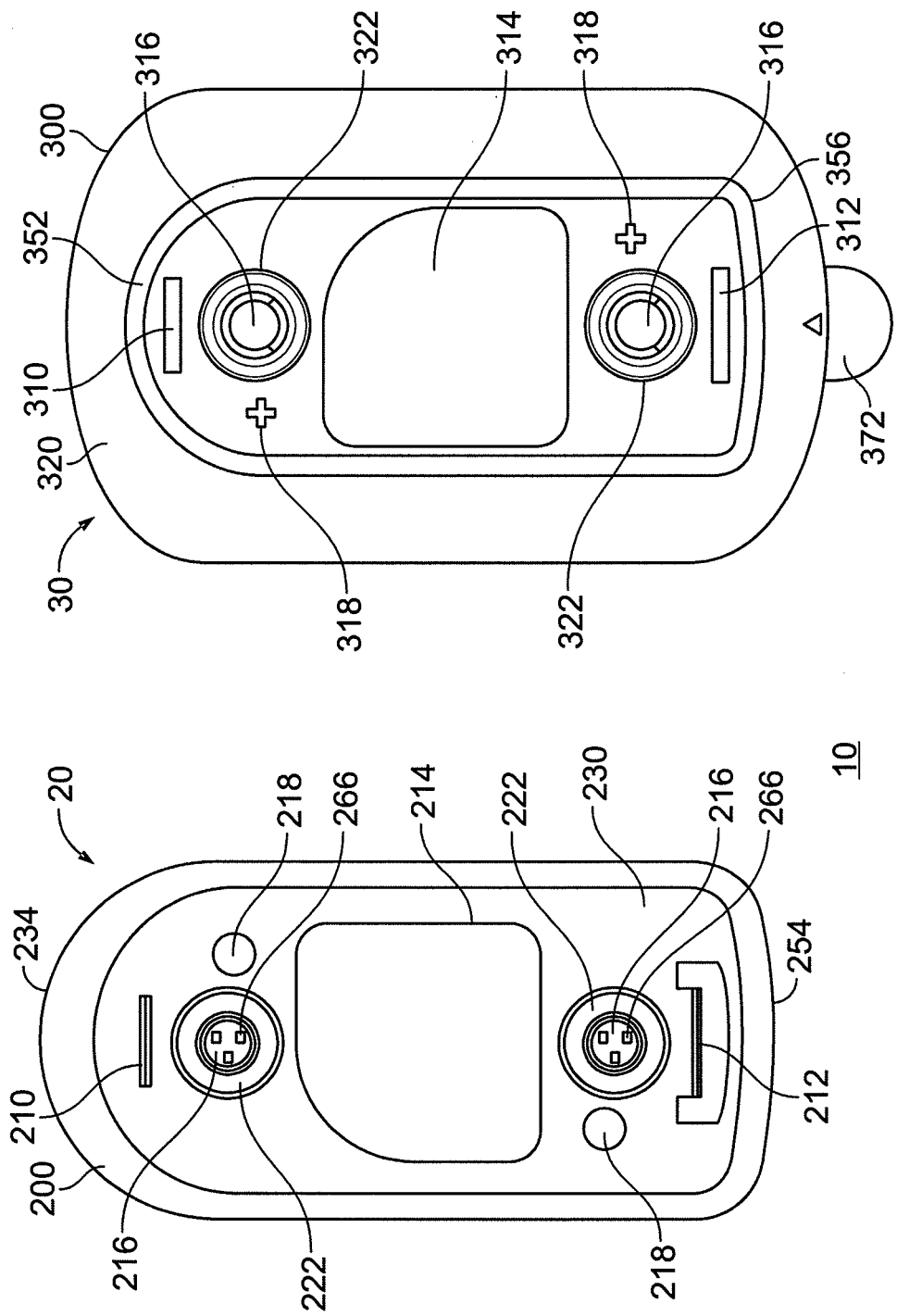


FIG. 6

FIG. 9

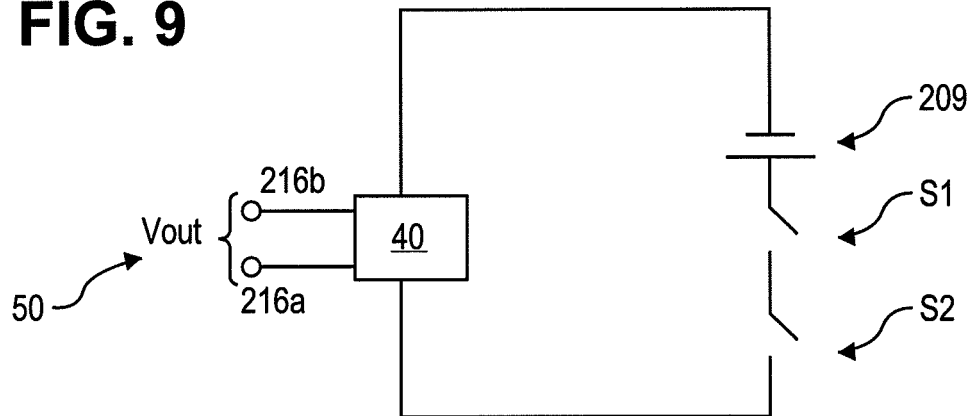


FIG. 7A

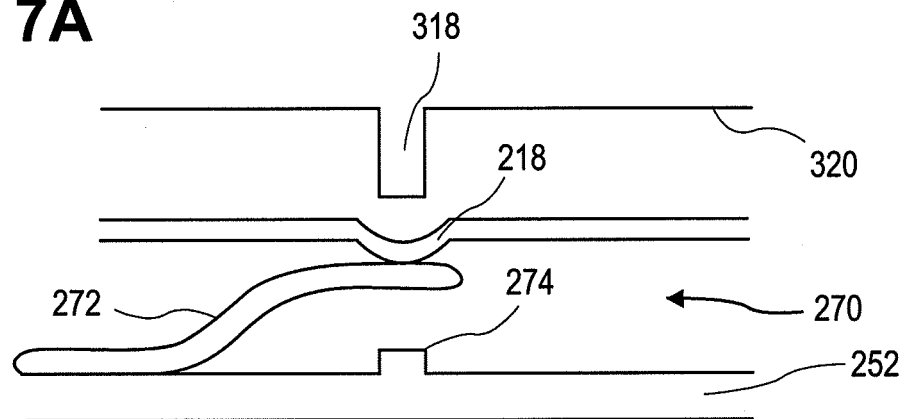
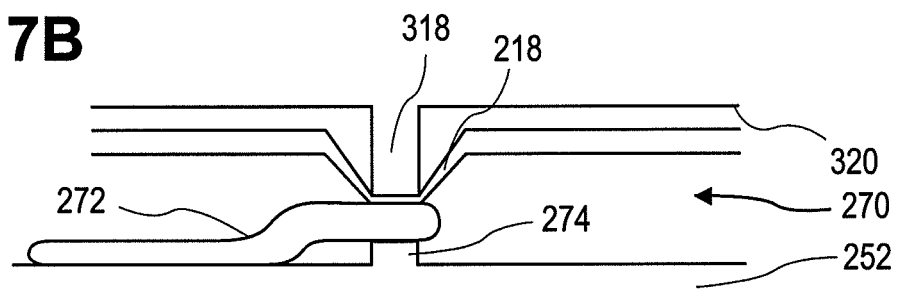


FIG. 7B



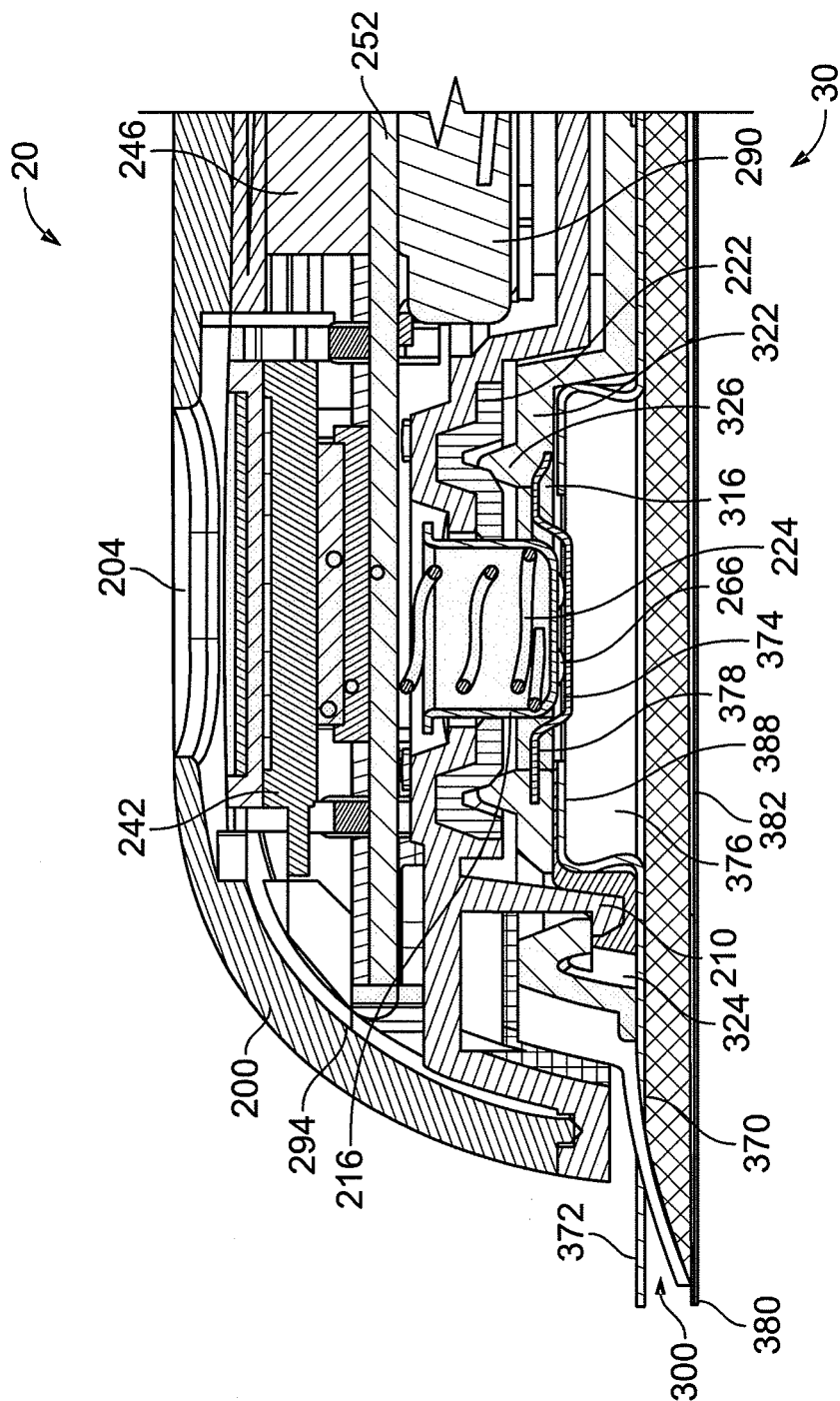
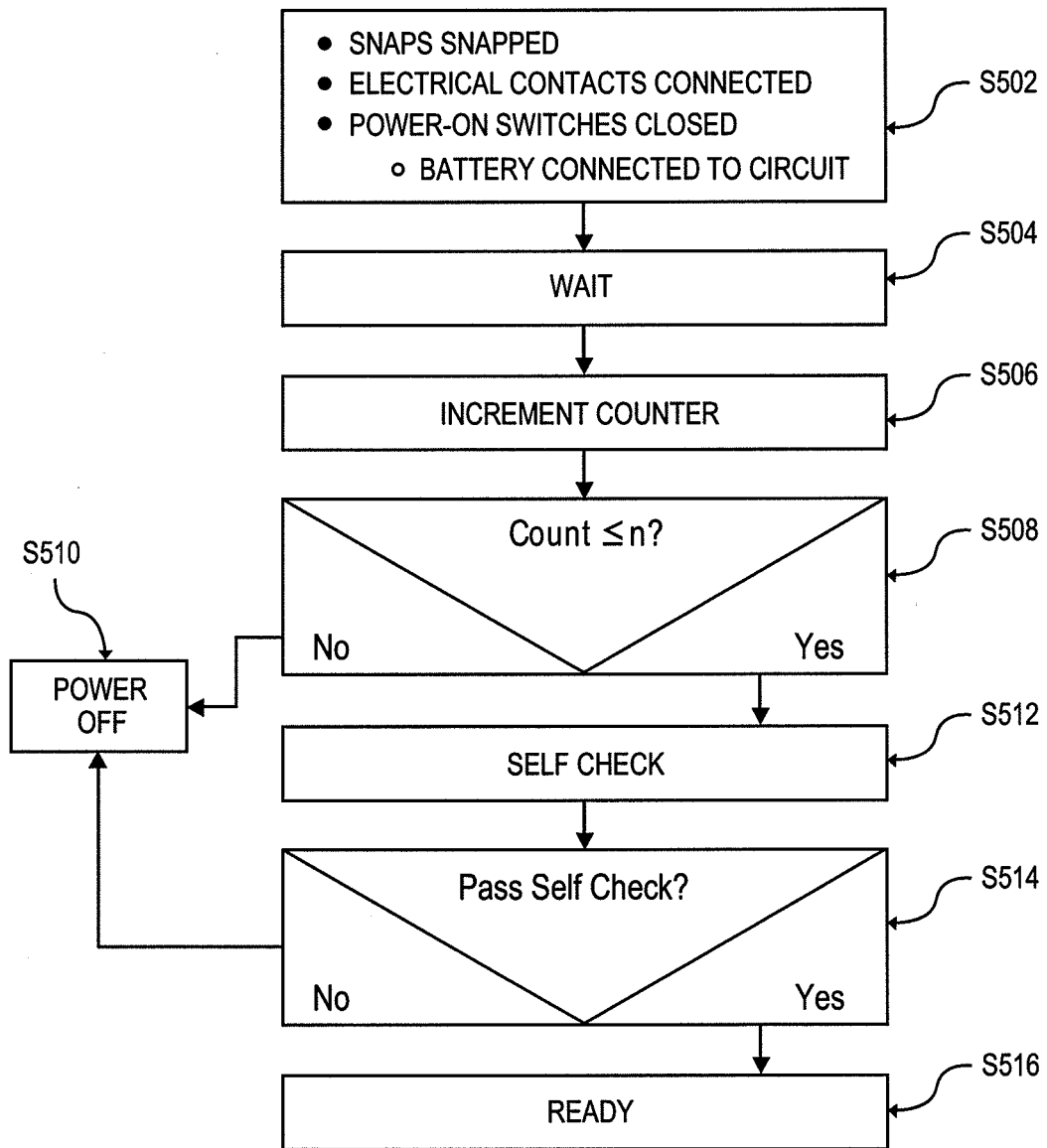
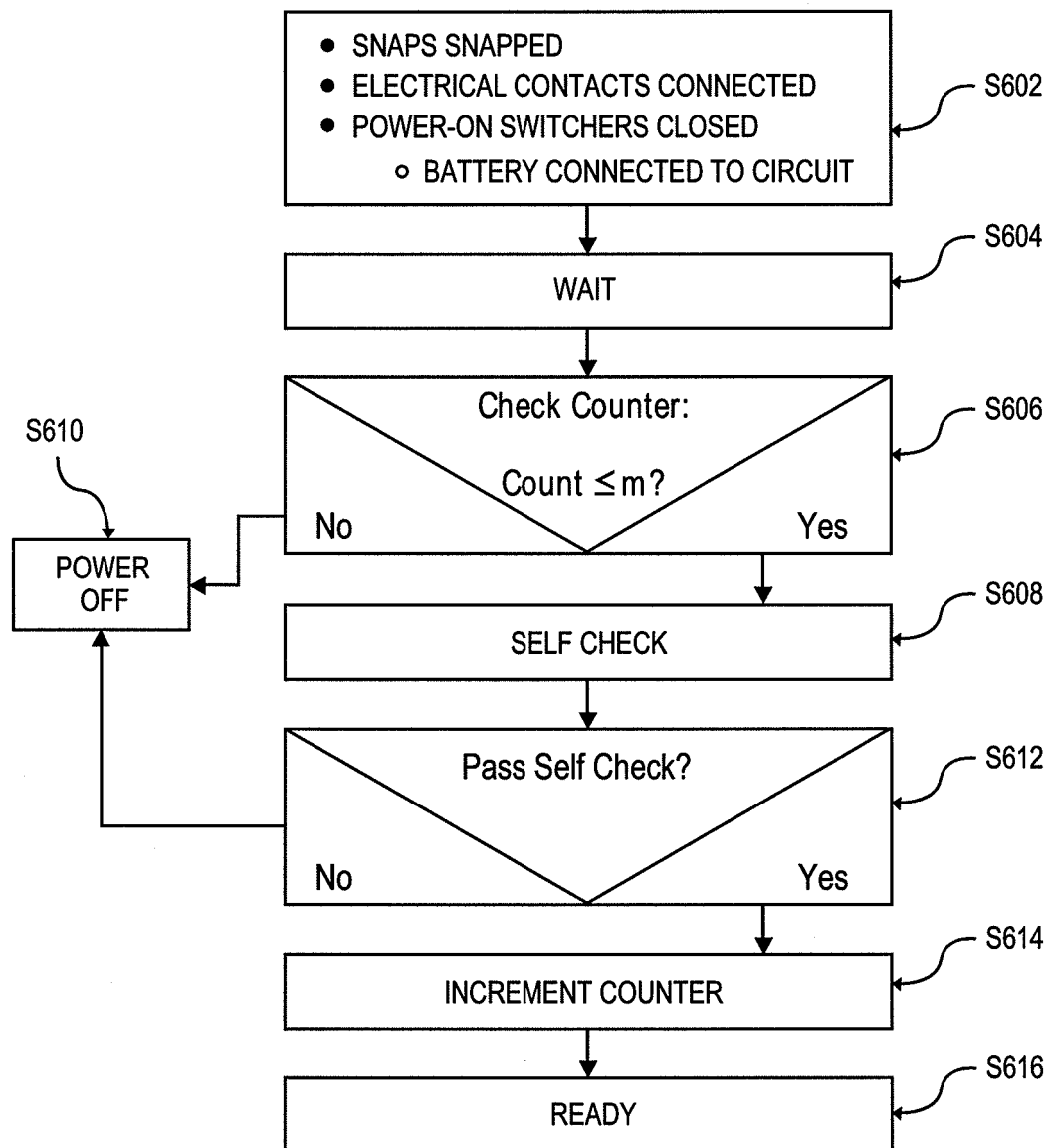


FIG. 8

**FIG. 10**

**FIG. 11**

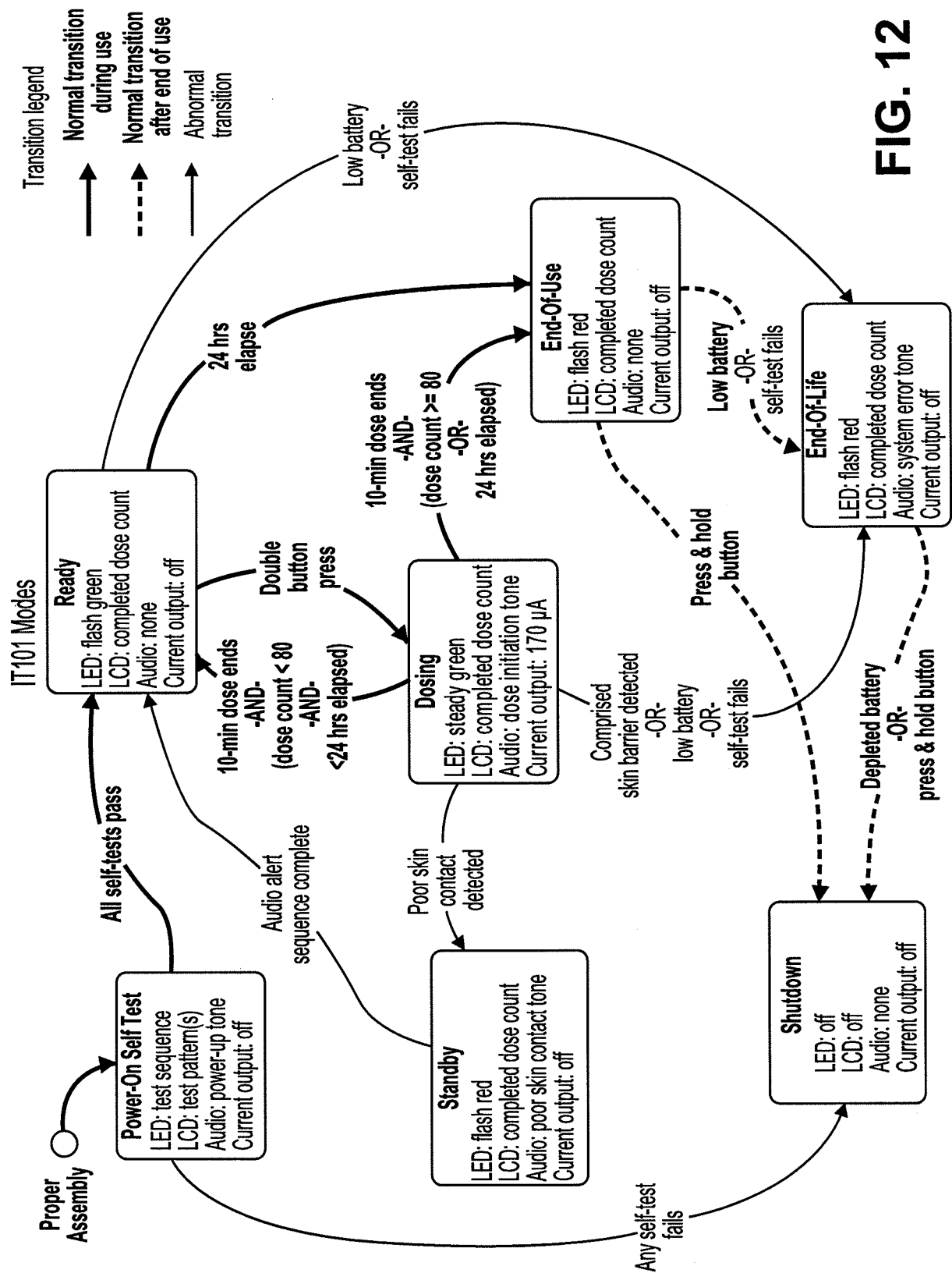


FIG. 12

IT101 Software Functional Block Diagram

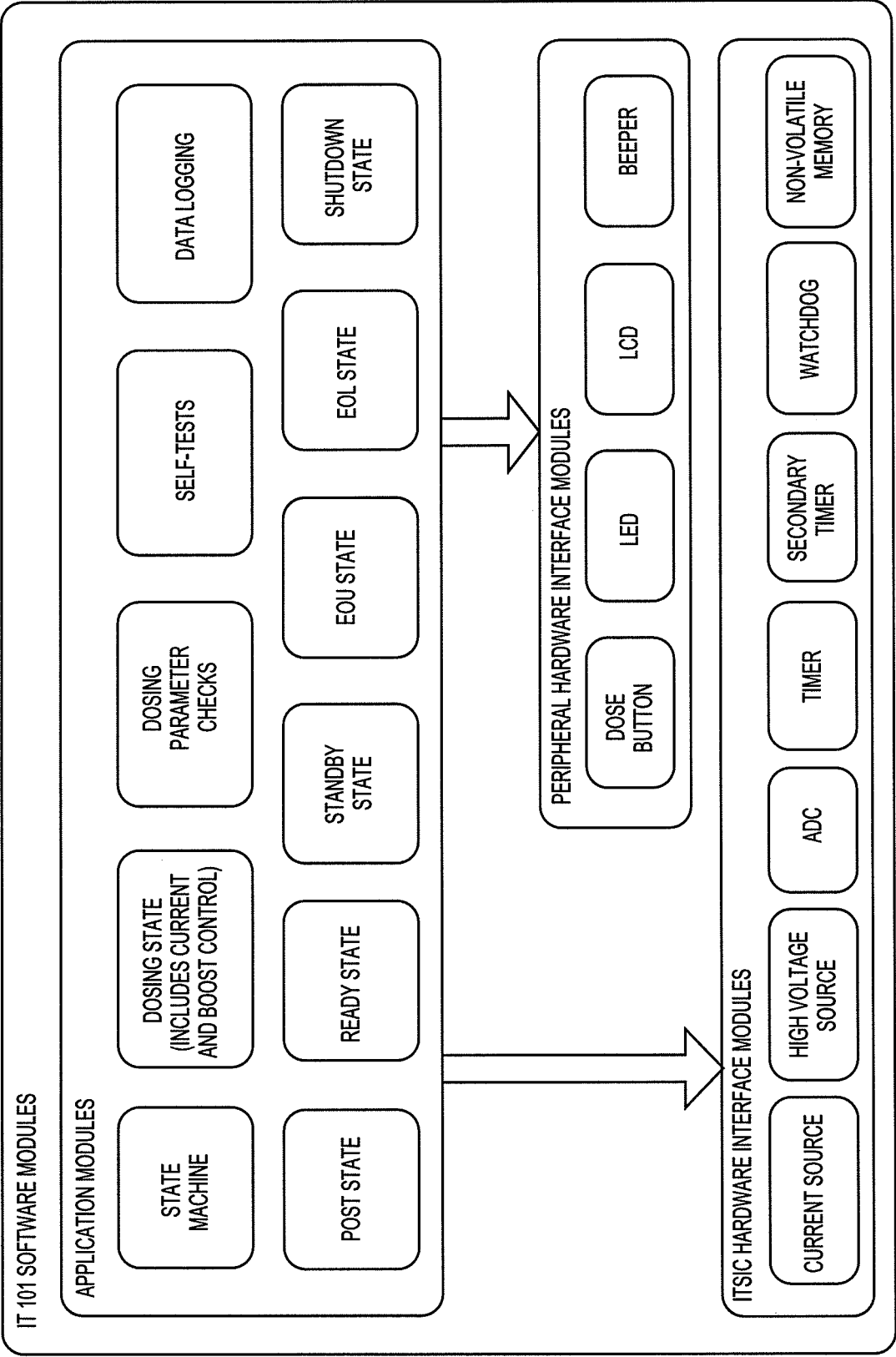
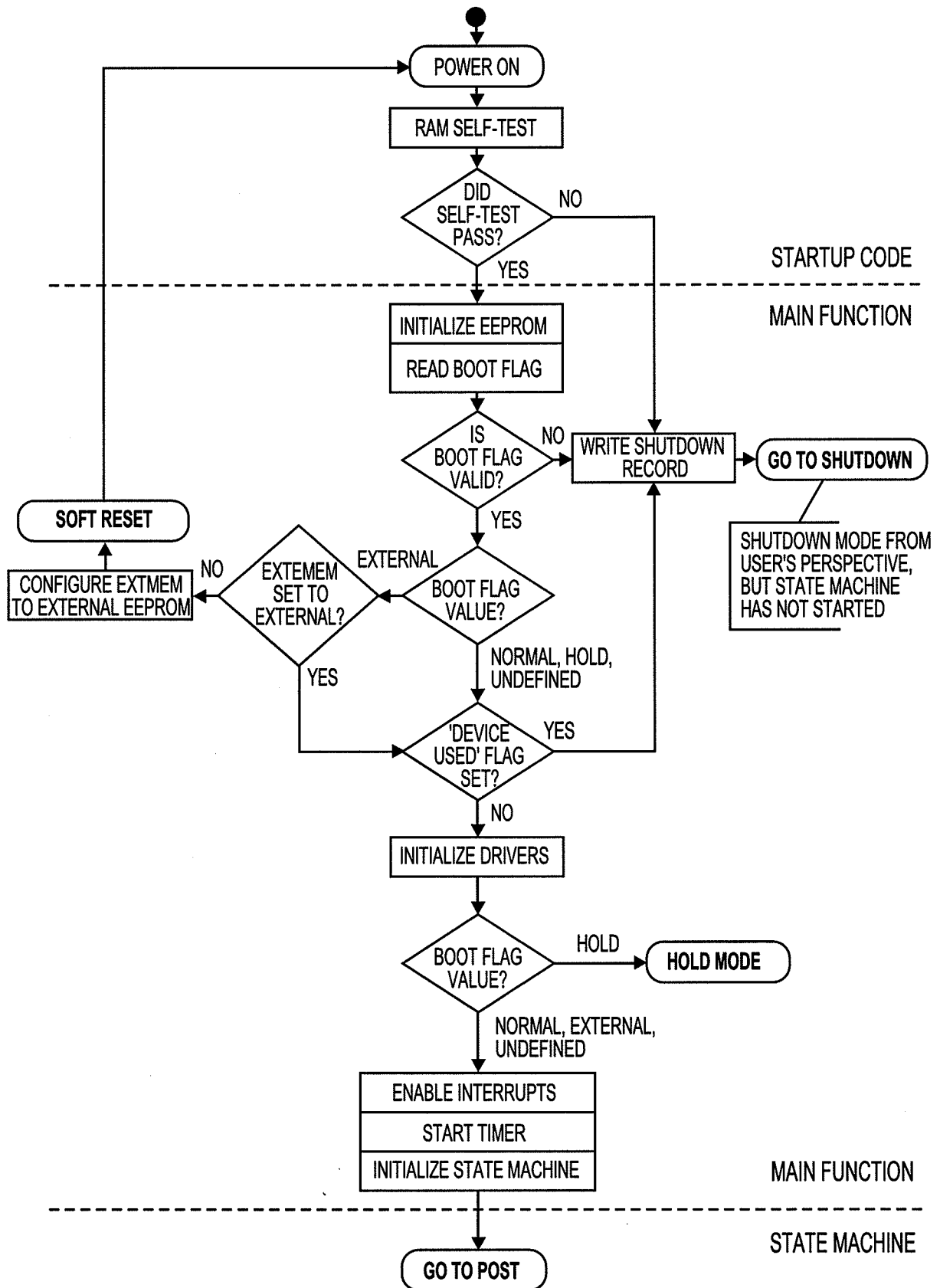


FIG. 13

**FIG. 14**

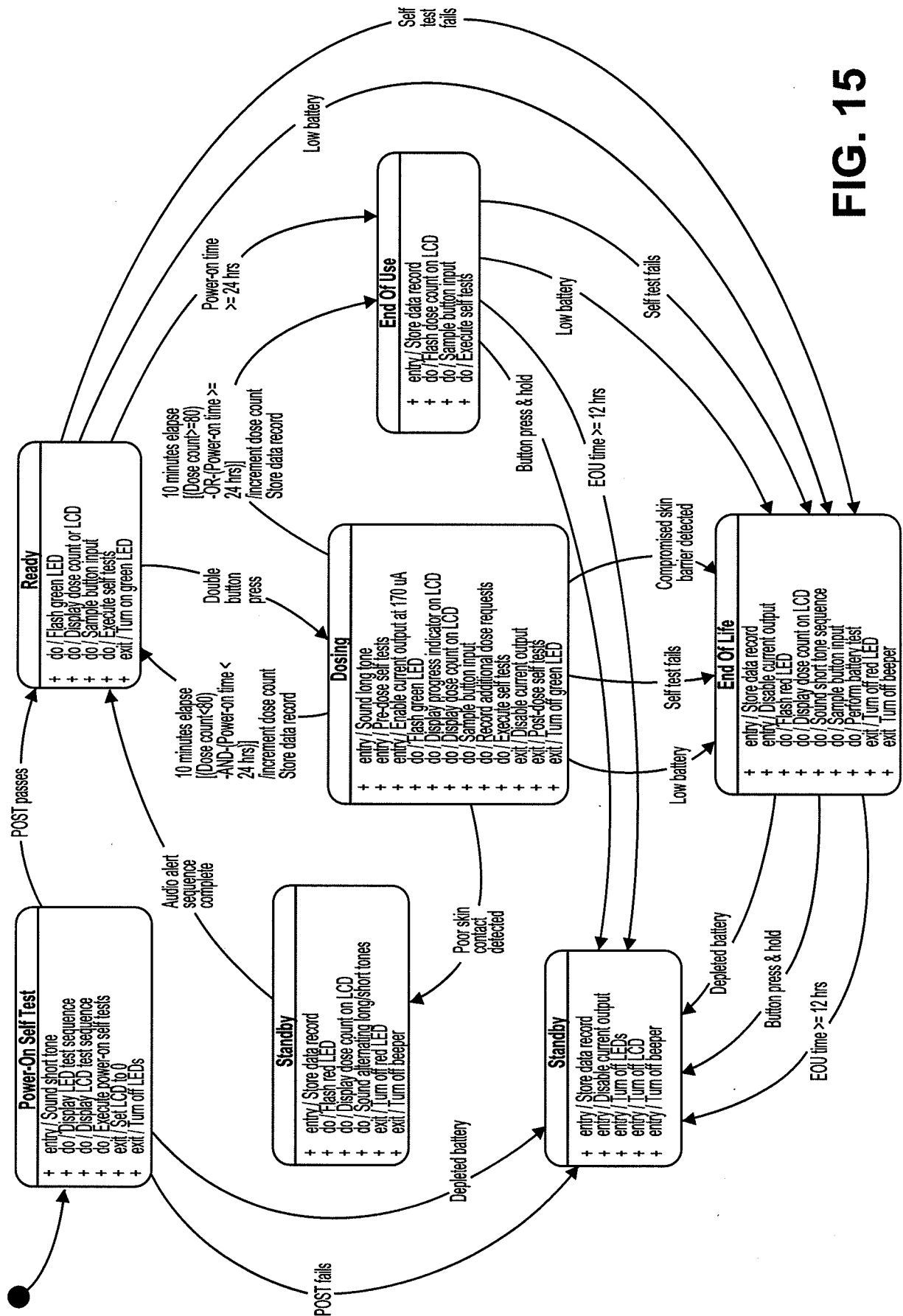
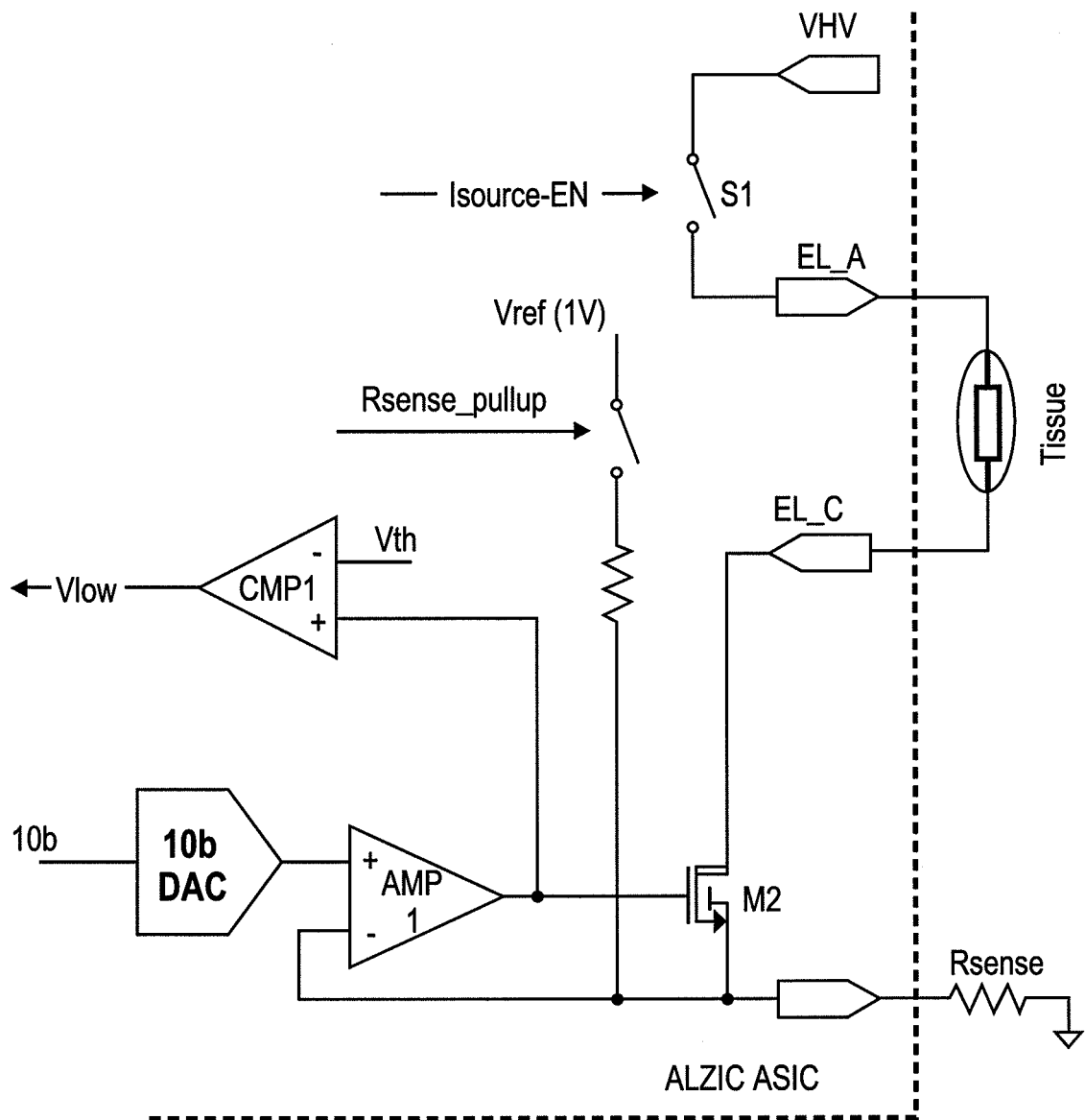
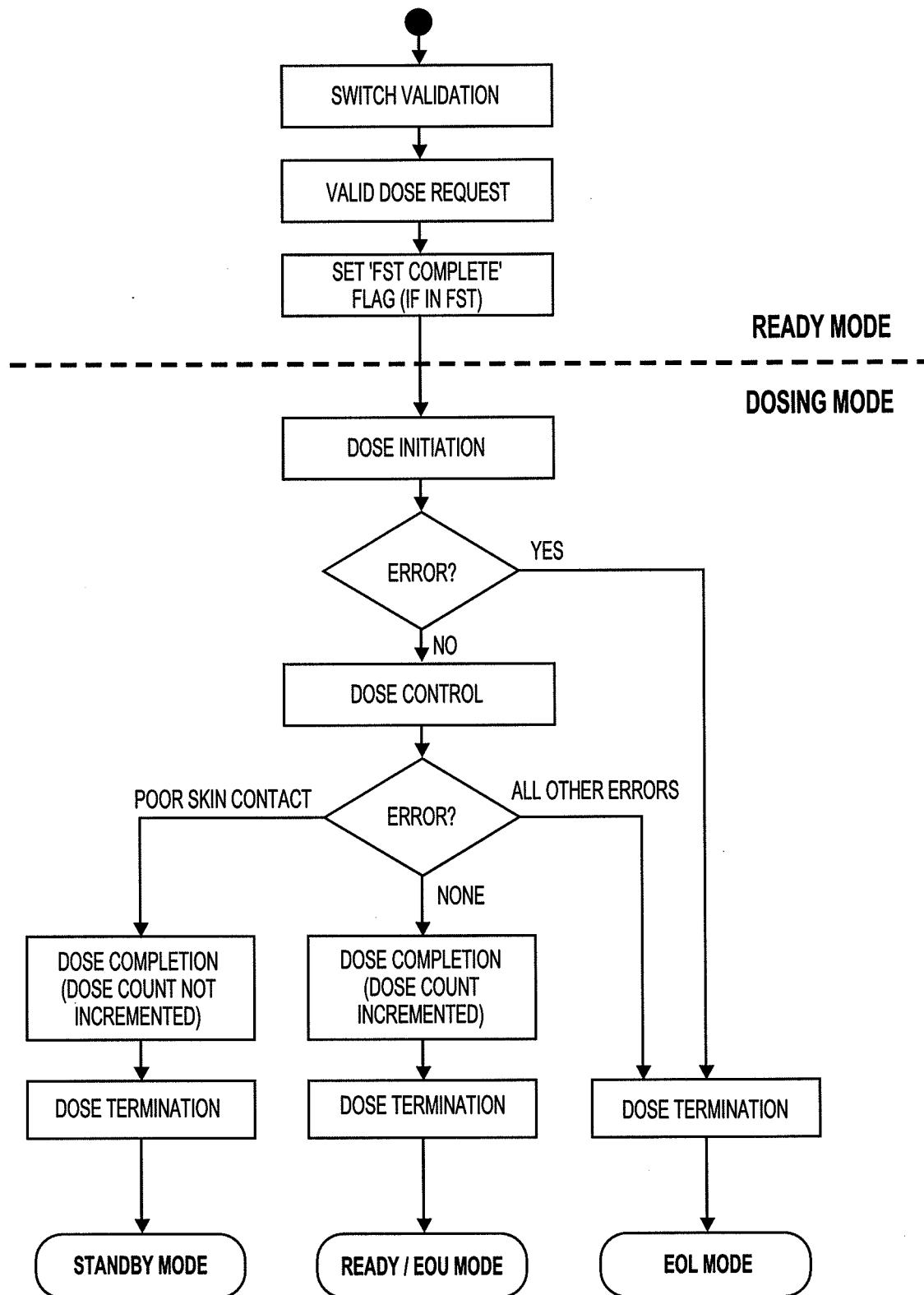


FIG. 15

**FIG. 16**

**FIG. 17**

DOSE INITIATION

FIG. 18

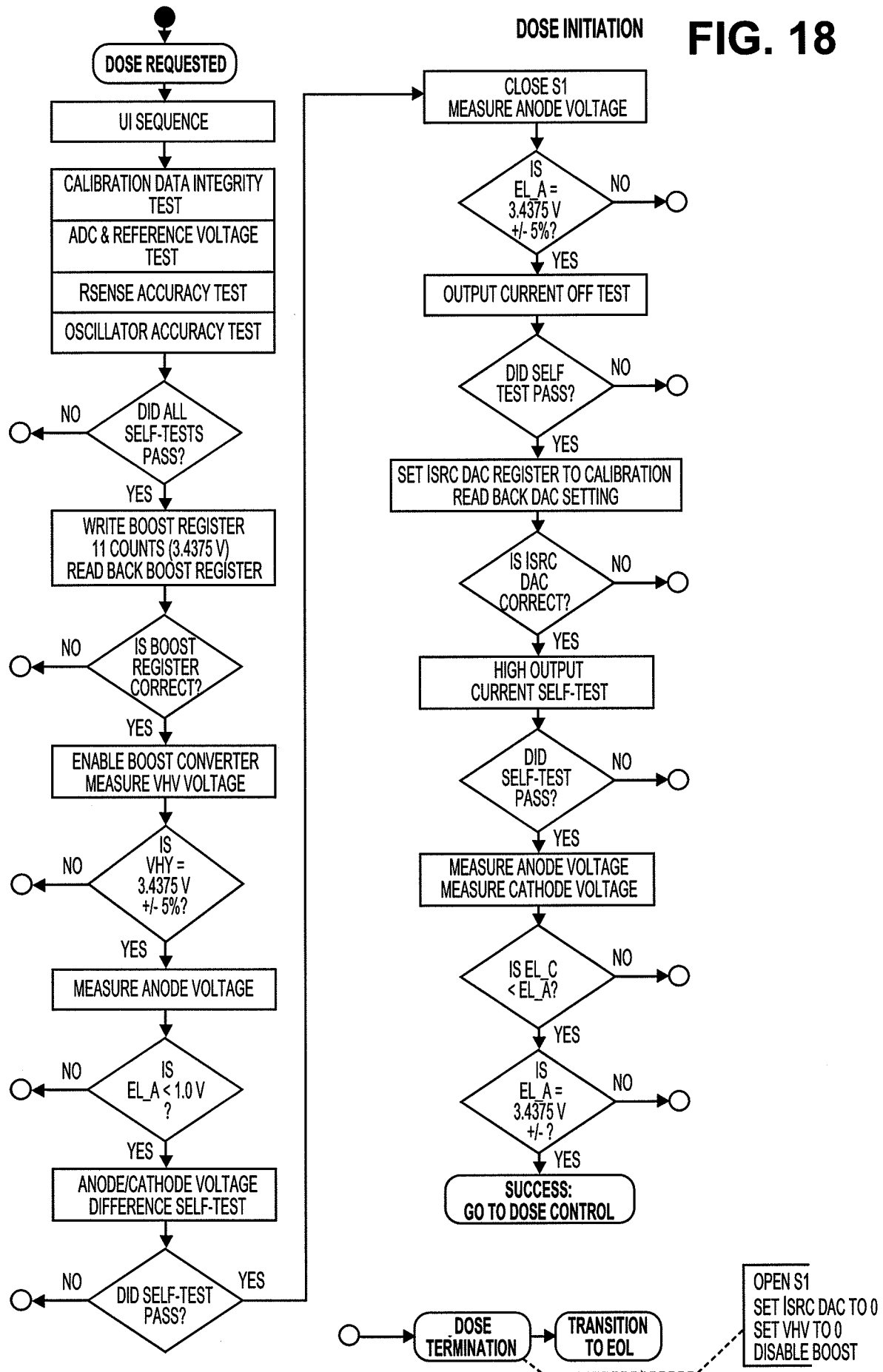


FIG. 19

DOSE CONTROL

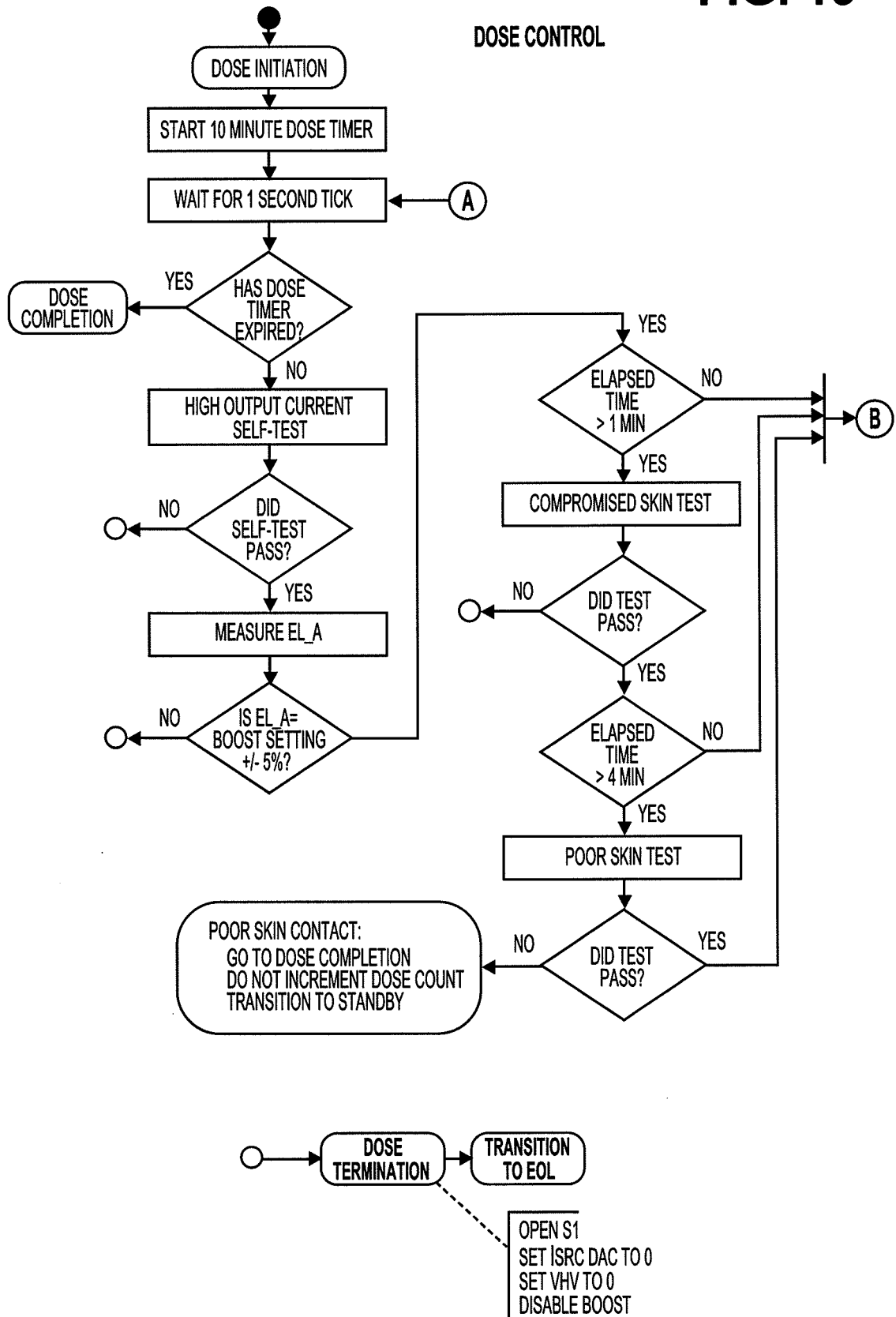
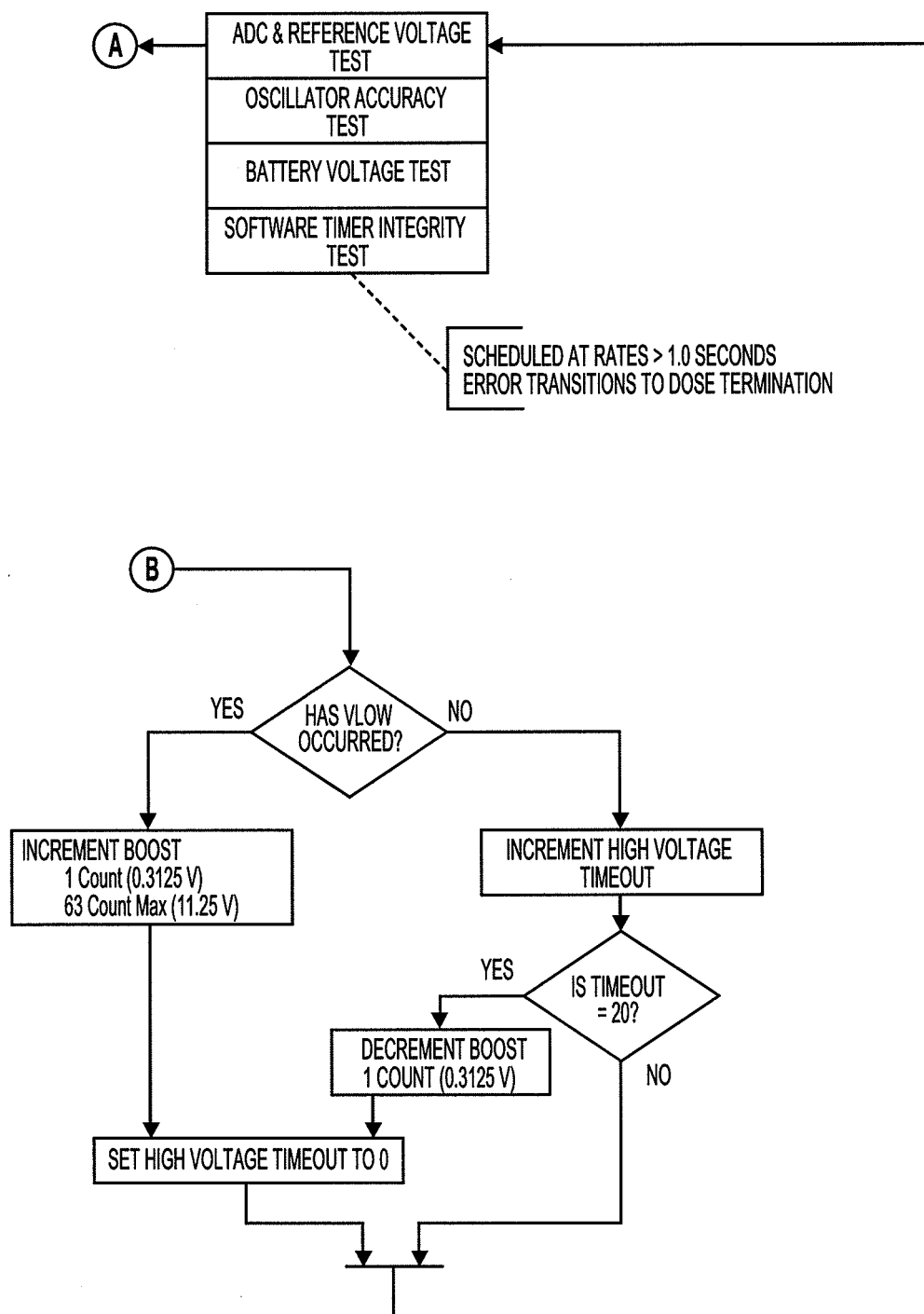
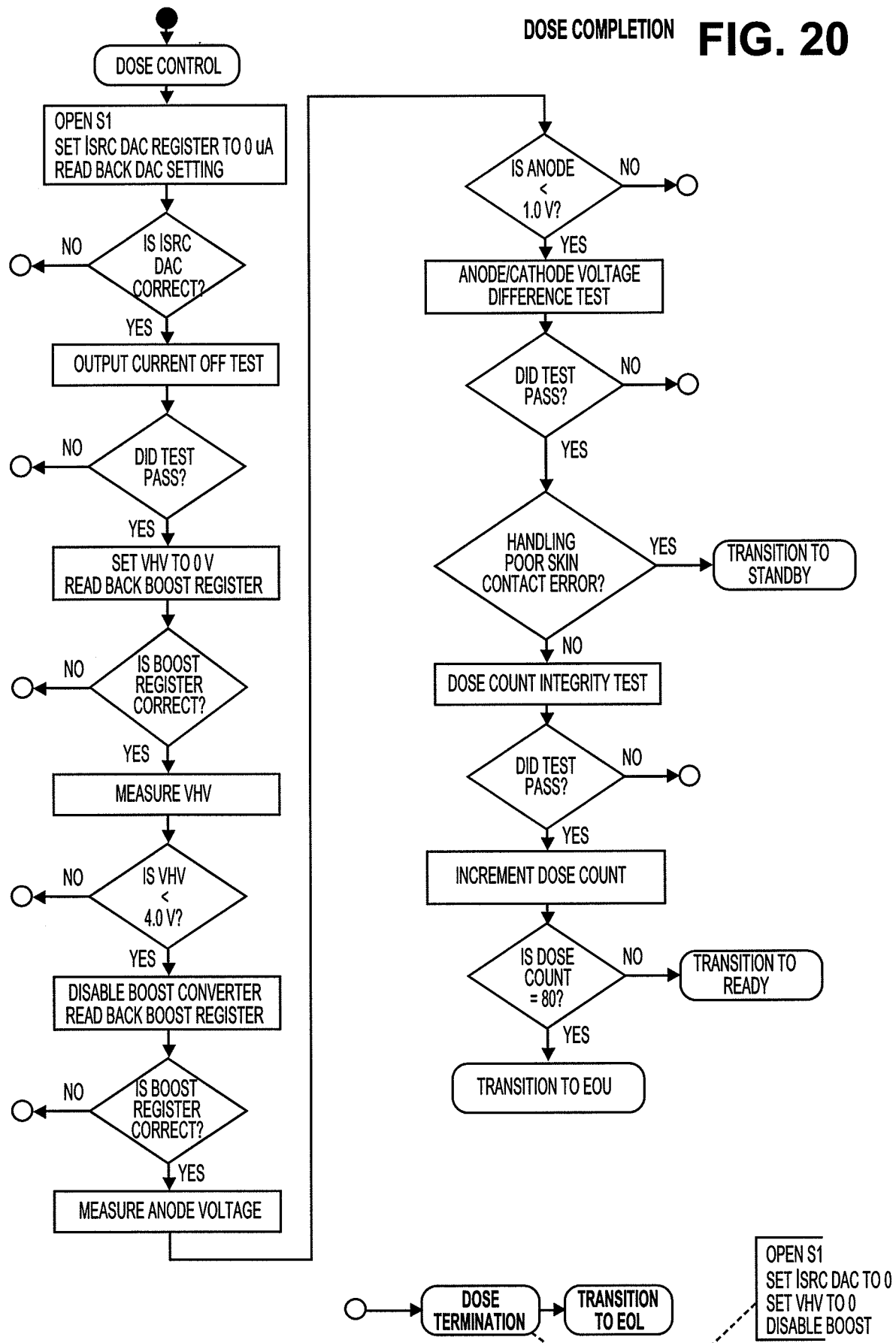


FIG. 19
(CONT.)

DOSE COMPLETION **FIG. 20**

Test name & ID		Test sequencing	Test scheduling						
			POST	Ready	Dosing			EOU	EOL
Predecessor tests				Periodically w/ indicated period	Before enabling current	Periodically w/ indicated period	After disabling current	Periodically w/ indicated period	Periodically w/ indicated period
1	RAM Test	N/A	X						
2	ROM Test	1	X						
3	Calibration Data Integrity Test	1,2	X	10 minutes	X			10 minutes	
4	ADC and Reference Voltage Test	1,2,3	X	1 minute	X		1 minute	1 minute	
5	Oscillator Accuracy Test	1,2,3,4	X	4 minutes	X		20 seconds		
6	Anode/Cathode Voltage Difference Test	1,2,3,4	X	1 minute	X		X	1 minute	
7	Rsense Accuracy Test	1,2,3,4	X	1 minute	X			1 minute	
8	Output Current Off Test	1,2,3,4,7	X	1 minute			X	1 minute	

FIG. 21

Test name & ID	Test sequencing	Test scheduling						
		POST	Ready	Dosing		Periodically w/ indicated period	EOL	
				Before enabling current	After disabling current			
	Predecessor tests		Periodically w/ indicated period	Before enabling current	Periodically w/ indicated period	After disabling current	Periodically w/ indicated period	
9	Battery Voltage Test 1,2,3,4	X	10 minutes		1 minute		10 minutes	
10	Software Timer Integrity Test 1,2,5		10 minutes		1 minute			
11	Dose Count Integrity Test 1,2,5					Before counting dose		
12	Analog Switch Validation Test 1,2,3,4		On every detected button release					
13	Digital Switch Validation Test 1,2		On second button release of double press					
14	Compromised Skin Barrier Test 1,2,3,4,7				1 second (after 1 min elapsed)			
15	Poor Skin Contact Test 1,2,3,4,7				1 second (after 4 min elapsed)			
16	High Output Current Test 1,2,3,4,7				1 second			

FIG. 21 (CONT.)