

Description

The invention relates to an amplifier arrangement comprising a first amplifier section having an input and an output, a second amplifier section having an input which is connected to the output of the first amplifier section, an output, at least a first output transistor and a first driver transistor for driving said output transistor, which second amplifier section is frequency compensated and has a gain which falls off at a rate of 6 dB/octave from a first angular frequency to a second angular frequency above a third angular frequency, where the open loop gain of the amplifier arrangement is equal to the inverse of the maximum negative feedback factor for which the amplifier arrangement operates without instabilities, and a protection circuit for overload protection of said output transistor, which protection circuit forms a loop around the second amplifier section and acts on the input of that second amplifier section.

Such amplifier arrangements are used for example as integrated power amplifiers for audio signals. The output transistors of such amplifiers must be protected against voltage and/or current overloading or overloading by a combination of voltage and current (so-called SOAR protection).

An amplifier arrangement of the type set forth in the opening paragraph is known from IEEE Journal of Solid State Circuits, December 1971, pages 357—366.

In this amplifier arrangement the protection circuit forms a loop around the second amplifier section and acts on the input of the second amplifier section which results in a high gain in the protection loop because of the utilization of the gain of the driver transistor. However, this high gain in the protection loop has the drawback that the protection circuit may give rise to instabilities when the protection circuit is in the activated condition.

It is the object of the invention to provide such an amplifier arrangement in which the risk of instabilities is reduced. An amplifier arrangement of the type set forth in the opening paragraph is characterized in that the protection circuit shows a frequency response with a first portion, which falls off with increasing frequency for a first range of frequencies, and with a second portion, which is frequency independent for a second range of frequencies above the first range, and which is situated around a fourth angular frequency which is lower than the third angular frequency, at which fourth angular frequency the modulus of the loop gain through the second amplifier section reaches the value unity when the protection circuit is in the activated condition.

With respect to the protection circuit, an amplifier arrangement in accordance with the invention may further be characterized in that the protection circuit comprises a detection circuit for supplying a signal which is a measure of the voltage and/or current carried by the first output transistor, a frequency-dependent network for obtaining the desired frequency dependence of

the transfer characteristic of the protection circuit and a buffer amplifier, and with respect to the frequency-dependent network the amplifier arrangement may further be characterized in that the detection circuit is arranged to supply an output current in an output-current circuit and the frequency-dependent network comprises the series arrangement of a resistor and a capacitance in said output circuit, the voltage across this output circuit being converted into a current via said buffer amplifier, which current is fed to the input of the second amplifier section.

In order to obtain a sharp transition between the active and the inactive range of the protection circuit a preferred amplifier arrangement in accordance with the invention is characterized in that a current source is arranged in parallel with the said series arrangement and a unidirectional clamping circuit is arranged at the output of the detection circuit, which clamping circuit clamps the input of the buffer amplifier at a comparatively fixed potential as long as the output current of the detection circuit does not exceed the current from said current source.

Moreover, if this preferred amplifier arrangement comprises a second output transistor which is driven in push-pull with the first output transistor and, in addition to the said protection circuit comprises a second protection circuit, for overload protection of said second output transistor, and the first amplifier section comprises a differential pair whose collector signal currents are applied to the second amplifier section in phase opposition, it may be characterized in that the output of one protection circuit is coupled to the collector circuit of one transistor of the differential pair and the output of the other protection circuit is coupled to the collector circuit of the other transistor of the differential pair.

The invention will now be described in more detail, by way of example, with reference to the drawings, in which

Fig. 1 shows a known amplifier arrangement in which a protection circuit in accordance with the invention may be used,

Fig. 2 is a block diagram of the amplifier shown in Fig. 1 provided with negative feedback,

Fig. 3 shows a frequency diagram for the amplifier arrangement shown in Fig. 2,

Fig. 4 shows the block diagram of Fig. 2 plus a protection circuit,

Fig. 5 is a block diagram of a part of the circuit arrangement shown in Fig. 4 in order to explain the operation of this arrangement,

Fig. 6 shows some frequency diagrams for the amplifier arrangement shown in Fig. 4 in order to clarify the operation thereof,

Fig. 7 shows a version of the protection circuit 13 (Fig. 4),

Fig. 8 shows in more detail a version of the detection circuit 12 shown in Fig. 7, and

Fig. 9 shows a preferred embodiment of the invention.

Fig. 1 shows a known amplifier arrangement to which a protection system may be added in

accordance with the invention. The known amplifier is of the same type as the operational amplifiers which are commercially available under type number μA 741. The amplifier comprises a first section 10, which has the nature of a voltage-current converter, comprising a pair of transistors T_1 and T_2 which are arranged as a differential amplifier and whose bases constitute the inverting (1) and non-inverting (2) inputs of the amplifier. The emitters of these transistors T_1 and T_2 are connected to the positive power-supply terminal 5 via a current source 4. The collectors of the transistors T_1 and T_2 are connected to an output 3 of said amplifier section 10, the collector of transistor T_1 via a current mirror comprising the transistors T_3 and T_4 , which output also constitutes the input 3 of the following section 11, which has the nature of a current-voltage converter. This section comprises a driver transistor T_5 which drives a conventional class-B output stage comprising an output 8, diodes D_1 and D_2 , output transistors T_A and T_B and a current source 7. The amplifier is frequency compensated in that a Miller capacitor C_m is arranged across the amplifier section 11.

Fig. 2 is a block diagram of the amplifier arrangement of Fig. 1 provided with a feedback loop and Fig. 3 shows the frequency response of this amplifier to illustrate the frequency behaviour of such an amplifier. As can be seen in Fig. 2 the amplifier receives negative feedback via a network 12 between the output 8 of the amplifier section 11 and the input 1 of the amplifier section 10, which network 12 produces a negative-feedback factor k .

The frequency-compensated amplifier without negative feedback as shown in Fig. 1 has the frequency response shown in Fig. 3, the gain $A(\omega)$ being A_0 for low frequencies, and falling off by 6 dB/octave from a specific angular frequency ω_1 defined by the compensation capacitor C_m to a frequency ω_2 , where a further time constant of the amplifier introduces a frequency roll-off of 12 dB/octave.

If negative feedback is applied to the amplifier with a feedback factor k , the gain of the amplifier will be equal to

$$\frac{1}{k}$$

up to the angular frequency ω_k , where

$$A(\omega_k) = \frac{1}{k}$$

and above which the frequency response of the amplifier will be the same as for the amplifier without negative feedback. For reasons of stability the frequency roll-off at $\omega = \omega_k$ should not exceed 6 dB/octave and any frequency roll-off exceeding 6 dB/octave should be situated at at least a specific distance from this frequency along the frequency axis. This means that

$\omega_k < \omega_2$, so that

$$k \leq k_{\max} \quad (1)$$

for which

$$\omega_k \leq \omega_{k_{\max}} < \omega_2,$$

where $k_{\max}$ and the corresponding value $\omega_{k_{\max}}$ are *inter alia* determined by the value of the angular frequency ω_2 . In general condition (1) applies to an amplifier without a protection circuit and consequently to an amplifier with a protection circuit which is not activated.

When it is assumed that the section 10 has a transconductance g_1 , the gain of section 11 will be

$$\frac{A(\omega)}{g_1}$$

The amplifier with negative feedback then has a gain factor v_o/v_i , where v_o is the output voltage on output 8 and v_i the input voltage on input 2, which is given by:

$$V_o/V_i = \frac{A(\omega)}{1 + A(\omega)k} = \frac{\frac{A(\omega) g_1}{g_1}}{\frac{1 + A(\omega) k g_1}{g_1}} \quad (2)$$

It is to be noted that the angular frequency ω_1 and, as a rule, the angular frequency ω_2 are determined by the second section, so that the gain g_1 in the relevant portion of the frequency spectrum is frequency-independent.

Fig. 4 is a block diagram of an operational amplifier provided with a protection circuit in accordance with the invention. The diagram is similar to that shown in Fig. 2, except that a protection circuit 13 is provided which acts on point 3 between the two amplifier sections. The protection circuit receives its information from the output transistors and when it is activated it constitutes a transconductance amplifier 13 having a transconductance g_b between the output of the amplifier 11 and its input 3.

When the protection circuit is activated the gain of the operational amplifier shown in Fig. 4 becomes:

$$V_o/V_i = \frac{A(\omega)}{g_1} \{g_1 (V_i - k V_o) - g_b V_o\}$$

which may be written as:

$$V_o/V_i = \frac{A(\omega)}{1 + A(\omega)k} \cdot \frac{1}{1 + \frac{g_b}{g_1} \frac{A(\omega)}{1 + A(\omega)k}} \quad (3)$$

This gain is the gain in conformity with expres-

sion (2), i.e. the gain in the absence of the protection circuit, multiplied by a factor $1/f$ which represents the reduction in gain as a result of the actuation of the protection circuit. This reduction factor f complies with:

$$\frac{1}{f} = \frac{1}{1 + \frac{g_b}{g_1} \frac{A(\omega)}{1 + A(\omega)k}}$$

For $A(\omega) \gg 1$ this equation may be reduced to:

$$g_b = g_1 k (f - 1)$$

As the reduction factor should be high in order to obtain satisfactory protection, it follows that

$$g_b \gg g_1 k \quad (4)$$

Rewriting expression (3) yields:

$$V_o/V_i = \frac{\frac{A(\omega)}{g_1} \cdot g_1}{1 + \frac{A(\omega)}{g_1} \cdot (kg_1 + gb)} \quad (5)$$

Since the amplifier should remain stable when the protection circuit is in the activated condition expression (5) should meet the stability criteria. This means that point -1 in the Nyquist diagram should not be enclosed. As regards the stability, the amplifier in conformity with expression (5), when ignoring a constant gain factor g_1 , may be regarded as an amplifier having a gain

$$\frac{A(\omega)}{g_1}$$

which receives feedback by a factor $(kg_1 + g_b)$, which amplifier is shown schematically in Fig. 5. In the situation shown in Figs. 2 and 3 a maximum feedback factor $k_{\max}$ must be observed for the amplifier and consequently a maximum feedback factor $k_{\max} g_1$ must be observed for the amplifier section 11 in view of the 12 dB/octave roll-off of the characteristic

$$\frac{A(\omega)}{g_1}$$

at the angular frequency ω_2 (see also Fig. 6a), so that the same condition must now be imposed:

$$kg_1 + g_b \leq k_{\max} g_1$$

$$\text{or} \quad g_b \leq (k_{\max} - k) g_1 \quad (6)$$

The stability criterion (6) consequently demands a

comparatively small value of the gain g_b , whereas the criterion (4) demands that the gain g_b be sufficiently high to achieve a high gain reduction. These two requirements seem to be conflicting except for small values of k and therefore lead to the conclusion that protection in this way is possible only when hardly any negative feedback is applied to the amplifier.

However, in accordance with the invention both requirements can be met because the stability requirement (6) is met for higher frequencies and the requirement (4) of a sufficiently high gain reduction is met for low frequencies. Thus, both requirements can be met when g_b is, for low frequencies, substantially higher than $g_1 k$ and has decreased to a value smaller than $(k_{\max} - k)g_1$ at the angular frequency $\omega_{k_{\max}}$.

In order to meet requirement (6) the point where the modulus of the loop gain

$$\frac{A(\omega)}{g_1}$$

$(kg_1 + g_b)$ (see expression 5) becomes unity is situated well before ω_2 , where $A(\omega_2)$ begins to exhibit a phase shift of 180° (12 dB/octave roll-off). This requirement is not sufficient because the term $(kg_1 + g_b)$ also introduces a phase shift. However, the amplifier becomes stable if requirement (6) is met and if around the point where the modulus of the loop gain becomes unity the term $(kg_1 + g_b)$ does not add any significant phase shift to the phase shift of

$$\frac{A(\omega)}{g_1}$$

which second requirement is met by making the term g_b frequency-independent around this point. To illustrate this Fig. 6 shows some frequency diagrams namely in Fig. 6a the modulus of the gain

$$\frac{A(\omega)}{g_1}$$

as a function of the angular frequency ω , in Fig. 6b the modulus of the gain g_b of the protection stage, and in Fig. 6c the modulus of the loop gain

$$\frac{A(\omega)}{g_1} (kg_1 + g_b)$$

of the amplifier stage 11 when the protection circuit is in the activated condition.

Since the term g_1 is assumed to be constant the characteristic

$$\frac{A(\omega)}{g_1}$$

varies in the same way as the characteristic $A(\omega)$ shown in Fig. 3. The negative feedback factor of the amplifier is k , which factor is such that

$$\frac{A(\omega k)}{g_1}$$

is equal to

$$\frac{1}{g_1 k}$$

for $\omega = \omega_k$ and is

$$\frac{1}{g_1 k_{\max}}$$

for $\omega = \omega_{k\max}$.

For $|g_b|$ a variation (Fig. 6b) is selected for which $|g_b|$ for $\omega = 0$ is equal to g_{b0} and for an angular frequency around $\omega = \omega_{k\max}$ is equal to $(k_{\max} - k)g_1$, which is the maximum value which is permissible in accordance with expression (6). Outside these points the response is not of great importance and in the present example it is flat up to $\omega = \omega_g$ followed by a slope of 6 dB/octave up to an angular frequency $\omega = \omega_4$. Above this frequency the response is flat up to an angular frequency $\omega = \omega_3$ where $|g_b|$ falls off further. The combined characteristic (Fig. 6c) is initially flat, and via one or two break points, depending on the situation of the angular frequency ω_g relative to angular frequency ω_1 , it changes to a slope which is 12 dB/octave at most and which depends on the slope of the term $kg_1 + g_b$ in comparison with the 6 dB/octave slope of the term g_b alone, after which the characteristic falls off above the angular frequency $\omega = \omega_4$ at a rate of 6 dB/octave as a result of the flatness of the characteristic for g_b at this frequency. It will be evident that the angular frequency for which this graph intersects the line 1 should lie within a portion of the graph where the slope is substantially smaller than 12 dB/octave, i.e. in the portion where this slope is 6 dB/octave, which requirement is met in this situation.

In the situation as outlined above it is assumed that $g_b = (k_{\max} - k)g_1$ for $\omega = \omega_{k\max}$. However, this is the maximum value of g_b which accords with expression 6. Since the various parameters may exhibit a spread and, moreover, may be selected more or less freely (for example the parameter k), g_b will be smaller than the value $(k_{\max} - k)g_1$ in practice, so that the value of $|g_b|$ decreases (dotted characteristic in Fig. 6b) as a result of which the value of

$$\left| \frac{A(\omega)}{g_1} (kg_1 + g_b) \right|$$

decreases (dotted characteristic in Fig. 6c) and the line

$$\left| \frac{A(\omega)}{g_1} (kg_1 + g_b) \right| = 1$$

is intersected at an angular frequency ω_5 which is lower than the angular frequency $\omega_{k\max}$. The flat portion of the characteristic g_b should therefore be sufficiently wide to encompass the frequency ω_5 . A decrease of g_b relative to the value $(k_{\max} - k)g_1$ for high frequencies may occur when the term kg_1 increases or the quantity $g_b(\omega_1)$ (g_b for the value $\omega = \omega_1$) decreases or when the effect of the negative feedback via the protection circuit 13 decreases in comparison with the effect of the negative feedback via the negative-feedback path 12. In the term $kg_1 + g_b$ this means a decrease of the effect of the phase shift of the frequency-dependent term g_b . If this decrease of $g_b(\omega_1)$ in comparison with $(k_{\max} - k)g_1$ is such that $g_b \ll kg_1$, the point where

$$\left| \frac{A(\omega)}{g_1} (kg_1 + g_b) \right| = 1$$

will be situated at $\omega = \omega_k$.

Thus, when the flat portion of the characteristic for g_b extends further than the angular frequency ω_k no stability problems are envisaged. The angular frequency ω_k , however, depends on the negative feedback factor k . However, in practice a rather accurately defined value will be required for the negative feedback factor k , so that the stability requirements can be met. In a practical version the selected values were

$$3\omega_4 \leq \omega_{k\max} \leq \frac{1}{3}\omega_3.$$

Fig. 7 shows a version of a protection circuit 13 providing the frequency response shown in Fig. 6b. The protection circuit comprises a frequency-independent section 12a, which in addition to those from output 8 can also receive other input signals, and a section 12b which determines the frequency response. The section 12a, having a transconductance g_m , supplies a current i_m . This current is converted into a voltage by means of an RC-network comprising a resistor 15 having a resistance R_x and a capacitor 16 having a capacitance C_x , which voltage is converted into a current i_b through a resistor 17 having a value R_o via a buffer amplifier 14, for example an emitter follower. Moreover, the circuit comprises a spurious capacitance 117 of the value C_p and a leakage resistance 18 of a value R_p , which are responsible for the break-points at $\omega = \omega_g$ and $\omega = \omega_3$ in the characteristic of Fig. 6b. The transfer function is

$$\frac{i_b}{V_o} = g_b = g_m \frac{R_p (1 + j \omega \tau_2)}{R_o (1 + j \omega \tau_1) (1 + j \omega \tau_3)} \quad (7)$$

where

$$\begin{aligned} \tau_1 &= R_p (C_x + C_p) \\ \tau_2 &= R_x (C_x + C_p) \\ \tau_3 &= R_x C_p \end{aligned}$$

The various parameters in the characteristic of Fig. 6b are then as follows:

$$g_{bo} = g_m \frac{R_p}{R_o}$$

$$g_k = g_m \frac{R_x}{R_o}$$

$$\omega_g = \frac{1}{R_p(C_x + C_p)}$$

$$\omega_4 = \frac{1}{R_x(C_x + C_p)}$$

$$\omega_3 = \frac{1}{R_x C_p}$$

Fig. 8 shows a practical version of the protection circuit 13 shown in Fig. 7. An output transistor T_A to be protected has its collector connected to the positive power-supply terminal 5 via a sensing resistor 23 having a resistance value R_{23} (for example 0.03Ω) and its emitter connected to the output 8, to which a terminating impedance 26 of the value R_L is connected. The transistor T_A must be protected against excessive currents and excessive voltages and a combination of the two (so-called SOAR protection). For this purpose the collector current I_C is measured by means of the resistor 23. The resistor 23 forms part of the input circuit of a current mirror comprising transistors T_{14} and T_{15} , a resistor 25 and an input-current source 26.

When the currents through transistors T_{14} and T_{15} and/or the voltages across the resistors 23 and 25 are such that the difference between the base-emitter voltages of transistors T_{14} and T_{15} is of subordinate importance, the output current I_{C15} will be such that the voltages across the resistors 23 and 25 are substantially equal to each other, which can be achieved over an adequately wide range of the current I_C to be measured. The current I_{C15} is then:

$$I_{C15} = \frac{R_{23}}{R_{25}} I_C + I_1 \quad (8)$$

where R_{23} is the value of the resistor 23, R_{25} the value of the resistor 25, and I_1 a direct current term as a result of the current from the current source 26.

In order to measure the collector voltage of the transistor T_A a resistive divider comprising the resistors 19 (of the value R_{19}) and 20 (of the value

R_{20}) is connected between the power-supply terminal 5 and the output 8. The resistor 20 is also the resistor in the input circuit of a current mirror comprising transistors T_{12} and T_{13} , the resistors 20 and 24 (of the value R_{24}) and the direct-current source 27. The voltage on the junction point of the resistors 19 and 20 is limited by a transistor T_{11} arranged as a Zener diode.

When it is assumed that the difference between the base-emitter voltages of the two transistors T_{12} and T_{13} plays a subordinate role, the voltages across the resistors 20 and 24 will be substantially equal to each other in this current mirror. The collector current I_{C13} of transistor T_{13} is then:

$$I_{C13} = I_2 - \frac{R_{20}}{(R_{19} + R_{20})R_{24}} V_o \quad (9)$$

where I_2 is a direct current term caused by the current from the input-current source 27.

From the expressions (8) and (9) and the relationship $I_C = V_o/R_L$ (R_L is the value of the load connected to output 8), the following can be derived for $I_m = I_{C13} + I_{C15}$:

$$I_m = I_1 + I_2 + \left(\frac{R_{23}}{R_{25}R_L} - \frac{R_{20}}{(R_{19} + R_{20})R_{24}} \right) V_o \quad (10)$$

This means that the transconductance g_m in equation (7) is:

$$g_m = \frac{R_{23}}{R_{25}R_L} - \frac{R_{20}}{(R_{19} + R_{20})R_{24}}$$

In this respect it is to be noted that since the load R_L now appears in the transfer characteristic care must be taken that it has a resistive nature, at least in the relevant frequency range around ω_k . The current I_R from the current source 28 is subtracted from this current I_m , this defining the activation point of the protection circuit. When the current I_m exceeds the current I_R the difference i_m , in the same way as in the case of Fig. 7, flows through the series arrangement of the resistor 15 and the capacitor 16 and the voltage thus obtained is applied to resistor 17 via amplifier 14, comprising the emitter-follower transistor T_{16} , which resistor 17 is arranged between the emitter of transistor T_{16} and the junction point 3 between the amplifier stages 10 and 11. The base-emitter junction between point 3 and earth hardly affects the current-voltage conversion across the resistor 17.

In the protection circuit of Fig. 8 the base of transistor T_{16} is clamped at a point carrying the reference voltage V_R by means of a transistor T_{17} . This step serves to preclude the activation of the protection circuit 13 when this is not required and the current I_m does not exceed a specific value I_R . Conduction of the clamping transistor T_{17} is sustained by the excess current from the current source 28. Indeed, when the current I_C or the

voltage V_o is such that the voltage drop across the resistors 20 and 23 is inadequate, the sum of the output currents of the associated current mirrors T_{14} , T_{15} and T_{12} , T_{13} will be smaller than the current I_R so that the current source 28 can produce a current through transistor T_{17} . The voltage V_R is such that the transistor T_{16} is not turned on when the protection circuit is not activated. If the protection circuit is activated, transistor T_{17} is cut off because the current I_m exceeds the value I_R and transistor T_{16} is turned on. This results in a very sharp transition between the two states (activated and non-activated).

Fig. 9 shows a preferred embodiment of the invention. The first (10) and second (11) amplifier sections are essentially the same as those in the circuit arrangement shown in Fig. 1 and corresponding parts bear the same reference numerals. In the transconductance amplifier 10 the collector-base coupling across transistor T_3 is formed by the base-emitter junction of a transistor T_6 . In the output amplifier 11 a driver transistor T_5 is arranged as a Darlington stage with transistor T_7 and current source 29, whilst the output stage itself is arranged as a quasi-complementary output stage with Darlington output transistors in that the output transistors T_A and T_B are of the same conductivity type and form a Darlington arrangement with transistors T_8 and T_9 respectively. The quasi-complementary behaviour is obtained by the addition of the pnp-transistors T_{10} and T_{21} , as is shown in the Figure. Output transistor T_A is protected by a circuit 13 which is identical to the circuit shown in Fig. 8 and whose parts bear the same reference numerals. Output transistor T_B is protected in a similar manner by means of a circuit 13a, which largely corresponds to the circuit 13 and of which corresponding parts bear the same reference numerals with the index a. This circuit operates in the same way as the circuit shown in Fig. 7, but the current mirrors comprising the transistors T_{12a} to T_{15a} are of the complementary type, so that the current i_m is reflected to the base of transistor T_{16a} by means of a current mirror comprising transistors T_{22} and T_{23} and resistors 30 and 31.

Via resistor 17 the emitter of transistor T_{16} is coupled directly to point 3. The emitter current of transistor T_{16a} must be inverted because of the complementary drive of transistor T_B from point 3. This is effected by connecting the emitter of transistor T_{16a} to the input of the current mirror T_3 , T_4 via resistor 17a, so that this current mirror inverts the emitter current of said transistor to output 3.

Claims

1. An amplifier arrangement comprising a first amplifier section (10) having an input (2) and an output (3), a second amplifier section (11) having an input which is connected to the output (3) of the first amplifier section (10), an output (8), at least a first output transistor and a first driver transistor for driving said output transistor, which

second amplifier section (11) is frequency compensated and has a gain which falls off at a rate of 6 dB/octave from a first angular frequency to a second angular frequency above a third angular frequency where the open loop gain of the amplifier arrangement is equal to the inverse of the maximum negative feedback factor for which the amplifier arrangement operates without instabilities, and a protection circuit (13) for overload protection of said output transistor, which protection circuit (13) forms a loop around the second amplifier section (11) and acts on the input (3) of that second amplifier section (11), characterized in that the protection circuit (11) shows a frequency response with a first portion which falls off with increasing frequency for a first range of frequencies, and with a second portion, which is frequency independent for a second range of frequencies above the first range and which is situated around a fourth angular frequency which is lower than the third angular frequency, at which fourth angular frequency the modulus of the loop gain through the second amplifier section (11) reaches the value unity when the protection circuit (13) is in the activated condition (Fig. 4).

2. An amplifier arrangement as claimed in Claim 1, characterized in that the protection circuit comprises a detection circuit (12a) for supplying a signal which is a measure of the voltage and/or current carried by the first output transistor, a frequency dependent network (15, 16) for obtaining the desired frequency dependence of the transfer characteristic of the protection circuit and a buffer amplifier (14) (Fig. 7).

3. An amplifier arrangement as claimed in Claim 2, characterized in that the detection circuit (12a) is arranged to supply an output current (i_m) in an output-current circuit (12b) and the frequency-dependent network comprises the series arrangement of a resistor (15) and a capacitance (16) in said output circuit (12b), the voltage across this output circuit being converted into a current (i_b) via said buffer amplifier (14), which current (i_b) is fed to the input of the second amplifier section (Fig. 7).

4. An amplifier arrangement as claimed in Claim 3, characterized in that a current source (28) is arranged in parallel with said series arrangement (15, 16) and a unidirectional clamping circuit (T_{17}) arranged at the output of the detection circuit, which clamping circuit (T_{17}) clamps the input of the buffer amplifier (14) at a fixed potential as long as the output current (I_m) of the detection circuit does not exceed the current (I_R) from said current source (28) (Fig. 8).

5. An amplifier arrangement as claimed in any of the preceding Claims, which comprises a second output transistor (T_B) which is driven in push-pull with the first output transistor (T_A), which in addition to the said protection circuit (13) comprises a second protection circuit (13a) for overload protection of said second output transistor (T_B), and in which the first amplifier section (10) comprises a differential pair (T_1 , T_2)

voltage V_o is such that the voltage drop across the resistors 20 and 23 is inadequate, the sum of the output currents of the associated current mirrors T_{14} , T_{15} and T_{12} , T_{13} will be smaller than the current I_R so that the current source 28 can produce a current through transistor T_{17} . The voltage V_R is such that the transistor T_{16} is not turned on when the protection circuit is not activated. If the protection circuit is activated, transistor T_{17} is cut off because the current I_m exceeds the value I_R and transistor T_{16} is turned on. This results in a very sharp transition between the two states (activated and non-activated).

Fig. 9 shows a preferred embodiment of the invention. The first (10) and second (11) amplifier sections are essentially the same as those in the circuit arrangement shown in Fig. 1 and corresponding parts bear the same reference numerals. In the transconductance amplifier 10 the collector-base coupling across transistor T_3 is formed by the base-emitter junction of a transistor T_6 . In the output amplifier 11 a driver transistor T_5 is arranged as a Darlington stage with transistor T_7 and current source 29, whilst the output stage itself is arranged as a quasi-complementary output stage with Darlington output transistors in that the output transistors T_A and T_B are of the same conductivity type and form a Darlington arrangement with transistors T_8 and T_9 respectively. The quasi-complementary behaviour is obtained by the addition of the pnp-transistors T_{10} and T_{21} , as is shown in the Figure. Output transistor T_A is protected by a circuit 13 which is identical to the circuit shown in Fig. 8 and whose parts bear the same reference numerals. Output transistor T_B is protected in a similar manner by means of a circuit 13a, which largely corresponds to the circuit 13 and of which corresponding parts bear the same reference numerals with the index a. This circuit operates in the same way as the circuit shown in Fig. 7, but the current mirrors comprising the transistors T_{12a} to T_{15a} are of the complementary type, so that the current i_m is reflected to the base of transistor T_{16a} by means of a current mirror comprising transistors T_{22} and T_{23} and resistors 30 and 31.

Via resistor 17 the emitter of transistor T_{16} is coupled directly to point 3. The emitter current of transistor T_{16a} must be inverted because of the complementary drive of transistor T_B from point 3. This is effected by connecting the emitter of transistor T_{16a} to the input of the current mirror T_3 , T_4 via resistor 17a, so that this current mirror inverts the emitter current of said transistor to output 3.

Claims

1. An amplifier arrangement comprising a first amplifier section (10) having an input (2) and an output (3), a second amplifier section (11) having an input which is connected to the output (3) of the first amplifier section (10), an output (8), at least a first output transistor and a first driver transistor for driving said output transistor, which

second amplifier section (11) is frequency compensated and has a gain which falls off at a rate of 6 dB/octave from a first angular frequency to a second angular frequency above a third angular frequency where the open loop gain of the amplifier arrangement is equal to the inverse of the maximum negative feedback factor for which the amplifier arrangement operates without instabilities, and a protection circuit (13) for overload protection of said output transistor, which protection circuit (13) forms a loop around the second amplifier section (11) and acts on the input (3) of that second amplifier section (11), characterized in that the protection circuit (11) shows a frequency response with a first portion which falls off with increasing frequency for a first range of frequencies, and with a second portion, which is frequency independent for a second range of frequencies above the first range and which is situated around a fourth angular frequency which is lower than the third angular frequency, at which fourth angular frequency the modulus of the loop gain through the second amplifier section (11) reaches the value unity when the protection circuit (13) is in the activated condition (Fig. 4).

2. An amplifier arrangement as claimed in Claim 1, characterized in that the protection circuit comprises a detection circuit (12a) for supplying a signal which is a measure of the voltage and/or current carried by the first output transistor, a frequency dependent network (15, 16) for obtaining the desired frequency dependence of the transfer characteristic of the protection circuit and a buffer amplifier (14) (Fig. 7).

3. An amplifier arrangement as claimed in Claim 2, characterized in that the detection circuit (12a) is arranged to supply an output current (i_m) in an output-current circuit (12b) and the frequency-dependent network comprises the series arrangement of a resistor (15) and a capacitance (16) in said output circuit (12b), the voltage across this output circuit being converted into a current (i_b) via said buffer amplifier (14), which current (i_b) is fed to the input of the second amplifier section (Fig. 7).

4. An amplifier arrangement as claimed in Claim 3, characterized in that a current source (28) is arranged in parallel with said series arrangement (15, 16) and a unidirectional clamping circuit (T_{17}) arranged at the output of the detection circuit, which clamping circuit (T_{17}) clamps the input of the buffer amplifier (14) at a fixed potential as long as the output current (i_m) of the detection circuit does not exceed the current (I_R) from said current source (28) (Fig. 8).

5. An amplifier arrangement as claimed in any of the preceding Claims, which comprises a second output transistor (T_B) which is driven in push-pull with the first output transistor (T_A), which in addition to the said protection circuit (13) comprises a second protection circuit (13a) for overload protection of said second output transistor (T_B), and in which the first amplifier section (10) comprises a differential pair (T_1 , T_2)



whose collector signal currents are applied to the second amplifier section (11) in phase opposition, characterized in that the output of one protection circuit (13) is coupled to the collector circuit of one transistor (T_2) of the differential pair (T_1 , T_2) and the output of the other protection circuit (13a) is coupled to the collector circuit of the other transistor (T_1) of the differential pair (T_1 , T_2) (Fig. 9).

Patentsprüche

1. Verstärkeranordnung, bestehend aus einem ersten Verstärkerabschnitt (10) mit einem Eingang (2) und einem Ausgang (3), aus einem zweiten Verstärkerabschnitt (11) mit einem Eingang, der an den Ausgang (3) des ersten Verstärkerabschnitts (10) angeschlossen ist, aus einem Ausgang (8), zumindest einem ersten Ausgangstransistor und einem ersten Steuertransistor zum Steuern des Ausgangstransistors, wobei der zweite Verstärkerabschnitt (11) in der Frequenz ausgeglichen ist und eine Verstärkung hat, die mit einer Geschwindigkeit von 6 dB/Oktave von einer ersten Winkelfrequenz nach einer zweiten Winkelfrequenz über einer dritten Winkelfrequenz abfällt, wobei die Leerlaufverstärkung der Verstärkeranordnung gleich dem umgekehrten Wert des maximalen Gegenkopplungsfaktors ist, bei dem die Verstärkeranordnung schwankungsfrei arbeitet, und aus einer Schutzschaltung (13) für den Überlastungsschutz des Ausgangstransistors, wobei dieser Schutzschaltung (13) eine Schleife um den zweiten Verstärkerabschnitt (11) bildet und auf den Eingang (3) dieses zweiten Verstärkerabschnitts (11) einwirkt, dadurch gekennzeichnet, dass die Schutzschaltung (13) einen Frequenzgang mit einem ersten Teil, der bei ansteigender Frequenz für eine erste Reihe von Frequenzen abfällt, und mit einem zweiten Teil aufweist, der für eine zweite Reihe von Frequenzen über der ersten Reihe frequenzunabhängig und um eine vierte Winkelfrequenz herum angebracht ist, die niedriger als die dritte Winkelfrequenz ist und bei der der Modulus der Schleifenverstärkung durch den zweiten Verstärkerabschnitt (11) den Wert eins erreicht, wenn die Schutzschaltung (13) sich im aktivierten Zustand befindet (Fig. 4).

2. Verstärkeranordnung nach Anspruch 1, dadurch gekennzeichnet, dass die Schutzschaltung eine Detektorschaltung (12a) zur Lieferung eines Signals, das ein Mass für die vom ersten Ausgangstransistor geführten Spannung und/oder für den vom ersten Ausgangstransistor geführten Strom ist, und ein frequenzabhängiges Netzwerk (15, 16) zum Erhalten der gewünschten Frequenzabhängigkeit der Übertragungskennlinie der Schutzschaltung sowie von einem Pufferverstärker (14) enthält (Fig. 7).

3. Verstärkeranordnung nach Anspruch 2, dadurch gekennzeichnet, dass die Detektorschaltung (12a) zur Lieferung eines Ausgangsstroms (i_m) in einer Ausgangstromschaltung (12b) angeordnet ist und das frequenzabhängige

Netzwerk die Serienschaltung aus einem Widerstand (15) und einer Kapazität (16) in der genannten Ausgangsschaltung (12b) enthält, wobei die Spannung an dieser Ausgangsschaltung in einer Strom (i_b) über den Pufferverstärker (14) umgesetzt wird, und dieser Strom (i_b) dem Eingang des zweiten Verstärkerabschnitts zugeführt wird. (Fig. 7).

4. Verstärkeranordnung nach Anspruch 3, dadurch gekennzeichnet, dass eine Stromquelle (28) parallel zur genannten Serienschaltung (15, 16) angeordnet ist und eine Einrichtungsklemmschaltung (T_{17}) am Ausgang der Detektorschaltung angeordnet ist, wobei die Klemmschaltung (T_{17}) den Eingang des Pufferverstärkers (14) auf einem festen Potential klemmt, so lange der Ausgangsstrom (i_m) der Detektorschaltung den Strom (I_r) von der Stromquelle (28) nicht überschreitet (Fig. 8).

5. Verstärkeranordnung nach einem oder mehreren der vorangehenden Ansprüche, mit einem zweiten Ausgangstransistor (T_B), der mit dem ersten Ausgangstransistor (T_A) im Gegentakt gesteuert wird, der neben der Schutzschaltung (13) eine zweite Schutzschaltung (13a) für den Überlastungsschutz des zweiten Ausgangstransistor (T_B) enthält, und wobei der erste Verstärkerabschnitt (10) ein differentielles Paar (T_1 , T_2) enthält, dessen Kollektorsignalströme dem zweiten Verstärkerabschnitt (11) in Gegenphase zugeführt werden, dadurch gekennzeichnet, dass der Ausgang der eine Schutzschaltung (13) mit der Kollektorschaltung eines Transistors (T_2) des differentiellen Paares (T_1 , T_2) und der Ausgang der anderen Schutzschaltung (13a) mit der Kollektorschaltung des anderen Transistors (T_1) des differentiellen Paares (T_1 , T_2) verbunden ist. (Fig. 9).

Revendications

1. Montage amplificateur muni d'un premier étage amplificateur (10) présentant une entrée (2) et une sortie (3), d'un second étage amplificateur (11) présentant une entrée qui est connectée à la sortie (3) du premier étage amplificateur (10), d'une sortie (8), d'au moins un premier transistor de sortie et d'un premier transistor d'excitation pour l'excitation dudit transistor de sortie, ce second étage amplificateur (11) étant compensé en fréquence et présentant une amplification, qui décroît à une vitesse de 6 dB/octave à partir d'une première fréquence angulaire à une seconde fréquence angulaire au-dessus d'une troisième fréquence angulaire, alors que l'amplification à boucle ouverte du montage amplificateur est égale à l'inverse du taux de réaction négative maximal auquel le montage amplificateur fonctionne sans instabilités, et d'un circuit de protection (13) pour la protection contre une surcharge dudit transistor de sortie, circuit de protection (13) qui constitue une boucle autour du second étage amplificateur (11) et qui agit sur l'entrée (3) de ce second étage amplificateur (11), caractérisé en ce que le circuit de protection (11) a une réponse de



fréquence présentant une première partie, qui décroît à fréquence croissante pour une première gamme de fréquences, et une seconde partie, qui est indépendante de la fréquence pour une seconde gamme de fréquences au-dessus de la première gamme et qui se situe autour d'une quatrième fréquence angulaire, qui est inférieure à la troisième fréquence angulaire, le module de l'amplification de boucle à ladite quatrième fréquence angulaire par le deuxième étage amplificateur atteignant la valeur de l'unité lorsque le circuit de protection est à l'état active (figure 4).

2. Montage amplificateur selon la revendication 1, caractérisé en ce que le circuit de protection comporte un circuit de détection (12^a) pour l'amenée d'un signal qui est une mesure de la tension et/ou du courant traversant le premier transistor de sortie, un réseau dépendant de la fréquence (15, 16) pour la réalisation de la dépendance de fréquence désirée de la caractéristique de transmission du circuit de protection et un amplificateur tampon (14) (figure 7).

3. Montage amplificateur selon la revendication 2, caractérisé en ce que le circuit de détection (12^a) est conçu pour fournir un courant de sortie (i_m) dans un circuit de courant de sortie (12^b) et le réseau dépendant de la fréquence comportant le montage en série d'une résistance (15) et d'un condensateur (16) dans ledit circuit de sortie (12^b), la tension se produisant aux extrémités du circuit de sortie étant convertie en un courant (i_1) par

l'intermédiaire dudit amplificateur tampon (14), courant (i_1) qui est amené à l'entrée du second étage amplificateur (figure 7).

4. Montage amplificateur selon la revendication 3, caractérisé en ce que une source de courant (28) est montée en parallèle avec ledit montage en série (15, 16), et un circuit de blocage unidirectionnel (T_{17}) est monté à la sortie du circuit de détection, circuit de blocage (T_{17}) qui assure le blocage de l'entrée de l'amplificateur tampon (14) à un potentiel relativement fixe aussi longtemps que le courant de sortie (i_m) du circuit de détection ne dépasse pas le courant (I_1) de ladite source de courant (28) (figure 8).

5. Montage amplificateur selon l'une des revendications précédentes, comportant un deuxième transistor de sortie (T_B), qui est excité symétriquement avec le premier transistor de sortie (T_A) et, outre ledit circuit de protection (13) un second circuit de protection (13^a), fournissant une protection contre la surcharge dudit second transistor (T_B) de sortie, et le premier étage amplificateur (10) comporte une paire différentielle, dont les courants de signal de collecteur sont appliqués en opposition de phase au second étage amplificateur, caractérisé en ce que la sortie d'un circuit de protection (13) est couplée au circuit collecteur d'un transistor (T_2) de la paire différentielle (T_1 , T_2) et la sortie de l'autre circuit de protection (13^a) est couplée au circuit de collecteur de l'autre transistor (T_1) de la paire différentielle (T_1 , T_2) (figure 9).

