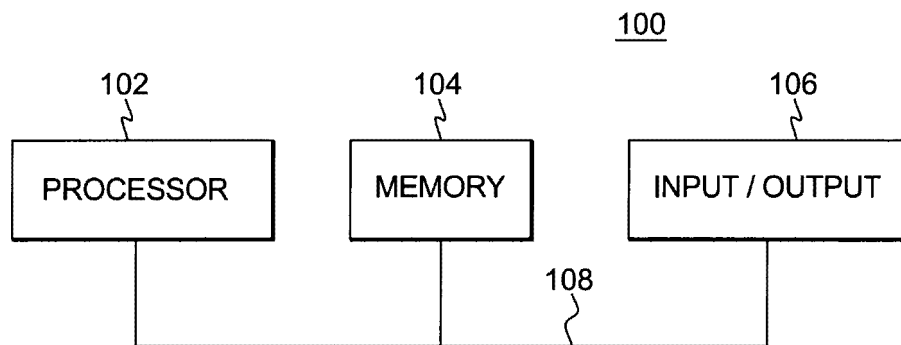
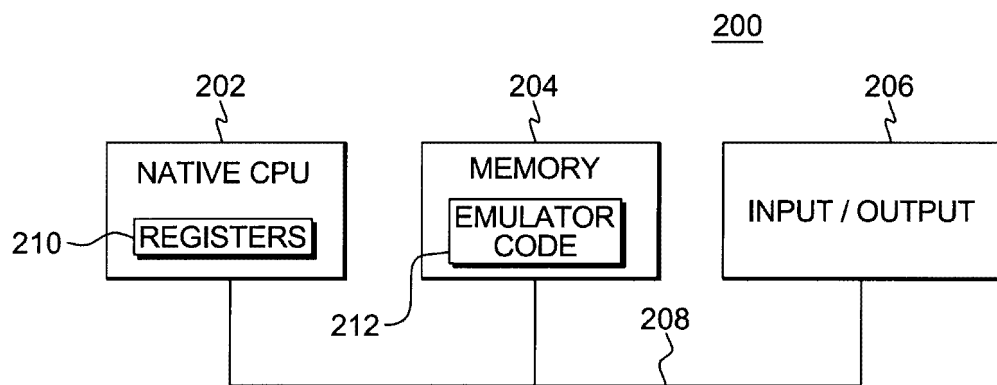
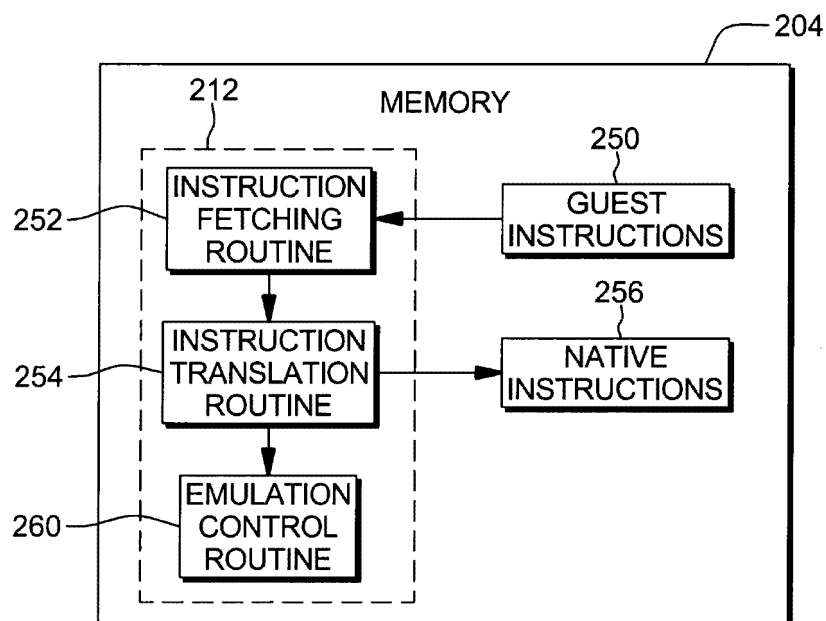


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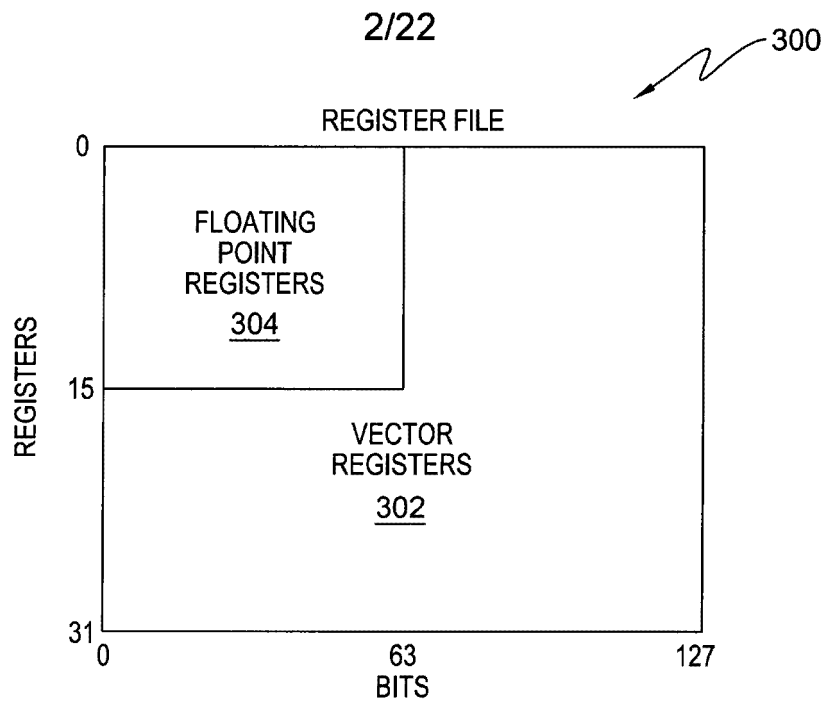


FIG. 3

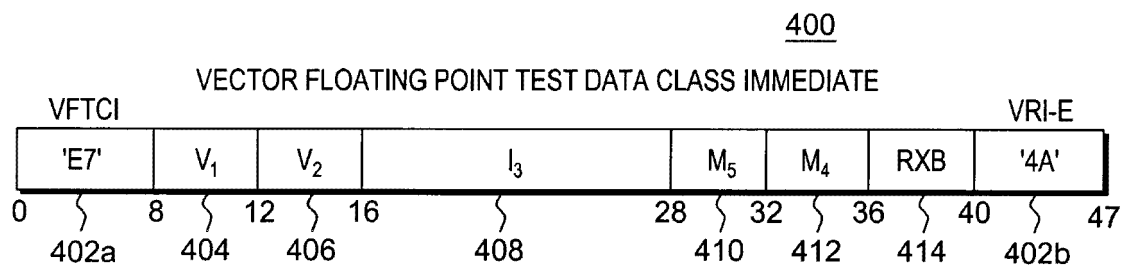


FIG. 4A

430 BFP ELEMENT CLASS	BIT USED WHEN SIGN IS	
	+	-
ZERO	0	1
NORMAL NUMBER	2	3
SUBNORMAL NUMBER	4	5
INFINITY	6	7
QUIET NAN	8	9
SIGNALING NAN	10	11

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FIG. 4B

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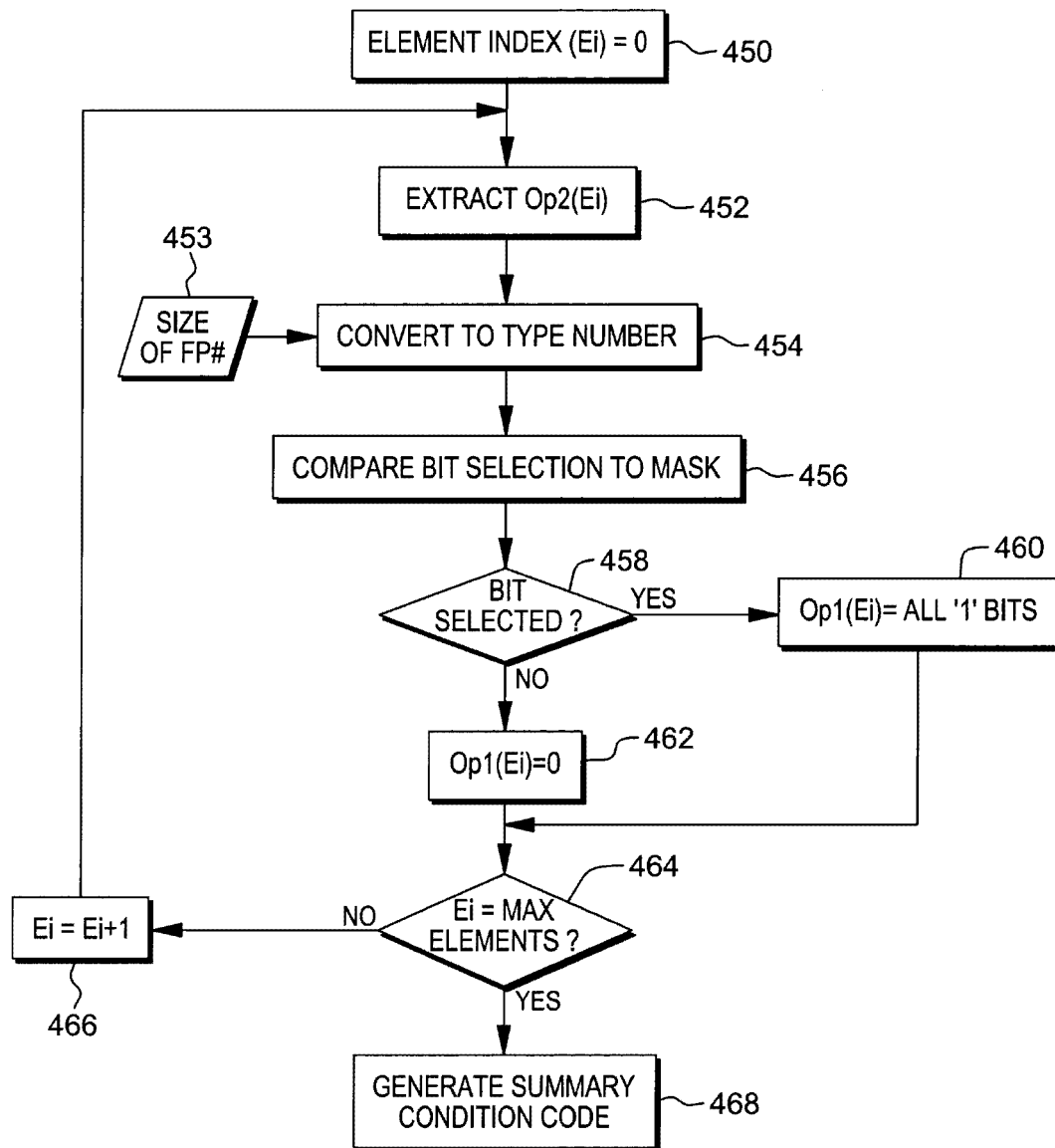


FIG. 4C

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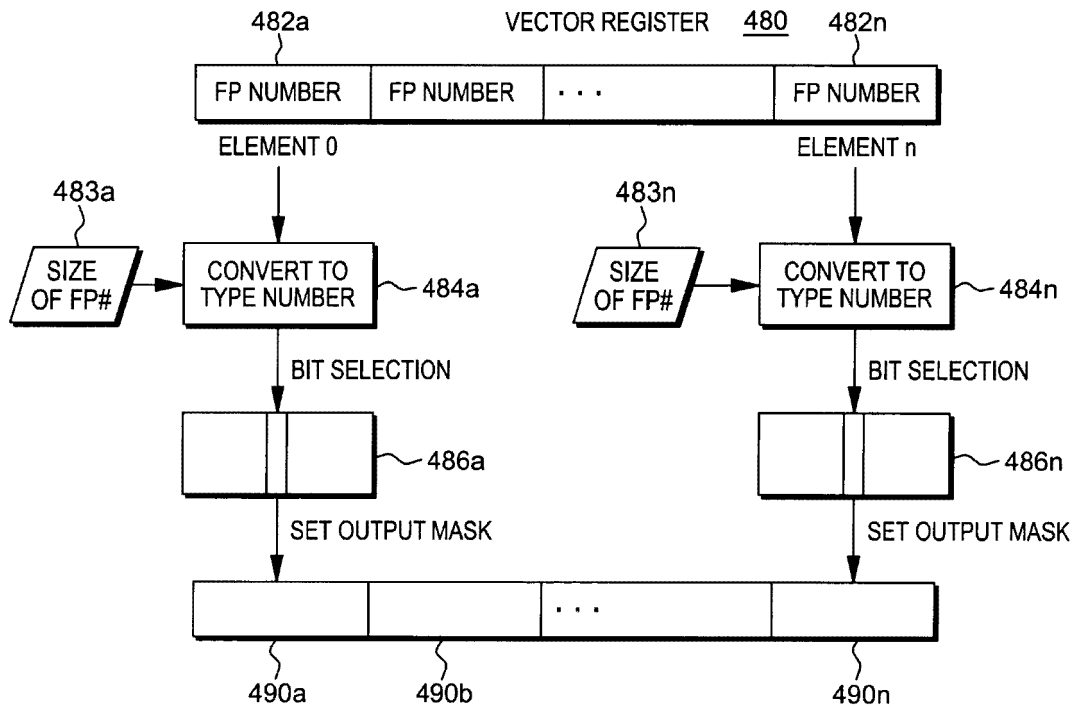


FIG. 4D

ENTITY	SIGN	BIASED EXPONENT	UNIT BIT *	FRACTION
TRUE ZERO	$\pm$	0	0	0
DENORMALIZED NUMBERS	$\pm$	0**	0	NOT 0
NORMALIZED NUMBERS	$\pm$	NOT 0, NOT ALL ONES	1	ANY
INFINITY	$\pm$	ALL ONES	-	0
QUIET NAN	$\pm$	ALL ONES	-	FO=1, Fr=ANY
SIGNALING NAN	$\pm$	ALL ONES	-	FO=0, Fr $\neq$ 0
EXPLANATION:				
* THE UNIT BIT IS IMPLIED				
** THE BIASED EXPONENT IS TREATED ARITHMETICALLY AS IF IT HAD THE VALUE ONE				
NAN NOT A NUMBER				
FO LEFTMOST BIT OF FRACTION				
Fr REMAINING BITS OF FRACTION				

FIG. 4E

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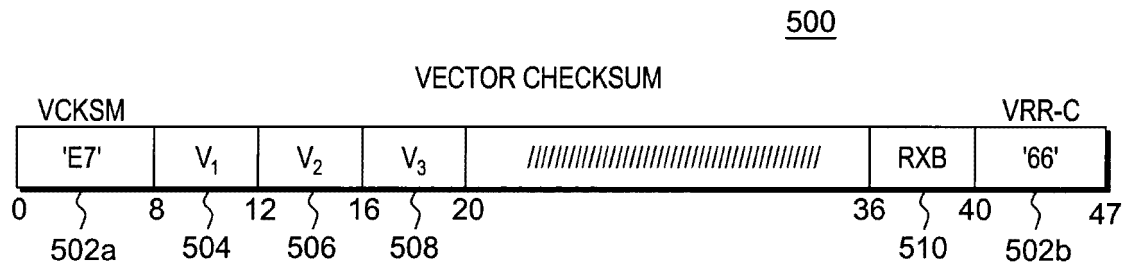


FIG. 5A

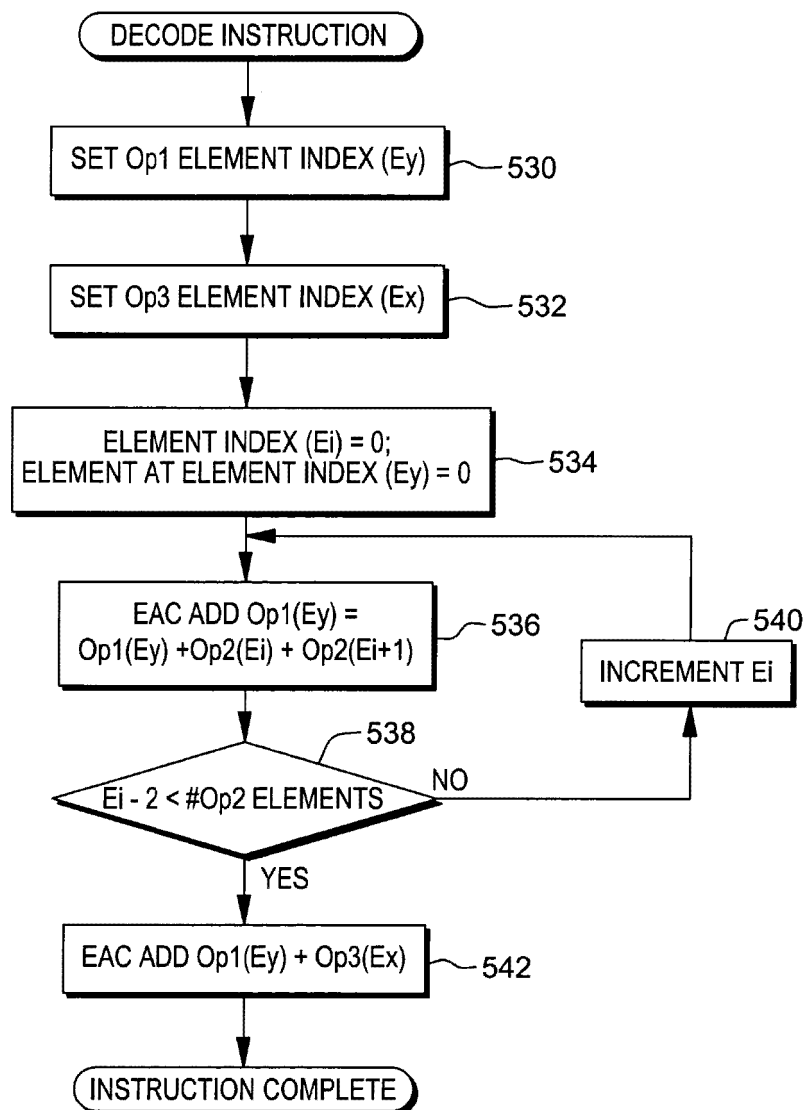


FIG. 5B

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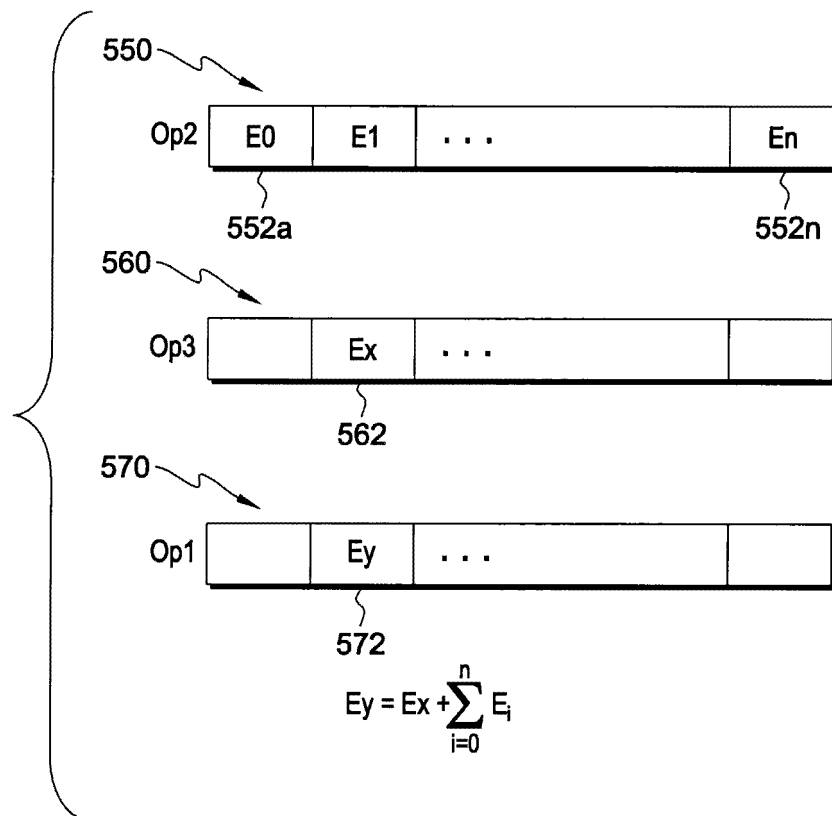


FIG. 5C

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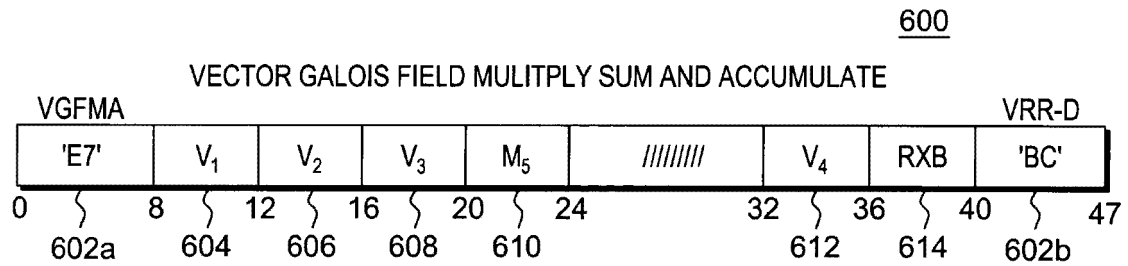


FIG. 6A

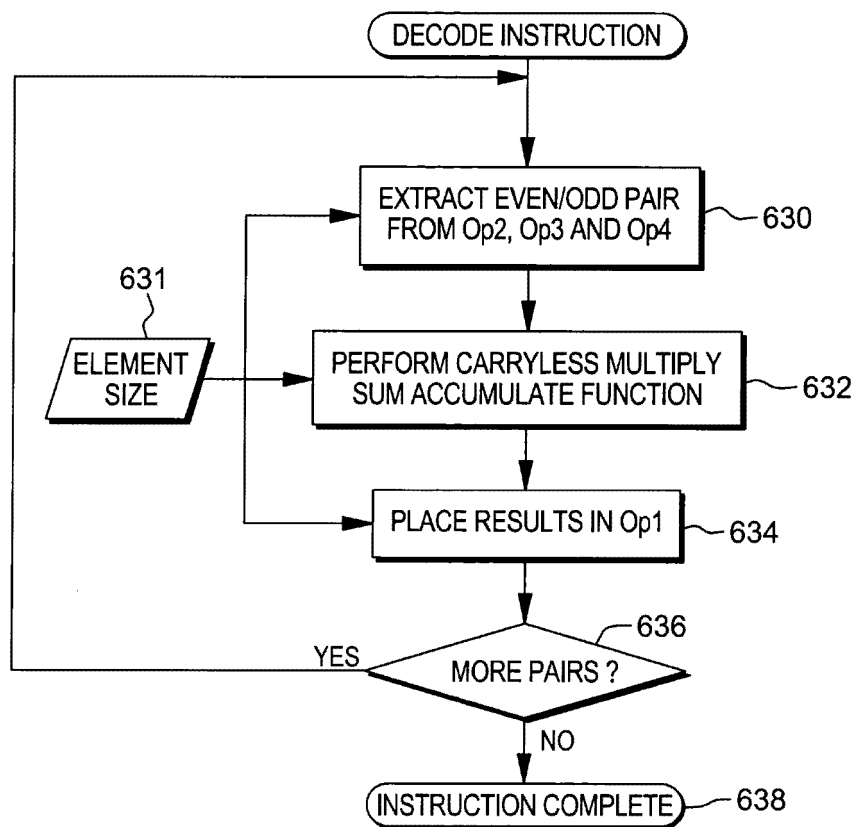


FIG. 6B

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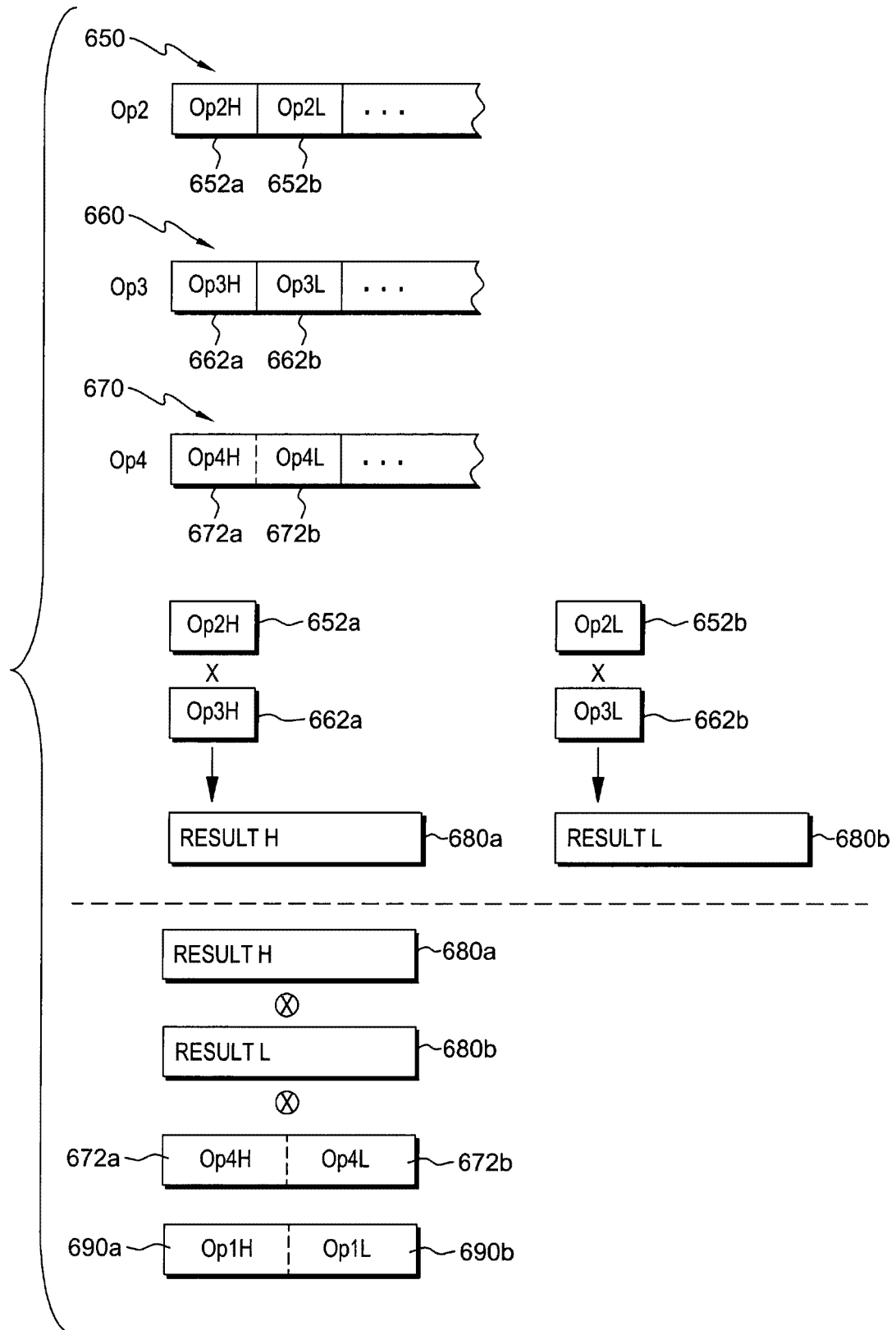


FIG. 6C

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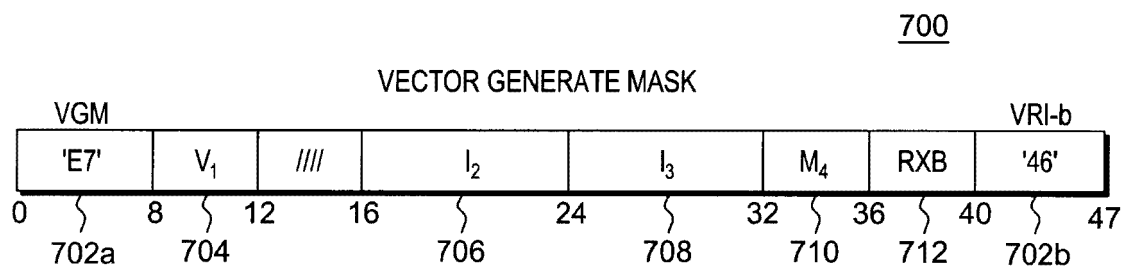


FIG. 7A

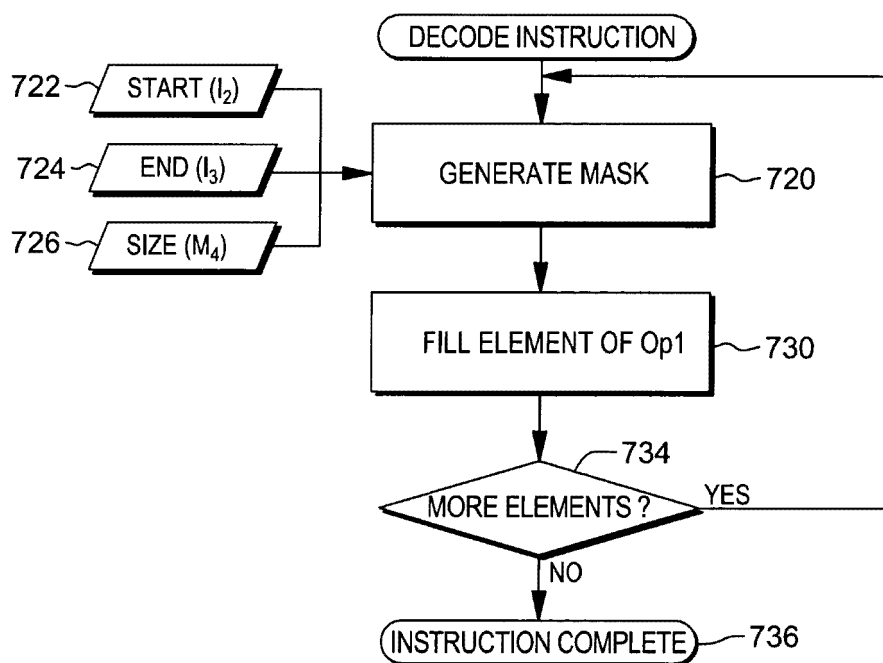


FIG. 7B

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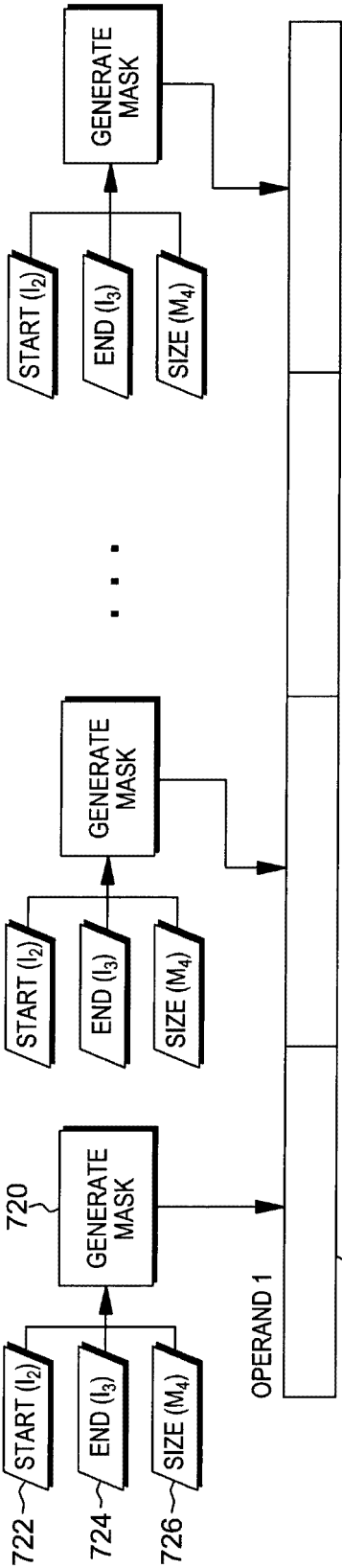


FIG. 7C

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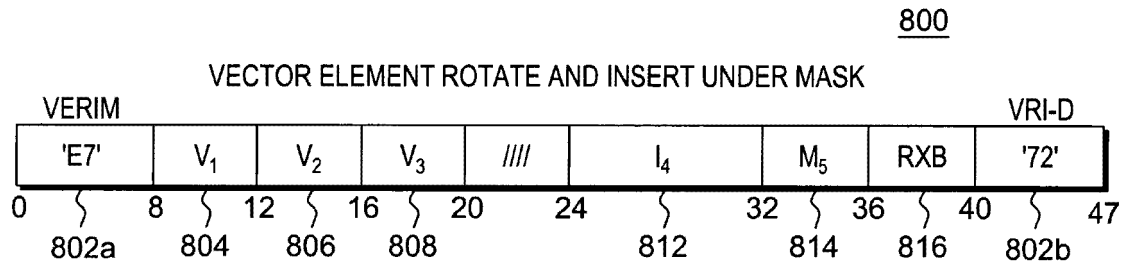


FIG. 8A

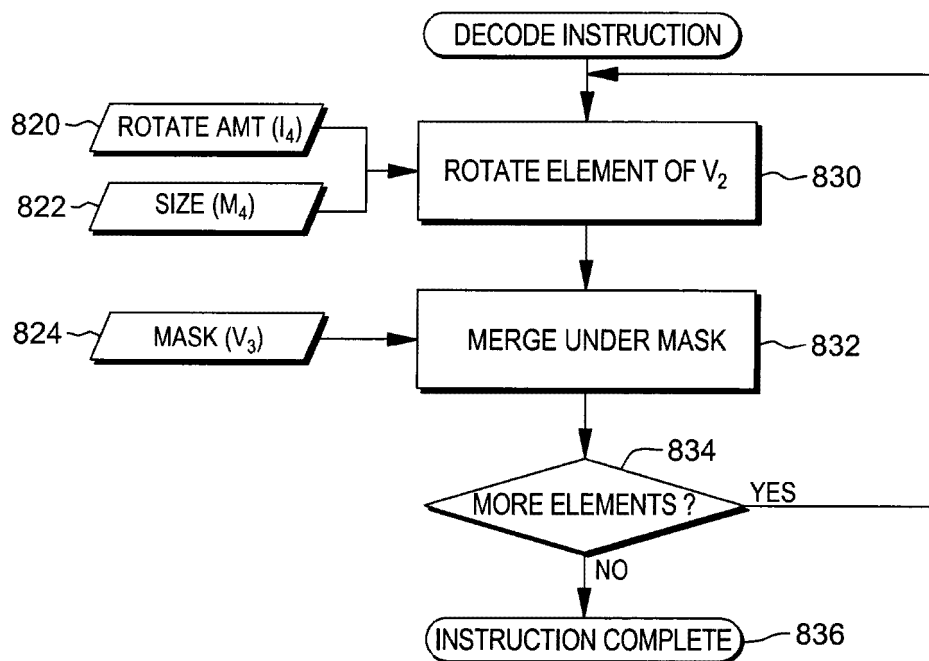


FIG. 8B

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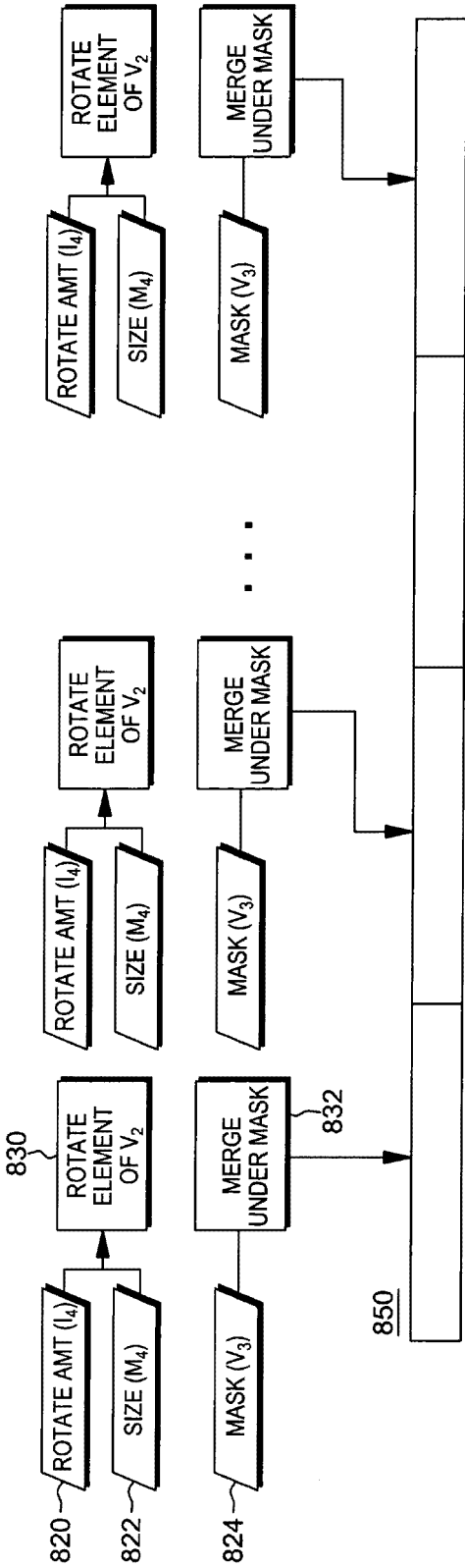


FIG. 8C

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VECTOR EXCEPTION CODE

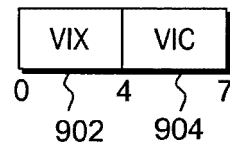


FIG. 9A

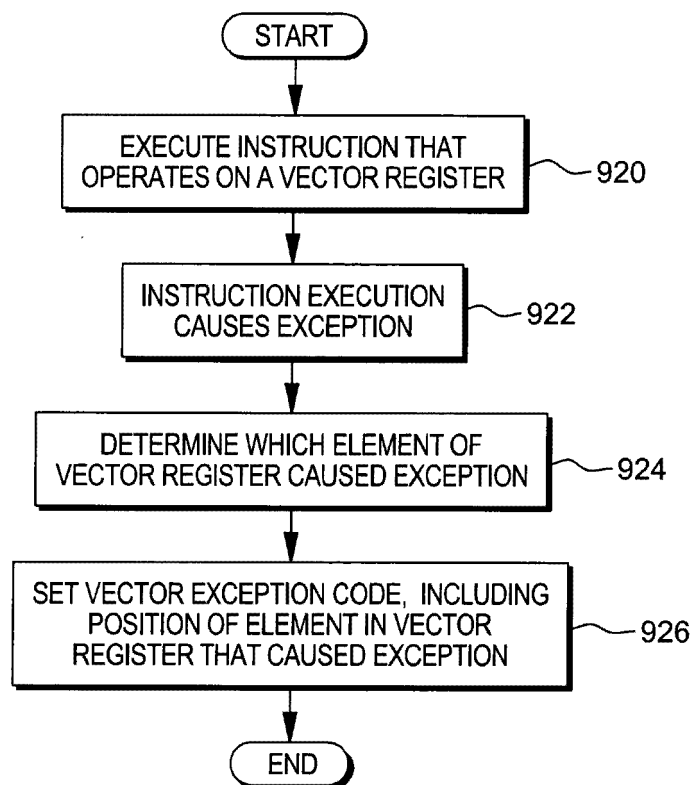


FIG. 9B

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COMPUTER
PROGRAM
PRODUCT
1000

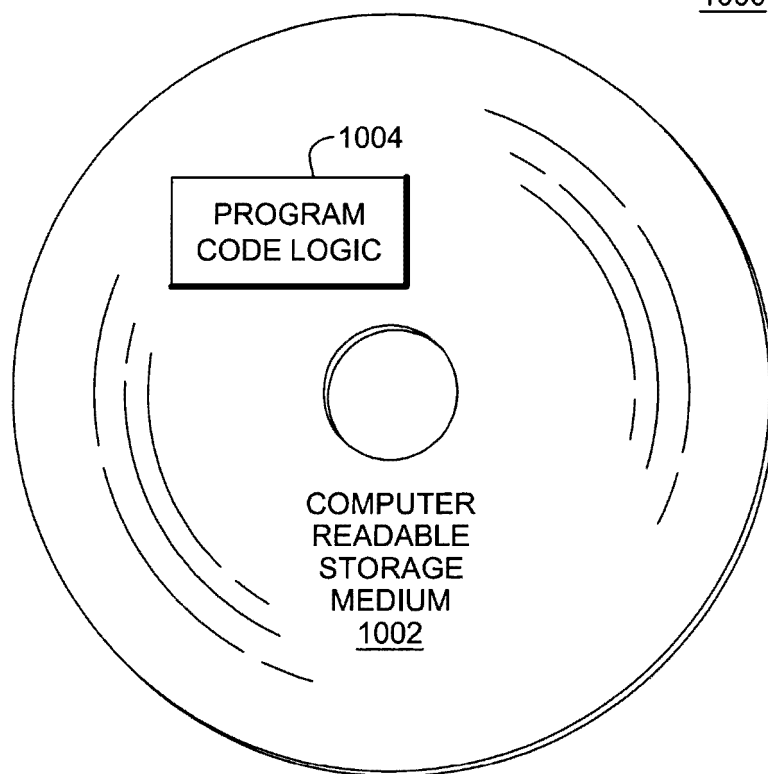


FIG. 10

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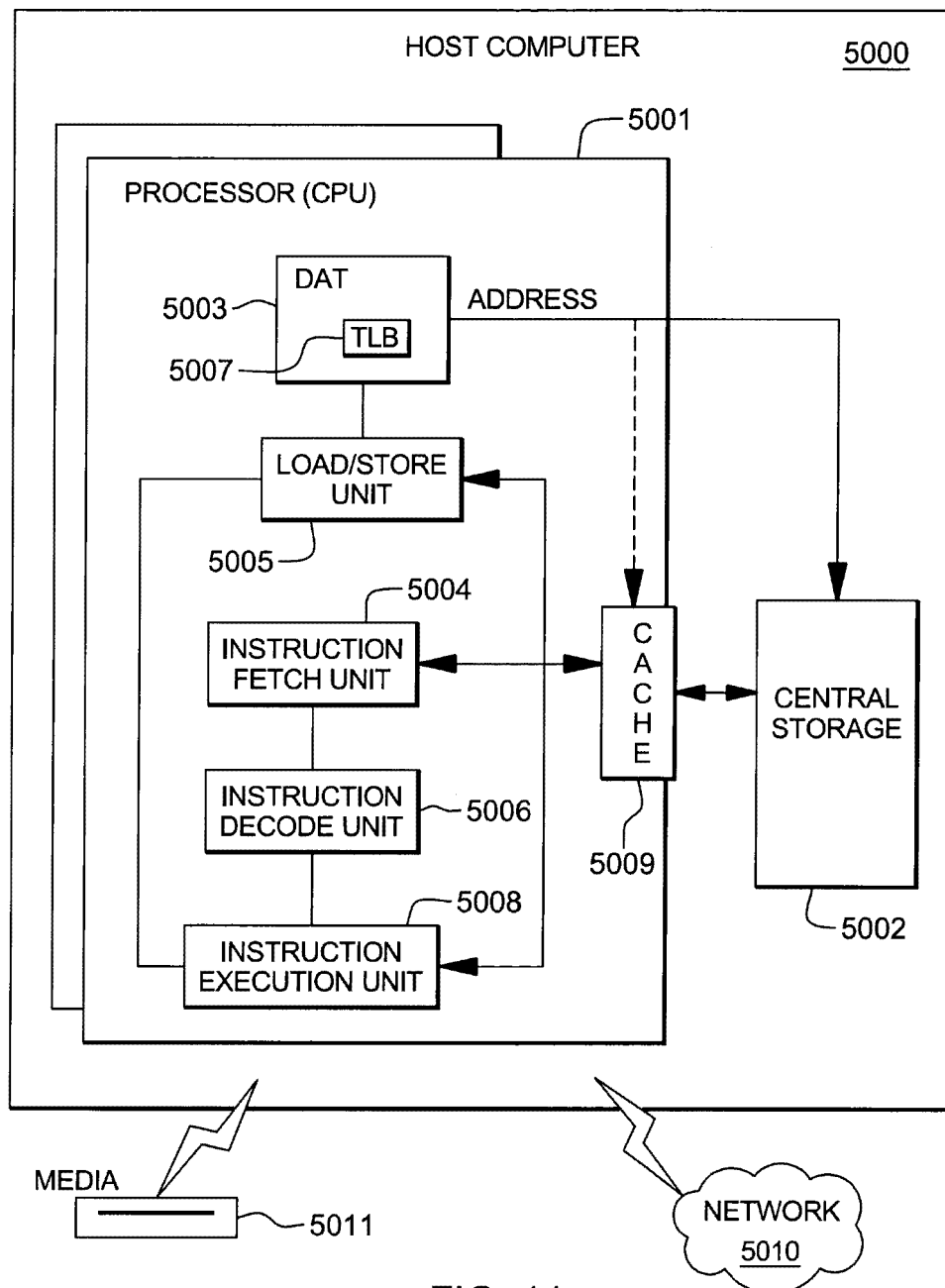


FIG. 11

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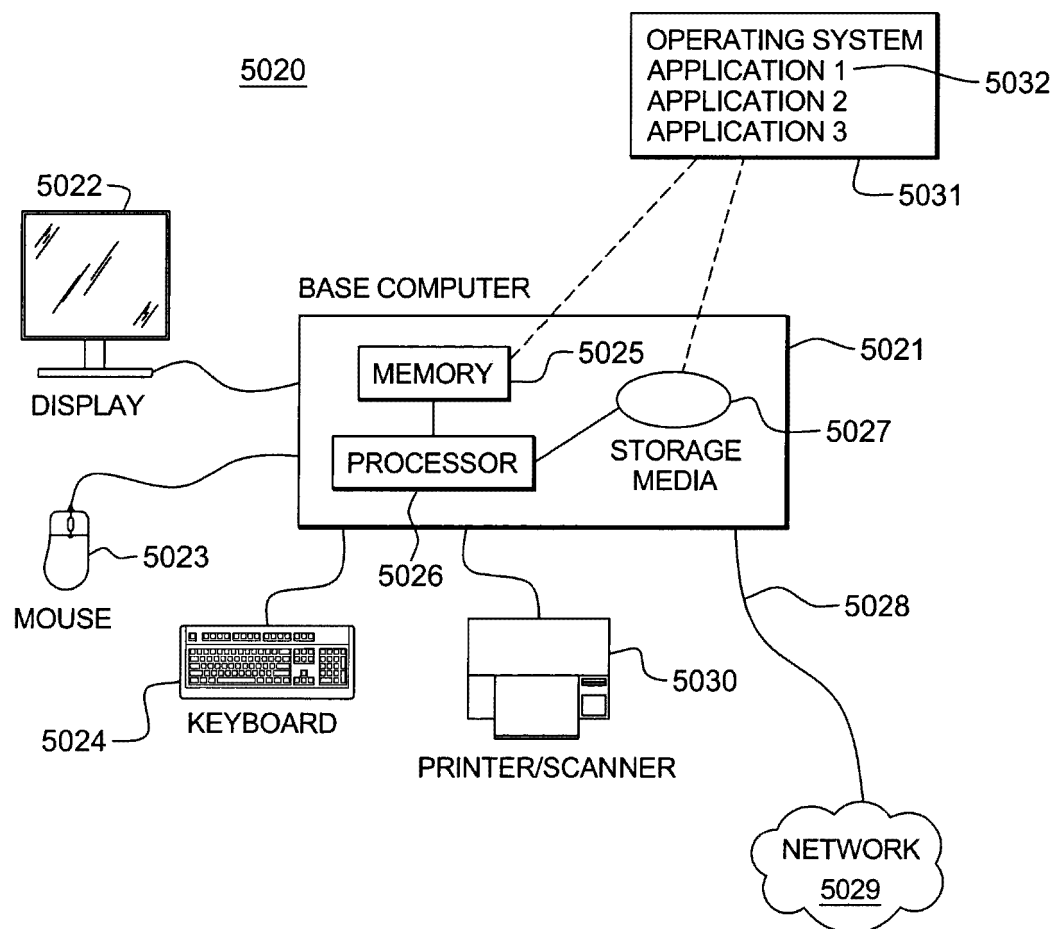


FIG. 12

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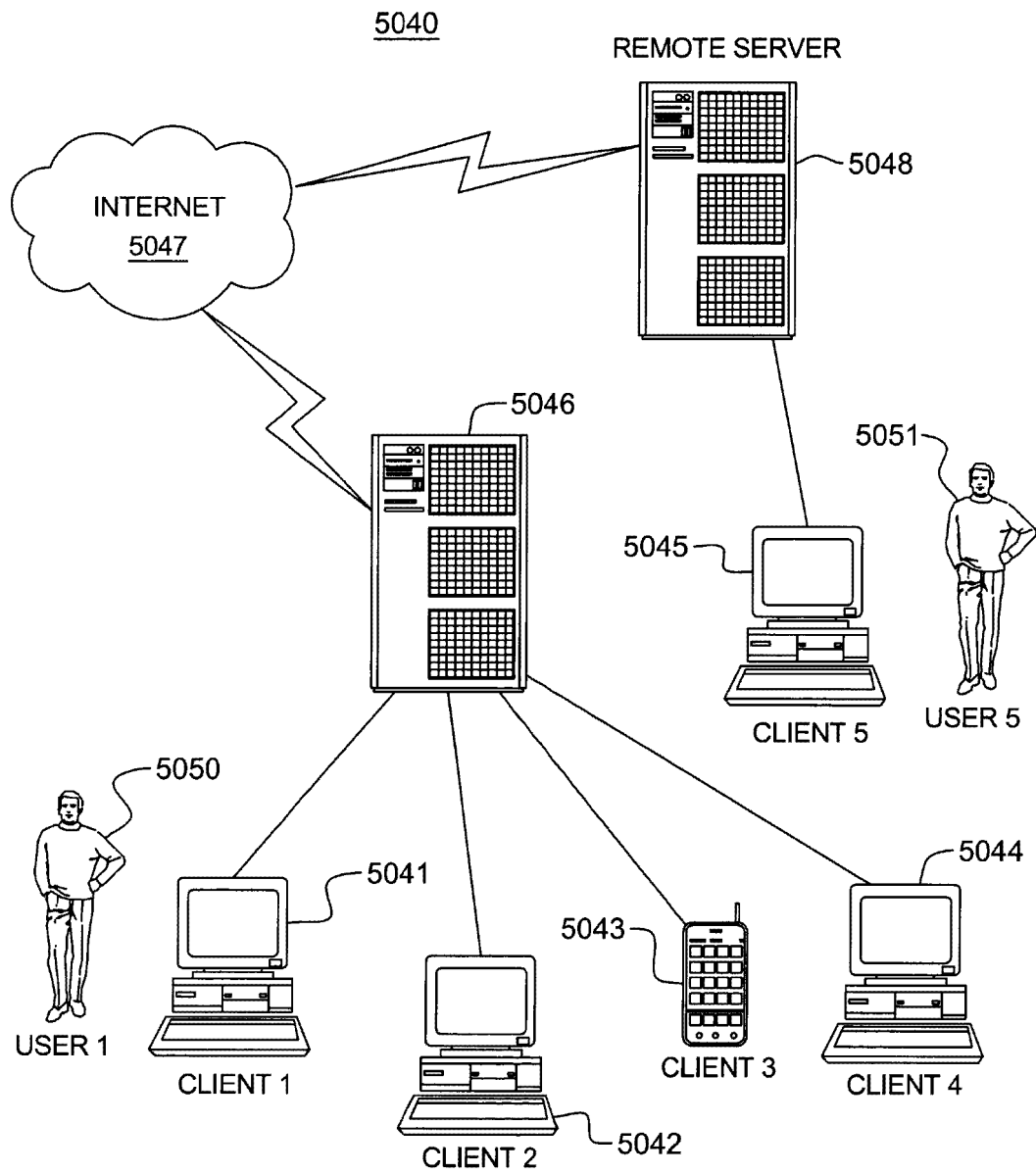


FIG. 13

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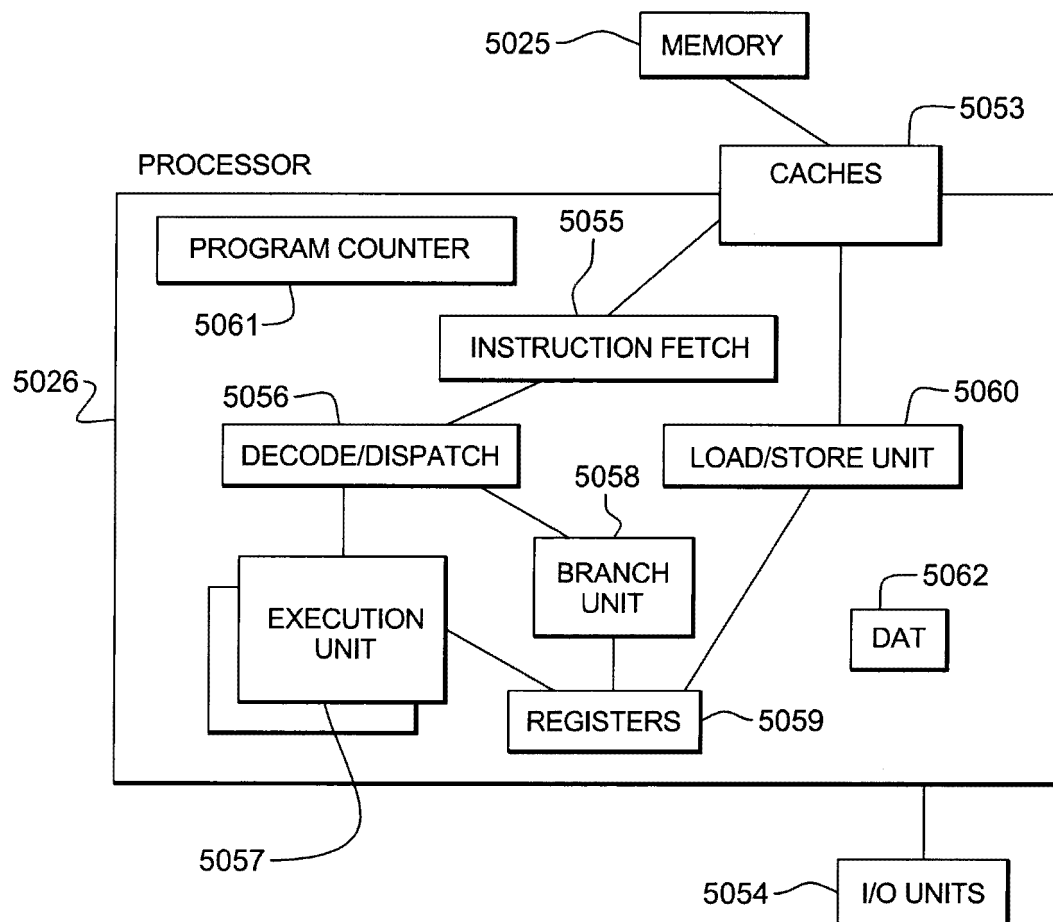


FIG. 14

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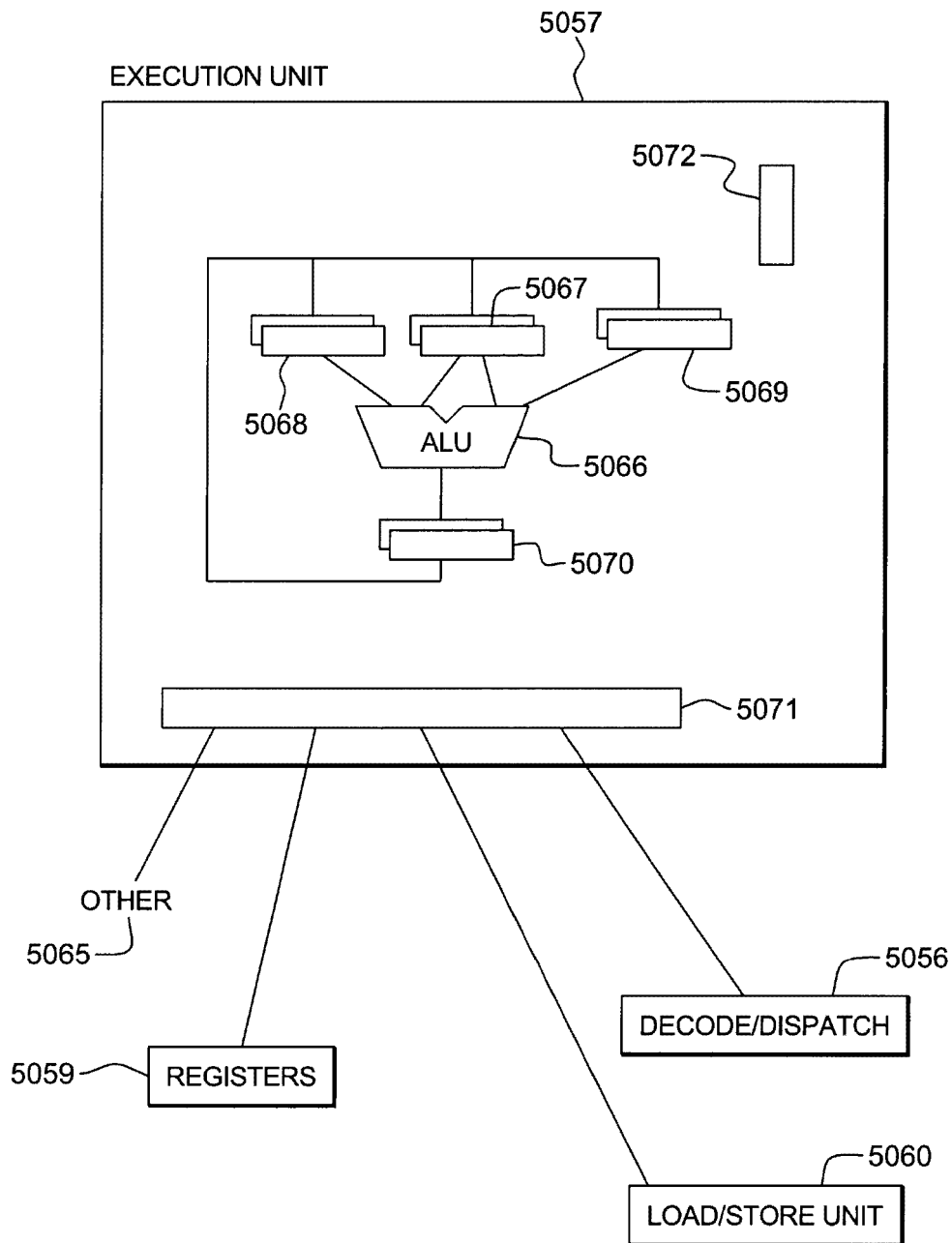


FIG. 15A

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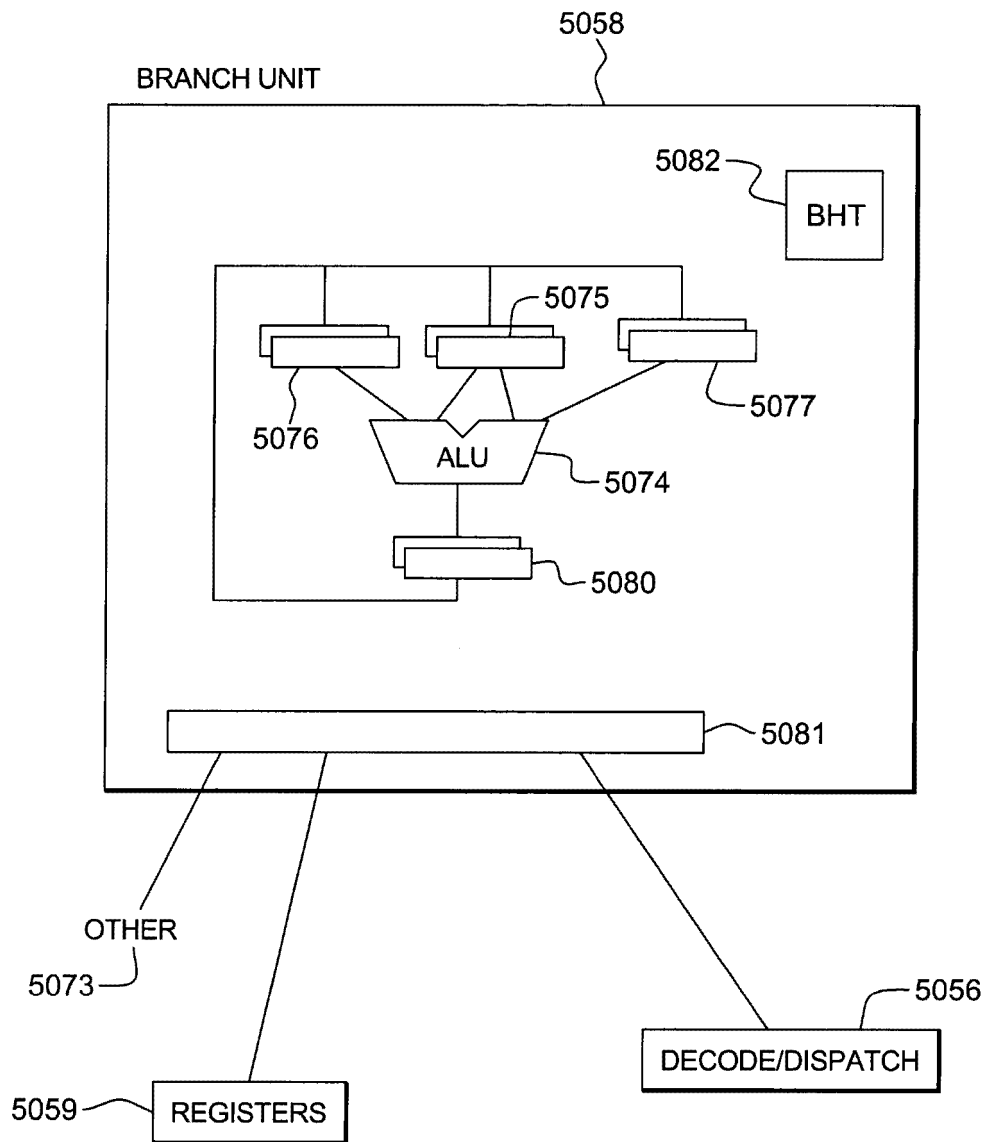


FIG. 15B

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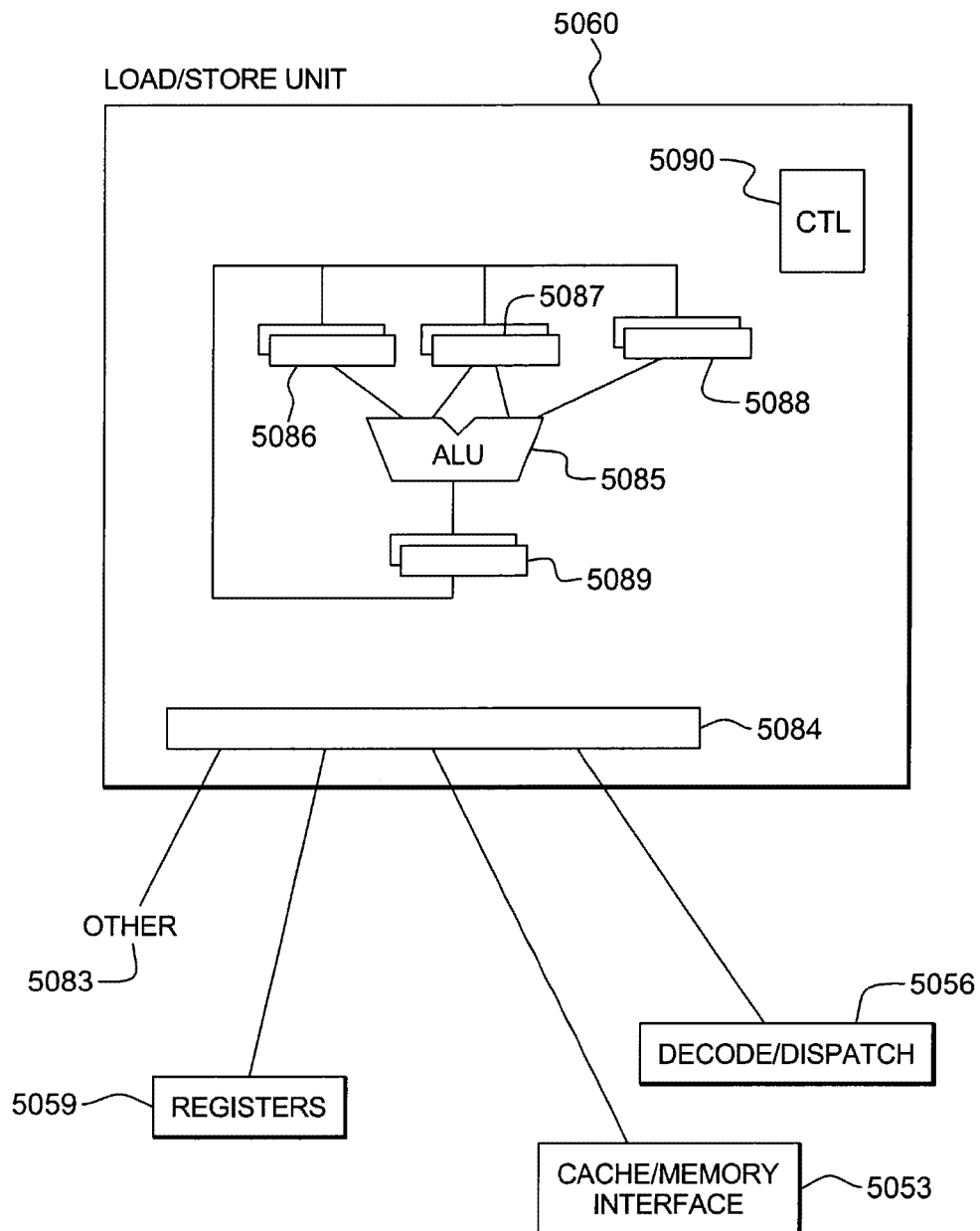


FIG. 15C

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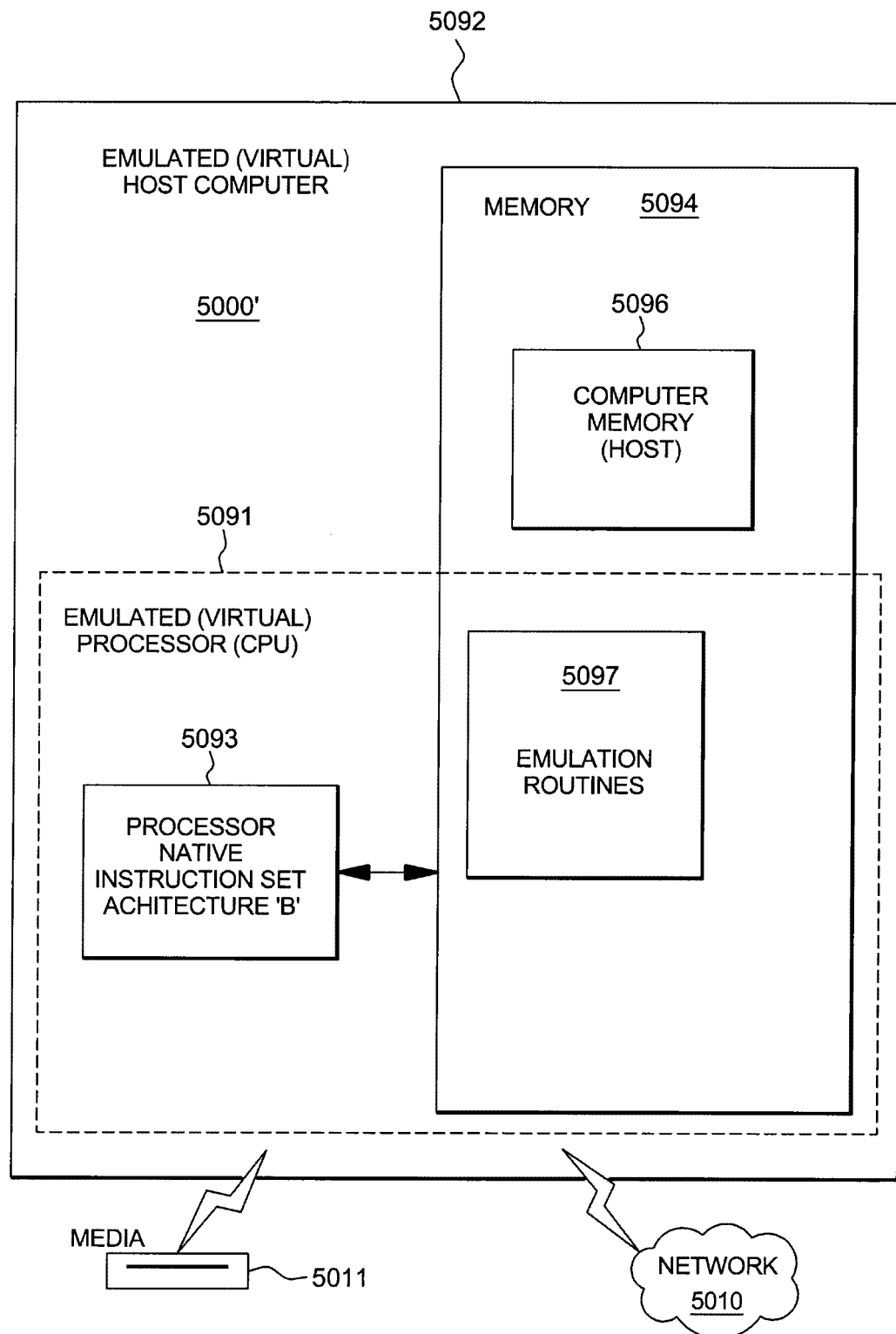


FIG. 16