

MAXIMUM SEARCH CIRCUIT

BACKGROUND

The present invention generally relates to methods and apparatus for digital signal processing or computational operations.

It is sometimes desired to find the greatest of a set of values that may be electrically stored as a set of digital words in memory elements such as registers, random access memory ("RAM") or read-only memory ("ROM"). Also, it is often desired to identify the largest such value, e.g., by finding its associated index number, which may be the number of the memory element in which the largest value is stored.

A common method for finding the largest of a set of values involves sequentially scanning the set. A register for storing the largest value is loaded with the first value (and its index), and the contents of the register is compared to the second value. If the second value is larger, the second value and its index replace the first value and its index in the register. The third value is then compared to the register contents, and if it is larger, the third value and its index replace the value and index stored in the register. The process continues until all subsequent values in the set have been compared to the register contents.

Unfortunately, the amount of time needed for such a sequential search is proportional to the number of values in the set; thus, a sequential search may be too slow when the set is large. As described in more detail below, the present invention provides a fully parallel search method and circuit implementation using bit-serially presented digital values that determine the maximum value and its index in a time period that is independent of the number of values in the set searched.

The present invention is particularly useful for code division multiple access ("CDMA") communications

techniques in cellular radio telephone communication systems, such as the enhanced CDMA demodulation scheme based on successive signal subtractions, in signal strength order, of multiple CDMA signals that is described in co-pending U.S. Patent Application Serial No. 07/628,359, filed December 17, 1990.

In that co-pending patent application, it is explained that superior methods of spectrally spreading an information signal, such as occurs in a CDMA system, use error correction coding. When a single information bit is expanded into a pseudo-random sequence of R bits, the information bandwidth is spread without error-correction-coding gain; this technique may be termed "simple spreading". On the other hand, spreading a block of M information bits, where $M > 1$, into a pseudo-random sequence of $M \times R$ bits provides an error correction coding gain of the spreading ratio R . This technique, called "intelligent spreading", can involve either orthogonal or bi-orthogonal block coding of the information signal to be transmitted.

In orthogonal block coding, M bits to be transmitted are converted to one of 2^M available 2^M -bit orthogonal codewords. Decoding involves correlating a received signal with all members of the set of orthogonal codewords, and the index of the codeword giving the highest correlation yields the desired information. For example, if a signal's correlation with sixteen 16-bit codewords index-numbered 0 to 15 produces the highest correlation on the tenth codeword, the desired signal information is the 4-bit binary word 1010 (decimal 10).

A comparison processor may determine which correlation has the largest magnitude and may set that signal to zero by opening a corresponding switch. In this manner, the demodulated signal is subtracted effectively from the composite signal. The remaining spectrum with one component removed is processed and re-scrambled to reconstruct the original signal samples

less the just-decoded signal. The magnitude of the correlated signal is representative of signal strength and may be stored in a sorting processor along with the signal's corresponding scrambling code. The processor
5 orders the scrambling codes from greatest to weakest correlated signal magnitudes, and the code corresponding to the greatest magnitude may then be transmitted to the descrambler for the next signal demodulation.

10 Thus, after the comparison processor detects real and imaginary correlations and determines complex correlation magnitudes by calculating the square root of the sum of the squares of the real and imaginary components, the processor may then determine which
15 complex correlation has the greatest magnitude. The real and imaginary components of the selected correlation may also be analyzed in the complex plane to determine if the phase has changed.

According to a first aspect of the present
20 invention, there is provided an electronic comparator for selecting and outputting a larger of first and second electrical, binary-coded input values presented bit-serially, most-significant-bit first, comprising:

first and second input terminals for receiving,
25 respectively, the first and second input values;

comparison means, operatively connected to the first and second input terminals, for comparing a serial input bit of the first input value with a bit of like significance from the second input value, and for
30 generating as an output a signal alternatively indicating a like or unlike comparison result;

first latching means, operatively connected to the output of the comparison means, for registering a first occurrence of the unlike comparison result generated by
35 the comparison means and for generating a trigger pulse in response to the first occurrence of the unlike

comparison result;

second latching means, operatively connected to the first latching means and the first input terminal, for latching the serial input bit of the first input value in response to the trigger pulse and for providing the latched serial input bit at an output;

first selecting means, operatively connected to the first and second input terminals and the second latching means, and responsive to the output of the second latching means for selecting one of the input values as an output of the electronic comparator, wherein the first selecting means selects the first input value when the latched serial input bit is a "1" state, and the first selecting means selects the second input value when the latched serial input bit is a "0" state.

According to a second aspect of the present invention, there is provided an electronic comparator for selecting and outputting a larger of first and second electrical, binary-coded input values presented bit-serially, most-significant-bit first, comprising:

first and second input terminals for receiving, respectively, the first and second input values;

comparison means, operatively connected to the first and second input terminals, for comparing a serial input bit of the first input value with a bit of like significance from the second input value, and for generating as an output a signal alternatively indicating a like or unlike comparison result;

first latching means, operatively connected to the output of the comparison means, for registering a first occurrence of the unlike comparison result generated by the comparison means and for generating a trigger pulse in response to the first occurrence of the unlike comparison result;

second latching means, operatively connected to

the first latching means and the first input terminal, for latching the serial input bit of the first input value in response to the trigger pulse and for providing the latched serial input bit at an output;

5 first selecting means, operatively connected to the first and second input terminals and the second latching means, and responsive to the output of the second latching means for selecting one of the input values as an output of the electronic comparator,
10 wherein the first selecting means selects the logical OR of the first and second input values as the output when the first latching means has not registered the first occurrence of the unlike comparison result, and the first selecting means selects the first input value
15 as the output when the second latching means is set to "1", and the first selecting means selects the second input value as the output when the second latching means is set to "0".

According to a third aspect of the present
20 invention, there is provided an electronic logic circuit for selecting and outputting a maximum of a plurality of electrical binary-coded values comprising:

a plurality of electronic comparators for selecting and outputting a larger of first and second
25 electronic comparator input values, the first and second electronic comparator input values being binary-coded input values presented bit-serially, most-significant-bit first, the plurality of electronic comparators being tree-connected to form a tree of
30 electronic comparators and each electronic comparator including:

first and second input terminals for receiving, respectively, the first and second electronic comparator input values;

35 comparison means, operatively connected to the first and second input terminals, for comparing a

serial input bit of the first electronic comparator
input value with a bit of like significance from the
second electronic comparator input value, and for
5 generating as an output a signal alternatively
indicating a like or unlike comparison result;

first latching means, operatively connected to the
output of the comparison means, for registering a first
occurrence of the unlike comparison result generated by
10 the comparison means and for generating a trigger pulse
in response to the first occurrence of the unlike
comparison result;

second latching means, operatively connected to
the first latching means and the first input terminal,
15 for latching the serial input bit of the first
electronic comparator input value in response to the
trigger pulse and for providing the latched serial
input bit at an output, wherein the output from the
second latching means is a traceback signal for
20 indicating which of the first and second electronic
comparator input values was selected; and

first selecting means, operatively connected to
the first and second input terminals and the second
latching means, and responsive to the output of the
25 second latching means for selecting one of the
electronic comparator input values as an output of the
electronic comparator, wherein the first selecting
means selects the first electronic comparator input
value when the latched serial input bit is a "1" state,
30 and the first selecting means selects the second
electronic comparator input value when the latched
serial input bit is a "0" state,

wherein pairs of the plurality of values are
presented bit-serially, most-significant-bit first, to
35 respective first ones of the electronic comparators
disposed in a first stage of the tree, each first
electronic comparator outputting a larger of the first

and second electronic comparator input values as a first-stage output signal and outputting its traceback signal as a first-stage traceback signal, the first-stage output signals being presented bit-serially, most-significant-bit first, to respective second ones of the electronic comparators disposed in a second stage of the tree, and so forth for subsequent stages of the tree until the maximum of the input values is passed as an output signal from a last electronic comparator disposed in a last stage of the tree, and the first-stage traceback signals being presented to respective second ones of the electronic comparators disposed in a second stage of the tree, each second electronic comparator including means for selecting either the first traceback signal associated with the second electronic comparator's first electronic comparator input value or the first traceback signal associated with the second electronic comparator's second electronic comparator input value, and so forth for subsequent stages of the tree.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the invention will be understood after reading the following detailed description in conjunction with the drawings, in which:

Figure 1 illustrates a binary tree structure for finding the greatest of eight values;

Figure 2A is a block diagram of one embodiment of a bit-serial, most-significant-bit-first comparator in accordance with the present invention;

Figure 2B is a block diagram of a structure of the comparator of Figure 2A for finding the greatest of eight values;

Figure 3 is a block diagram of another embodiment of a comparator in accordance with the present invention; and

Figure 4 is a diagram of a means for generating a

signal that indicates that the maximum value has been identified.

DETAILED DESCRIPTION

5 While portions of the present description are given in a context of cellular communications systems involving portable or mobile radio telephones and/or personal communication networks, it will be understood by those skilled in the art that the present invention
10 may be used in other applications. In addition, binary values that are always positive, with 00...0 being the smallest value and 11...1 being the largest value, are described, but it will be understood that the description is readily adapted to other binary formats.

As an aid in understanding the present invention, a process or apparatus for determining the greatest (or the least, for that matter) of a set of M values can be visualized as a binary tree that is symmetric, or
5 regular, when $M = 2^N$. For example, when $M = 8$ as shown in Figure 1, pairs of the M input values V_0-V_7 are compared in a first stage of a tree 10 having $M/2 = 4$ comparators 11-1 to 11-4; the larger value of each pair is selected and passed to a second stage having $M/4 = 2$ comparators
10 12-1, 12-2. The larger values of the two pairs are passed to the final, third stage having $M/8 = 1$ comparator 13, which passes the largest value V_{MAX} to its output. It will be appreciated that the number of stages needed for searching the M input values is just N .

15 Even sets of input values generating asymmetric trees can be efficiently processed by a tree structure like that shown in Figure 1 but in which appropriate ones of the comparators are absent. For example, if only input values V_0-V_4 were presented in Figure 1, the
20 comparators 11-3, 11-4 and 12-2 could be eliminated and the input value V_4 could be presented directly to the comparator 13. Alternatively, an asymmetric tree can be made symmetric by padding with a sufficient number of input zeroes or other known values. For the previous
25 example, the input values V_5-V_7 could be set to zero and presented to the tree 10 shown in Figure 1.

In one aspect of the invention, the tree structure is advantageously implemented by a suitable number of comparators that each compare two input values presented
30 bit-serially, most-significant-bit ("MSB") first, and pass the larger of the two with substantially no delay. Such comparators stand in marked contrast to conventional comparators that are based on bit-serial subtraction and compare values presented least-significant-bit first. In
35 another aspect of the invention, each comparator generates a traceback bit for identifying the larger of its input values and passes traceback bits for

identifying the comparators in the preceding stages that were deemed to have furnished the larger input values. It will be appreciated that such bit-serial, MSB-first comparators can be implemented in a suitable, otherwise conventional, integrated circuit.

Figure 2A illustrates one embodiment of a bit-serial, MSB-first comparator 100 according to the present invention that could implement the tree of Figure 1. A pair of binary-coded values are presented bit-serially, MSB first, on inputs A and B to an otherwise conventional exclusive-OR ("XOR") gate 102 that produces a logic HIGH, or "1", output when the values on inputs A and B are unequal. Since the pair of input values are presented and compared bit by bit, MSB first, the input value having the binary "1" will be recognized as the larger on the first occasion that two unlike bits are encountered. (It will be appreciated that as long as the input bits are the same, it cannot be known which value is the larger, but in that case it does not matter which of the two inputs is passed to the output.)

When the output of the XOR gate 102 goes HIGH, indicating that the inputs A, B, are different, it sets a latch 104 that remains set for the rest of the bits of the pair of input values. The latch 104, which may be a conventional set-reset flip-flop, also has a reset input for a suitable control signal for initializing the latch output to logic LOW, or "0", before the first and between sets of input values. The output of the latch 104 is connected to the clock input of a D-type flip-flop 106; thus, when the output of the latch 104 goes HIGH, the value of one of the inputs (input A, for example) is clocked into the flip-flop 106.

As seen in Figure 2A, when the A input value is larger than the B input value (e.g., A's MSB is a "1" and B's MSB is a "0"), the Q output of the flip-flop 106 goes HIGH. The Q output acts as a control signal indicated by the dotted line that causes an input-selector switch 108,

such as a field-effect transistor ("FET"), to switch to the "1" position as shown, thereby connecting the A input to the comparator output for the rest of the pair of input values. In the embodiment shown in Figure 2A, the $\bar{Q}$ output of flip-flop 106 is not used.

On the other hand, if the A input is a "0" when the output of the latch 104 goes HIGH, the A input is again clocked into the flip-flop 106, and the Q output goes LOW, causing the input-selector switch 108 to switch to the "0" position. Thus, the B input is connected to the output for the rest of the pair of input values. As noted above, because the input values are presented MSB first, it does not matter which input value is connected to the output before the output of the XOR gate 102 goes HIGH.

It will be appreciated that the Q output of the flip-flop 106 indicates which of the two inputs was selected (i.e., which value was "1"), and thus the Q output is provided as the comparator's traceback signal output C. The binary traceback signal can be used as an index of the larger value by arbitrarily assigning its value "0" to input A and the value "1" to input B, for example.

The comparator 100 may also have an associated traceback-selector switch 110 that may have a plurality of poles (only one is shown in Figure 2A). The state of the switch 110 is also controlled by the Q output of the flip-flop 106, and each pole of the switch 110 passes either an A TRACEBACK or B TRACEBACK signal from comparators in preceding tree stages. The number of poles provided in each traceback-selector switch 110 depends on how many traceback signals are to be passed from the preceding stage and the position of its associated comparator in the binary tree. Thus, a binary tree can be implemented by a suitable plurality of comparators 100 and switches 110 that yields not only the

largest value of a set of input values but also the index of the largest value.

For example, if the largest of $M = 128$ values were to be found, the tree would have seven stages, the first of which would have sixty-four comparators. The first-stage comparators would need no traceback-selector switches, but each would generate one (a first) traceback signal. Thus, the thirty-two second-stage comparators would each have an associated one-pole traceback-selector switch and would each generate a second traceback signal. The sixteen third-stage comparators would each have an associated two-pole traceback-selector switch and would each generate a third traceback signal. This would continue until the seventh stage, in which the one comparator would have a six-pole traceback-selector switch and would generate a seventh traceback signal. The 7-bit traceback word consisting of the traceback signals passed and generated by the seventh stage would then be the index of the largest of the one hundred twenty-eight input values with the symbols "1" and "0" assigned to the comparator inputs as described above.

The symmetric tree 10 of Figure 1 implemented by such comparators and traceback-selector switches is illustrated in Figure 2B. Eight input values V_0 to V_7 are presented to four first stage comparators 11-1 to 11-4, none of which has a traceback-selector switch but each of which generates one of the first traceback signals C_1 -1 to C_1 -4. The outputs of the first stage comparators are fed to the inputs of the two second stage comparators 12-1, 12-2, each of which has a one-pole traceback-selector switch 110-1, 110-2, respectively, for passing one of the pairs of traceback signals C_1 -1, C_1 -2, and C_1 -3, C_1 -4, respectively, and generates second traceback signals C_2 -1, C_2 -2. The outputs of the second stage comparators are fed to the inputs of the third stage comparator 13, which has a double-pole traceback-selector switch 110-3 and generates the third traceback signal C_3 . One pole of

the traceback-selector switch 110-3 passes one of the pair of traceback signals C_2-1 , C_2-2 , and the other pole passes one of the pair of outputs from preceding stage traceback selector switches 110-1, 110-2. The output V_{MAX} of the third stage comparator 13 is the largest of the input values V_0 to V_7 .

It will be appreciated that the apparatus illustrated in Figure 2B outputs and identifies the largest input value in a time no longer than that needed to present them. In fact, the maximal value's identification by the traceback word may be available in significantly less time; for example, a single large-magnitude input value could be identified early. These advantages are potentially available no matter how many input values must be searched. It may sometimes be more efficient from a hardware size and cost point of view, however, to divide large sets of input values into subsets, find the maximal value of each subset, and then find the maximal value of those subset maximal values.

In practice, a binary tree comprised of comparators such as that shown in Figure 2A could suffer from undesirable logic glitches due to varying propagation delays. Accordingly, Figure 3 shows a preferred embodiment of a comparator 100' in accordance with the present invention that avoids such logic glitches. A pair of input binary-coded values are presented bit-serially, MSB first, on inputs A' , B' , to an otherwise conventional XOR gate 102'. Instead of being connected directly to the SET input of a set-reset flip-flop 104' as in the comparator 100, the output of gate 102' is connected to the D-input of a second D-type flip-flop 103'. The flip-flop 103' is clocked by a BITCLOCK signal that is synchronized to the presentation of the input bits. The Q output of the flip-flop 103' is passed to the SET input of the latch 104', the output of which clocks a D-type flip-flop 106' as in comparator 100.

Besides beneficially eliminating the effects of varying propagation delays by synchronizing the operation of the comparator to the BITCLOCK signal, another effect of the second flip-flop 103' is to delay slightly the result of the decision by gate 102' whether the two input bits are the same or different. Thus, if the flip-flop 103' were simply inserted into the comparator 100, the input-selector switch 108 would not take on the correct state until slightly after the input bits were presented, and the wrong value could be temporarily presented at the comparator output.

To avoid temporarily selecting the wrong input value as a result of that delay, a modified input-selector switch 108' comprising five conventional NAND gates 108'-1 to 108'-5 is provided. The input-selector switch 108' has three states: (1) an initial state, in which the switch 108' behaves as an OR gate; (2) a select-A state; and (3) a select-B state. In the initial state, the input-selector switch's OR function has the effect that the comparator output promptly goes to "1" when different A and B inputs are presented. Thus, the bit value belonging to the larger input is presented at the output without waiting for the output of the XOR gate 102' to be clocked into flip-flop 103'. In the select-A state, the A value on the input A' is connected to the comparator output, and in the select-B state, the B value on the input B' is connected to the comparator output, both for the rest of the pair of input values as described above.

As seen in Figure 3, a suitable three-state input-selector switch 108' comprises five two-input NAND gates 108'-1 to 108'-5. With the latch 104' initialized (reset), the NAND gates 108'-1, 108'-2, are both fed with a "0" from the latch before unlike input bits are encountered, forcing their outputs to "1" irrespective of the outputs of the gate 106'. Thus, the outputs of the NAND gates 108'-3, 108'-4, are merely inversions of the A and B inputs, respectively. Also, the output of the gate

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108'-5 is the inversion of its (equal) inputs, i.e., A OR B, which is the same as both the A and B inputs so long as the A and B inputs are equal.

5 When the output of XOR gate 102' and the Q output of flip-flop 103' have gone HIGH, latch 104' clocks the A input into the flip-flop 106' and sets a "1" on the inputs of gates 108'-1, 108'-2, thereby passing to gates 108'-3, 108'-4, information about which of the A and B inputs is "1". Thus, an inversion of the Q output of
10 flip-flop 106' (i.e., $\bar{A}$) is presented to the inputs of the gate 108'-4, and an inversion of the $\bar{Q}$ output (i.e., A) is presented to the inputs of gate 108'-3.

If the A input is "1", that "1" and a "1" are presented on the inputs of gate 108'-3, and its output
15 goes LOW. The B-input "0" and a "0" are presented on the inputs of gate 108'-4, and its output goes HIGH. Thus, the output of gate 108'-5 goes HIGH. If the A input is "0", that "0" and a "0" are presented on the inputs of gate 108'-3, and its output goes HIGH. The B-input "1"
20 and a "1" are presented on the inputs of gate 108'-4, and its output goes LOW. Thus, the output of gate 108'-5 again goes HIGH. In either case, the output of gate 108'-5 continues to track the input that was "1" for the rest of the pair of input values.

25 As described above in connection with Figure 2A, the Q output of flip-flop 106' indicates which of the A and B inputs was selected, and is output as the traceback signal C'. In addition, Figure 3 shows the Q output as a control signal for a three-pole traceback-selector
30 switch 110' that passes A and B traceback signals from preceding comparators as described above.

As discussed above, the maximum value's identification by the traceback word can become available
35 after a time period significantly less than that needed to present the input values. A suitable means 112 for generating a signal that indicates that the maximum value has been identified is illustrated in Figure 4. Such a

generating means 112 can be provided with either of the comparators 100, 100', and traceback selectors 110, 110'.

Referring to Figure 4, the state of a selector switch 114 is controlled by the Q output of the comparator's D-type flip-flop (i.e., either the flip-flop 106 in the comparator 100, or the flip-flop 106' in the comparator 100'). The output of the switch 114 is presented to one input of an AND gate 116, and the other input of the AND gate 116 is connected to the SET output of the comparator's latch (i.e., the latches 104, 104' in the comparators 100, 100', respectively). Those inputs determine the state of the AND gate's output signal D. The signals E, F, that are presented to the inputs of the switch 114 are the outputs from the preceding stage's AND gates 116; it will thus be appreciated that the signals E, F, are different from the traceback signals handled by the selector switches 110, 110'.

The generating means 112 are provided in a manner substantially similar to the manner in which the traceback selector switches are provided. Just as the first stage of the tree does not need any selector switches 110, 110', the first stage of the tree does not need any generating means 112. The signals E, F, that are input to the respective switches 114 in the generating means associated with the tree's second stage are just the SET outputs of either the latches 104 or the latches 104' of the first stage comparators 100 or 100', respectively. When the output of the last stage generating means's AND gate 116 goes to "1", the traceback word presented from the last stage of the tree is valid (viz., the traceback bits identify the maximum value), and the search can be halted.

It is, of course, possible to embody the invention in specific forms other than those described above without departing from the invention. The embodiments described above are merely illustrative and should not be considered restrictive in any way. The

generating means 112 can be provided with either of the comparators 100, 100', and traceback selectors 110, 110'.

Referring to Figure 4, the state of a selector switch 114 is controlled by the Q output of the comparator's D-type flip-flop (i.e., either the flip-flop 106 in the comparator 100, or the flip-flop 106' in the comparator 100'). The output of the switch 114 is presented to one input of an AND gate 116, and the other input of the AND gate 116 is connected to the SET output of the comparator's latch (i.e., the latches 104, 104' in the comparators 100, 100', respectively). Those inputs determine the state of the AND gate's output signal D. The signals E, F, that are presented to the inputs of the switch 114 are the outputs from the preceding stage's AND gates 116; it will thus be appreciated that the signals E, F, are different from the traceback signals handled by the selector switches 110, 110'.

The generating means 112 are provided in a manner substantially similar to the manner in which the traceback selector switches are provided. Just as the first stage of the tree does not need any selector switches 110, 110', the first stage of the tree does not need any generating means 112. The signals E, F, that are input to the respective switches 114 in the generating means associated with the tree's second stage are just the SET outputs of either the latches 104 or the latches 104' of the first stage comparators 100 or 100', respectively. When the output of the last stage generating means's AND gate 116 goes to "1", the traceback word presented from the last stage of the tree is valid (viz., the traceback bits identify the maximum value), and the search can be halted.

It is, of course, possible to embody the invention in specific forms other than those described above without departing from the invention. The embodiments described above are merely illustrative and should not be considered restrictive in any way. The

scope of the invention is given by the appended claims, rather than the preceding description, and all variations and equivalents which fall within the range of the claims are intended to be embraced therein.

**CLAIMS**

1. An electronic comparator for selecting and outputting a larger of first and second electrical, binary-coded input values presented bit-serially, most-significant-bit first, comprising:

first and second input terminals for receiving, respectively, the first and second input values;

comparison means, operatively connected to the first and second input terminals, for comparing a serial input bit of the first input value with a bit of like significance from the second input value, and for generating as an output a signal alternatively indicating a like or unlike comparison result;

first latching means, operatively connected to the output of the comparison means, for registering a first occurrence of the unlike comparison result generated by the comparison means and for generating a trigger pulse in response to the first occurrence of the unlike comparison result;

second latching means, operatively connected to the first latching means and the first input terminal, for latching the serial input bit of the first input value in response to the trigger pulse and for providing the latched serial input bit at an output;

first selecting means, operatively connected to the first and second input terminals and the second latching means, and responsive to the output of the second latching means for selecting one of the input values as an output of the electronic comparator,

wherein the first selecting means selects the first input value when the latched serial input bit is a "1" state, and the first selecting means selects the second input value when the latched serial input bit is a "0" state.

2. An electronic comparator according to claim 1, wherein:



the comparison means is a logical exclusive-OR gate having an output;

the first latching means comprises a first resettable flip-flop having set and reset input
5 terminals and an output for providing the trigger pulse, wherein the set input terminal is operatively connected to the output of the logical exclusive-OR gate so that the output of the first flip-flop is set from a "0" state to a "1" state when the output of the
10 exclusive-OR gate indicates the first and second input values are unequal; and

the second latching means is a second flip-flop having a data input terminal operatively connected to the first input terminal and a clock input terminal
15 connected to the output of the first flip-flop.

3. An electronic comparator according to claim 2, wherein the second flip-flop generates a traceback signal to indicate which of the first and second input values was selected by the first selecting means.

20 4. An electronic comparator according to claim 3, further comprising second selecting means, responsive to the traceback signal, for alternatively selecting either a first traceback signal associated with the first input value or a second traceback signal
25 associated with the second input value based on the input value selected by the first selecting means.

5. An electronic comparator according to claim 4, further comprising means, operatively connected to the first and second flip-flops, for generating a
30 signal that indicates that the larger value has been identified.

6. An electronic comparator for selecting and outputting a larger of first and second electrical, binary-coded input values presented bit-serially, most-
35 significant-bit first, comprising:

first and second input terminals for receiving,



respectively, the first and second input values;

comparison means, operatively connected to the first and second input terminals, for comparing a serial input bit of the first input value with a bit of like significance from the second input value, and for
5 generating as an output a signal alternatively indicating a like or unlike comparison result;

first latching means, operatively connected to the output of the comparison means, for registering a first
10 occurrence of the unlike comparison result generated by the comparison means and for generating a trigger pulse in response to the first occurrence of the unlike comparison result;

second latching means, operatively connected to
15 the first latching means and the first input terminal, for latching the serial input bit of the first input value in response to the trigger pulse and for providing the latched serial input bit at an output;

first selecting means, operatively connected to
20 the first and second input terminals and the second latching means, and responsive to the output of the second latching means for selecting one of the input values as an output of the electronic comparator, wherein the first selecting means selects the logical
25 OR of the first and second input values as the output when the first latching means has not registered the first occurrence of the unlike comparison result, and the first selecting means selects the first input value as the output when the second latching means is set to
30 "1", and the first selecting means selects the second input value as the output when the second latching means is set to "0".

7. An electronic comparator according to claim 6, wherein:

35 the comparison means is a logical exclusive-OR gate operatively connected to the first and second



input terminals for forming, at an output of the logical exclusive-OR gate, a signal indicating a logical exclusive-OR of the first and second input values;

5 the first latching means comprises:

 a first-flip flop operatively connected to the output of the logical exclusive-OR gate for registering a value indicating whether corresponding bits of the first and second input values are equal or unequal,

10 wherein the first flip-flop registers the value in synchrony with a train of bitclock pulses applied to the first flip-flop; and

 a second resettable flip-flop operatively connected to an output of the first flip-flop, wherein
15 an output of the second flip-flop is set from a "0" state to a "1" state when the value registered by the first flip-flop indicates the two input values' bits are unequal; and

 the second latching means comprises a third flip-flop operatively connected to the second flip-flop and the first input terminal, wherein an output of the third flip-flop is alternatively set either to a "0" state or a "1" state in correspondence with the first input value's bit in response to the second flip-flop's
20 output changing state; and

 the first selecting means is operatively connected to the first and second input terminals and the second and third flip-flops, and the first selecting means selects the logical OR of the first and second input
30 values as the output when the second flip-flop is in the "0" state, and the first selecting means selects the first input value as the output when the third flip-flop is set to "1", and the first selecting means selects the second input value as the output when the
35 third flip-flop is set to "0".

8. An electronic comparator according to claim



7, wherein the third flip-flop generates a traceback signal to indicate which of the first and second input values was selected by the first selecting means.

9. An electronic comparator according to claim 5 8, further comprising second selecting means, responsive to the traceback signal, for alternatively selecting either a first traceback signal associated with the first input value or a second traceback signal associated with the second input value based on the 10 input value selected by the first selecting means.

10. An electronic comparator according to claim 8, further comprising means, operatively connected to the second and third flip-flops, for generating a signal that indicates that the larger value has been 15 identified.

11. An electronic logic circuit for selecting and outputting a maximum of a plurality of electrical binary-coded values comprising:

a plurality of electronic comparators for 20 selecting and outputting a larger of first and second electronic comparator input values, the first and second electronic comparator input values being binary-coded input values presented bit-serially, most-significant-bit first, the plurality of electronic 25 comparators being tree-connected to form a tree of electronic comparators and each electronic comparator including:

first and second input terminals for receiving, respectively, the first and second electronic 30 comparator input values;

comparison means, operatively connected to the first and second input terminals, for comparing a serial input bit of the first electronic comparator input value with a bit of like significance from the 35 second electronic comparator input value, and for generating as an output a signal alternatively



indicating a like or unlike comparison result;

first latching means, operatively connected to the output of the comparison means, for registering a first occurrence of the unlike comparison result generated by
5 the comparison means and for generating a trigger pulse in response to the first occurrence of the unlike comparison result;

second latching means, operatively connected to the first latching means and the first input terminal,
10 for latching the serial input bit of the first electronic comparator input value in response to the trigger pulse and for providing the latched serial input bit at an output, wherein the output from the second latching means is a traceback signal for
15 indicating which of the first and second electronic comparator input values was selected; and

first selecting means, operatively connected to the first and second input terminals and the second latching means, and responsive to the output of the
20 second latching means for selecting one of the electronic comparator input values as an output of the electronic comparator, wherein the first selecting means selects the first electronic comparator input value when the latched serial input bit is a "1" state,
25 and the first selecting means selects the second electronic comparator input value when the latched serial input bit is a "0" state,

wherein pairs of the plurality of values are presented bit-serially, most-significant-bit first, to
30 respective first ones of the electronic comparators disposed in a first stage of the tree, each first electronic comparator outputting a larger of the first and second electronic comparator input values as a first-stage output signal and outputting its traceback
35 signal as a first-stage traceback signal, the first-stage output signals being presented bit-serially,



most-significant-bit first, to respective second ones of the electronic comparators disposed in a second stage of the tree, and so forth for subsequent stages of the tree until the maximum of the input values is passed as an output signal from a last electronic comparator disposed in a last stage of the tree, and the first-stage traceback signals being presented to respective second ones of the electronic comparators disposed in a second stage of the tree, each second electronic comparator including means for selecting either the first traceback signal associated with the second electronic comparator's first electronic comparator input value or the first traceback signal associated with the second electronic comparator's second electronic comparator input value, and so forth for subsequent stages of the tree.

12. An electronic logic circuit according to claim 11, further comprising means, operatively connected to the electronic comparators, for generating a signal that indicates that the maximum value has been identified.

13. An electronic comparator, substantially as herein described with reference to, and as shown in, Figure 2A or Figure 3 of the accompanying drawings.

14. An electronic logic circuit, substantially as herein described with reference to, and as shown in, Figure 2B of the accompanying drawings.