

ABSTRACT

A semiconductor memory device is provided. The device includes a memory cell array including a plurality of dynamic memory cells; an error correction code (ECC) engine; an input/output (I/O) gating circuit connected between the ECC engine and the memory cell array; an error information register configured to store an error address and a first syndrome, the error address and the first syndrome being associated with a first error bit in a first codeword stored in a first page of the memory cell array; and a control logic configured to, based on the first codeword being read again and including a second error bit which is different from the first error bit, recover a second syndrome associated with the second error bit by using the first syndrome stored in the error information register and sequentially correct the first error bit and the second error bit.

FIG. 2