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"A STATIC MEMORY"

The present invention relates to a static memory, and more particularly to a static random access memory constructed of insulated-gate field effect transistors (hereinafter referred to as "MOS static RAM").

A MOS static RAM is usually provided with a sense amplifier along with a memory array composed of a plurality of static memory cells which are arranged in a matrix form, a plurality of word lines with which the selection terminals of the memory cells arranged in the same rows are connected in common, and a plurality of data lines with which the data terminals of the memory cells arranged in the same columns are connected in common. A data signal of comparatively low level delivered from a selected

memory cell is amplified by the sense amplifier.

In the case of a circuit arrangement in which a data line to be selected from amongst a plurality of data lines in the memory array is coupled to a common data line through a column switch circuit, the sense amplifier has its input terminal connected to the common data line. In this case, the output terminal of a writing circuit is also connected to the common data line. Accordingly, in the operation of reading out data, the data signal read out from the memory cell which has been selected by the word line and the column switch circuit is supplied to the sense amplifier through a common word line, whilst in the operation of writing down data, a data signal delivered from the writing circuit is supplied to the selected memory cell through the common word line:

In the operation of reading out the data, the read-out operation speed is limited by the period of time in which the potentials of the data line and the common data line are brought to predetermined potentials in accordance with the data signal delivered from the memory cell, and the operating characteristics of the sense amplifier.

The sense amplifier constructed of insulated-gate field effect transistors (hereinafter referred to as "MOSFETs"), especially the sense amplifier being in the differential circuit form, has its sensitivity affected by the varying range of an input signal to be applied to the input terminal thereof. When the varying range of the input signal becomes larger or smaller than a desired varying range, the sensitivity of the sense amplifier is decreased.

With a view of increasing the speed of the data read-out operation, the potential of the common data line before the initiation of the data read-out can be made a desired level in advance by arranging a MOSFET between, for example, a power source terminal and the common data line, the MOSFET causing a voltage drop of a magnitude equal to or greater than the threshold voltage thereof. Similarly, the potential of the data line can be set to a desired level in advance by arranging an appropriate MOSFET between the power source terminal and the data line. In this case, since the potentials of the common data line and the data line are preset to the prescribed values in a period such as a chip non-selection period, the period of time in which these potentials are brought to the predetermined potentials according to the data signal delivered from the memory cell becomes comparatively short. In addition, since the highest potentials of the common

data line and the data line are limited by the MOSFETs, the sensitivity of the sense amplifier is enhanced. It is consequently permitted to make the data read-out speed comparatively high.

However, the MOSFETs for applying the bias voltages as described above give rise to leakage currents or tailing currents which are not negligible.

In such a case where the chip non-selection period is made comparatively long, the potentials of the common data line and the data line are raised approximately to the potential of the power source terminal by the leakage currents or tailing currents. These leakage or tailing currents of the MOSFETs have their magnitudes increased with a rise in temperature. Therefore, when the temperature rises, the potentials of the common data line and the data line are responsively raised to undesirable levels in a comparatively short time. In response to the excessive potentials of the common data line and the data line, the sensitivity of the sense amplifier is reduced, so that the data read-out speed is limited.

In the case of an arrangement in which the sense amplifier in the differential circuit form is controlled by a chip selection signal, when the potential of the common data line is abnormally high as described above, the output voltage of this sense amplifier is reduced considerably irrespective of the level of the data read out from the memory cell, immediately after this amplifier has been brought into its operative state by the chip selection signal.

10 The output voltage of the sense amplifier is thereafter set to a level corresponding to the data level delivered from the memory cell. Accordingly, the data read-out speed is also limited by such output characteristic of the sense amplifier.

15 It is accordingly an object of the present invention to provide a MOS static RAM which can effect a stable high-speed operation.

According to a first aspect of the present invention there is provided a static memory comprising:

20 a static memory cell which has a selection terminal and a data terminal;

a signal line which is supplied with a data signal delivered from said static memory cell;

a sense amplifier which is supplied with
25 said data signal through said signal line;

a bias circuit which includes a MOSFET for
applying a bias voltage to said signal line, said
bias voltage having a value lowered with respect
to a power source voltage fed to a power source line;
5 and

resistance means for supplying a current
to said MOSFET to prevent an abnormal rise of a potential
of said signal line by a leakage current of said
MOSFET, said resistance means being connected between
10 said MOSFET and a reference potential point.

According to a second aspect of the present
invention there is provided a static memory including;

a plurality of static memory cells which are
arranged in the form of a matrix and each of which
15 has a selection terminal and a pair of data terminals;

a plurality of word lines each of which has
the selection terminals of the static memory cells
connected in common;

a plurality of paired data lines each of
20 which has the paired data terminals of the static
memory cells connected in common;

a pair of common data lines;

a switch circuit which couples the paired
data line to be selected amongst said plurality of
25 paired data lines, to said pair of common data lines;

25

a sense amplifier which has a pair of input terminals coupled to said pair of common data lines;

a bias circuit which includes a MOSFET for applying bias voltages to said pair of common data lines, said bias voltages having values reduced with respect to a power source voltage fed to a power source line; and

resistance means for supplying a current to said MOSFET to prevent an abnormal rise of a potential of said signal line by a leakage current of said MOSFET, said resistance means being connected between said MOSFET and a reference potential point.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a circuit diagram of one preferred form of static memory;

Figure 2A is a layout pattern diagram of memory cells,

Figure 2B is a layout pattern diagram of wiring layers corresponding to the layout pattern in Figure 2A, and

Figure 2C is a sectional view of a semiconductor substrate taken along the lines A-A' in Figure 2A;

Figure 3 is an operational waveform diagram of the sense amplifier shown in Figure 1;

Figure 4A is a layout pattern diagram of circuit

elements constituting the bias circuit shown in Figure 1; while Figure 4B is a sectional view of a semiconductor substrate taken along the lines A-A' in Figure 4A; and

Figures 5 and 6 are circuit diagrams of essential portions each constituting a modification of the embodiment shown in Figure 1.

Figure 1 shows the circuit of a MOS static RAM. The RAM is wholly formed on a single semiconductor substrate by the known CMOS integrated circuit technology. The RAM has external terminals AX_1 to AX_K , AY_1 to AY_L , D_{OUT} , $\overline{CS}$, $\overline{WE}$, D_{in} , V_{DD} and GND, and is operated in such a way that a power source voltage is supplied from an external power source 9 across the power source terminal V_{DD} and the earth terminal GND.

The MOS static RAM includes a memory array 1, which is constructed of memory cells $1a$ to $1d$, word lines W_1 to W_m , and data lines D_1 , $\overline{D_1}$ to D_n , $\overline{D_n}$.

The respective memory cells have arrangements identical to one another. Each of the memory cells is constructed, as illustrated in detail by the memory cell $1a$. The memory cell comprises a static flip-flop circuit which consists of driving MOSFETs Q_1 and Q_2

having their gates and drains cross-coupled to each other, load resistors R_1 and R_2 , and transfer gate MOSFETs Q_3 and Q_4 which are respectively arranged between the input and output terminals of the static flip-flop circuit and the pair of data lines D_1 and $\overline{D_1}$.

The memory cell has the node of the load resistors R_1 and R_2 supplied with the power source voltage through the power source terminal V_{DD} , and is thereby operated. In the memory cell, one of driving MOSFETs Q_1 and Q_2 is brought into the "on" state and the other into the "off" state in accordance with the data to be held.

The current consumption of the memory cell consists of an operating current which flow through that MOSFET which is turned "on" in the pair of driving MOSFETs Q_1 and Q_2 , and a leakage current which flows through that MOSFET which is turned "off". The current consumption is reduced by increasing the resistances of the load resistors R_1 and R_2 . The leakage current flowing through the driving MOSFET in the "off" state causes a voltage drop across the load resistor, and consequently reduces the voltage applied to the gate of the driving MOSFET in the "on" state. Therefore, the resistances of the load resistors R_1 and R_2 have their upper

limits set by the leakage currents of the driving MOSFETs. The lower limits of the resistances of the load resistors R_1 and R_2 are set by the required power consumption characteristic of the memory cell. The load resistors R_1 and R_2 are set at a high resistance value of, for example several megohms to several gigaohms in order to reduce the power consumption of the memory cell in the data retaining status thereof. With a view to reducing the occupying area of the memory cell, the resistors R_1 and R_2 are constructed of, for example polycrystalline silicon layers of comparatively high resistivity which are formed through field insulating films of comparatively great thickness on the surface of the semiconductor substrate forming the MOSFETs.

In each memory cell, the gates of the transfer gate MOSFETs Q_3 and Q_4 are regarded as the selection terminal of the corresponding memory cell, and the drains of the data terminals for receiving and delivering data.

The memory cells $1a$ to $1d$ are arranged in the form of a matrix as shown. The memory cells $1a$ and $1c$ and the memory cells $1b$ and $1d$ are arranged in the same rows and have their selection terminals connected to the word lines W_1 and W_m in common,

respectively. The memory cells $1a$ and $1b$ and the memory cells $1c$ and $1d$ are arranged in the same columns and have their pair of data terminals connected to the pair of data lines D_1 and $\overline{D_1}$ and data lines D_n and $\overline{D_n}$ in common, respectively. The data lines D_1 to $\overline{D_n}$ which are arranged in correspondence with the respective memory cell columns are connected to common data lines CD and $\overline{CD}$ through transfer gate MOSFETs Q_9 , Q_{10} and Q_{11} , Q_{12} which constitute a column switch circuit 10.

The word lines $W_1 - W_m$ in the memory array 1 are connected to the corresponding output terminals of an X address decoder 2, and are accordingly selected by the X address decoder 2 respectively.

The paired transfer gate MOSFETs Q_9 and Q_{10} , and Q_{11} and Q_{12} constituting the column switch circuit 10 have their gates connected to the corresponding output terminals of a Y address decoder 3 in common, respectively, and are selected by the Y address decoder 3.

The X address decoder 2 is supplied with address signals fed to the address input terminals AX_1 ,

to AX_k , through address buffer circuit BX_1 to BX_k . The X address decoder 2 has its operation controlled by a control signal CS. When the control signal CS is at its low level, the word lines $W_1 - W_m$ are brought to their non-selection level (low level) irrespective of the address signals.

The Y address decoder 3 is similarly supplied with address signals fed to the address input terminals AY_1 to AY_ℓ , through address buffer circuits BY_1 to BY_ℓ .

The pair of common data lines CD and $\overline{CD}$ are connected to the pair of input terminals of a sense amplifier 4 on one side, and are connected to the output terminals of a writing circuit 6 through transfer gate MOSFETs Q_{18} and Q_{19} on the other side. The output terminal of the sense amplifier 4 is connected to the input terminal of an output buffer circuit 5.

The sense amplifier 4 comprises a differential amplifier circuit which consists of differential MOSFETs Q_{13} and Q_{14} , MOSFETs Q_{15} and Q_{16} effecting a current mirror operation, and a MOSFET Q_{17} for providing a constant current. The MOSFET Q_{17} is also operated as a power switch. When a chip selection signal which is supplied to the chip

selection terminal $\overline{CS}$ is brought to its low level such as earth potential of the circuit, the control signal which is supplied from a control circuit 8 to the gate of the MOSFET Q_{17} responds thereto to become its high level. As a result, the MOSFET Q_{17} is brought into the "on" state, and the sense amplifier 4 is energized.

The output buffer circuit 5 comprises a 3-status circuit which includes the floating state of its output terminal. When the control signal CS provided from the control circuit 8 is at the low level, the output terminal of the output buffer circuit 5 is brought into the floating state. When the control signal CS is at the high level, the output terminal of the output buffer circuit 5 is brought to its low level or high level corresponding to the output level of the sense amplifier 4.

The common data lines CD and $\overline{CD}$ have also a bias circuit 7 connected thereto. The bias circuit 7 comprises an n-channel MOSFET Q_{20} for level shift the gate and drain of which are connected to the power source terminal V_{DD} , p-channel MOSFETs Q_{21} and Q_{22} constituting an equalizer which are respectively connected between the source of the MOSFET Q_{20} and the common data lines CD and $\overline{CD}$,

and resistors R_3 and R_4 which are respectively connected between the common data lines CD and $\overline{CD}$ and earth.

The MOSFETs Q_{21} and Q_{22} are switch-controlled by the control signal CS so as to be in the "on" states during the chip non-selection period. When the signal supplied to the external terminal $\overline{CS}$ is at the high level, the control signal CS is brought to the low level such as earth potential. The MOSFETs Q_{21} and Q_{22} are brought into the "on" states by the low level of the control signal CS .

In the case where the bias circuit 7 is omitted from the circuit, the potential difference between the common data lines CD and $\overline{CD}$ as has been set by the memory cell selected during a preceding data read-out operation is still held by stray capacitances (not shown) which exist between these common data lines CD and $\overline{CD}$ and earth. In this case, if a data signal which is provided from the memory cell to be selected anew has the inverted level to the level of a data signal which has been provided from the memory cell selected previously, a comparatively long time will be taken before the potential difference between the common data lines CD and $\overline{CD}$ reaches a new potential difference. That is, the access time

of the RAM will become long.

In the case where the bias circuit 7 is provided as shown in Figure 1, the potential difference corresponding to the previous data as stated above is made approximately zero by reason that the MOSFETs Q_{21} and Q_{22} are held in the "on" states during the chip non-selection period. When, in this manner, the potential difference between the pair of common data lines CD and $\overline{CD}$ is made approximately zero in advance, the potential difference corresponding to the data of the memory cell to be selected anew can be afforded to the common data line pair CD and $\overline{CD}$ in a comparatively short time, with the result that the access time of the RAM can be made short.

Since the MOSFET Q_{20} in the bias circuit 7 is connected in diode configuration, it causes a voltage drop approximately equal to its threshold voltage across its source and drain.

During the chip non-selection period, therefore, the common data lines CD and $\overline{CD}$ are supplied with a voltage whose level is shifted by the MOSFET Q_{20} with respect to the power source voltage of the power source terminal V_{DD} .

The sense amplifier 4 including the differential MOSFETs as stated above has its sensitivity usually influenced by the levels of bias potentials applied to its pair of input terminals.

In the case where the bias voltages of the pair of input terminals of the sense amplifier 4 are raised above a desired value, a voltage which is applied to the drain of the constant current MOSFET Q_{17} is correspondingly raised. In the case where the sense amplifier 4 is operated by a comparatively low power-source voltage e.g. +5 volts, the constant current MOSFET Q_{17} does not exhibit an ideal constant-current characteristic because its drain voltage is limited to a comparatively low value. The drain current of the constant current MOSFET Q_{17} is therefore increased by raising the drain voltage thereof. The increase of the drain current of the constant current MOSFET Q_{17} increases the drain currents of the respective differential MOSFETs Q_{13} and Q_{14} . In this case, when the potential of the common data line $\overline{CD}$ is made lower than that of the common data line CD in accordance with the data signal provided from the memory cell, the drain current of the MOSFET Q_{13} is increased and that of the MOSFET Q_{14} is decreased. As a result, a low level signal of comparatively good

level is provided at the drains of the MOSFETs Q_{13} and Q_{15} connected in common.

In contrast, when the potential of the common data line CD is made lower than that of the common data line $\overline{CD}$, the drain current of the MOSFET Q_{13} is decreased and that of the MOSFET Q_{14} is increased. As a result, a high level signal is provided from the MOSFETs Q_{13} and Q_{15} . In this case, however, the drain voltage of the MOSFET Q_{14} is lowered by a voltage developing across the source and drain of the diode-connected MOSFET Q_{16} , with the result that the increase of the drain current of the MOSFET Q_{14} is made comparatively small. Owing to the comparatively small increase of the drain current of the MOSFET Q_{14} , the increment of a voltage to be applied across the gate and source of the MOSFET Q_{15} is limited to be comparatively small. As a result, the increment of the drain current of the MOSFET Q_{15} becomes comparatively small. Notwithstanding that the drain current of the MOSFET Q_{13} is increased by the increase of the drain current of the constant current MOSFET Q_{17} , the increase of the drain current of the MOSFET Q_{15} is made comparatively small, and hence, the high level signal to be provided from the MOSFETs Q_{13} and Q_{15} is made a comparatively low level.

The level lowering of the high level signal at the time when the bias voltages of the pair of input terminals have been raised, becomes considerable in the case where the gain of the sense amplifier 4 is increased by making comparatively low the drain - source conductances of the MOSFETs Q_{15} and Q_{16} as the drain loads of the respective MOSFETs Q_{13} and Q_{14} , in other words, where the MOSFETs Q_{15} and Q_{16} are made comparatively small in size.

When the level of the high level signal of the sense amplifier 4 is lowered, the output buffer circuit 5 fails to execute the desired operation.

In the case where the bias voltages of the pair of input terminals are lowered below the desired value, the drain current of the constant current MOSFET Q_{17} is decreased. In response to the decrease of the drain current of the constant current MOSFET Q_{17} , a charging current to be supplied to the input capacitance (not shown) of the output buffer circuit 5 through the MOSFET Q_{15} or a discharging current to be supplied to the input capacitance through the MOSFET Q_{13} decreases. As a result, the operating speed of the sense amplifier is limited.

The sensitivity of a sense amplifier in a latch circuit arrangement, that is, the sensitivity of a sense

amplifier including a pair of input MOSFETs having their gates and drains cross-coupled with each other increases by raising the input bias voltages because the input MOSFETs have large conductances.

In the case of the circuit arrangement shown in Figure 1, the potentials of the common data lines CD and $\overline{CD}$ are lowered to the appropriate levels by the MOSFET Q_{20} , so that the sense amplifier 4 operates at a high sensitivity. As a result, the output of the sense amplifier 4 is brought to an appropriate level corresponding to the data supplied to the common data lines CD and $\overline{CD}$ within a comparatively short time.

In the case where, for example, the MOSFET Q_{20} has been removed from the bias circuit 7, the common data lines CD and $\overline{CD}$ have their respective potentials raised substantially to the potential of the power source terminal V_{DD} when the MOSFETs Q_{21} and Q_{22} are rendered conductive. Even in the case where the MOSFET Q_{20} is provided, the common data lines CD and $\overline{CD}$ have their respective potentials raised undesirably when the resistors R_3 and R_4 are omitted.

Examples of the potential variations of the common data lines CD and $\overline{CD}$ at the time when the potentials of these common data lines CD and $\overline{CD}$ have

been raised to the power source voltage in advance, are indicated in Figure 3 as solid-line curves CD and $\overline{CD}$. In this case, the potential difference to be afforded to the common data lines CD and $\overline{CD}$ by the selected memory cell exhibits only a comparatively small value because the MOSFETs in the memory cell are made comparatively small in size. Although this is not essential, current is caused to flow from one common data line $\overline{CD}$ to be made the high level to the other common data line CD to be made the low level through the MOSFETs Q_{21} and Q_{22} on account of the delays of the "off" timings of the equalizer MOSFETs Q_{21} and Q_{22} . As a result, the potential of the common data line $\overline{CD}$ to be made the high level is also lowered as shown in Figure 3.

In the case where the control signal CS to be supplied to the constant current MOSFET Q_{17} is made the high level at a comparatively early time in order to permit the data of the memory cell to be read out at a comparatively high speed, the sense amplifier 4 is activated by this control signal CS before a sufficient level difference is given between the common data lines CD and $\overline{CD}$ by the selected memory cell. Herein, since the level difference of the common data lines CD and $\overline{CD}$ is small, the differential MOSFETs Q_{13} and Q_{14} are simultaneously brought into the conductive states, with the result that the output of the sense amplifier 4 is temporarily

lowered.

In the case where the common data lines CD and $\overline{CD}$ have been raised undesirably as described above, the drain current of the constant current MOSFET Q_{17} is comparatively increased as referred to above. The output voltage V_{OUT} of the sense amplifier 4 is therefore lowered greatly as indicated by a solid-line curve V_{OUT} in Figure 3 when the constant current MOSFET Q_{17} has been turned "on" by the control signal CS (solid-line curve CS in Figure 3), even if the output voltage V_{OUT} ought to be made the high level. This output voltage V_{OUT} is changed to the high level again as seen from the solid-line curve V_{OUT} because a comparatively large level difference exists between the common data lines CD and $\overline{CD}$. When the output voltage V_{OUT} of the sense amplifier 4 becomes lower than the logic threshold voltage V_T of the output buffer circuit 5, the output of the output buffer circuit 5 is temporarily inverted even in the case where the data of the high level is read out from the memory cell. It is therefore inevitable that the read-out time of the data is late.

In contrast, when the bias circuit 7 is provided with the level shifting MOSFET Q_{20} as shown in Figure 1, the levels of the common data lines CD and $\overline{CD}$ are thereby lowered as shown by broken lines in Figure 3.

Therefore, the magnitude of recession of the output voltage of the sense amplifier 4 in the activation of this amplifier is reduced as indicated by the broken-line curve V_{OUT} in Figure 3. It is thus possible to read out the data from the memory cell at high speed.

The resistors R_3 and R_4 are provided in order to stably enhance the speed of the read-out operation, in other words, to prevent the level rises of the common data lines attributed to the leakage (or tailing) current of the level shifting MOSFET Q_{20} . The resistors R_3 and R_4 are provided between the respective common data lines CD and $\overline{CD}$ and the reference potential (0 V).

In order to prevent the power consumption of the RAM from increasing during the chip non-selection, the resistors R_3 and R_4 have their combined parallel resistance value set to a comparatively high resistance so as to conduct current substantially equal to or somewhat greater than the leakage current of the level shifting MOSFET Q_{20} .

In a modified form the resistors R_3 and R_4 can be replaced by diode-connected MOSFETs. However, it is desirable, that like the resistors R_1 and R_2 in the memory cell the resistors R_3 and R_4 are composed of polycrystalline silicon layers (not shown)

which are formed on the semiconductor substrate through field insulating films of comparatively great thickness. In the case where the resistors R_3 and R_4 are composed of polycrystalline silicon layers in this manner, their occupying areas can be made comparatively small because the polycrystalline silicon layers can be endowed with a comparatively high resistivity. In addition, the resistor composed of a polycrystalline silicon layer does not have a stray capacitance of comparatively great value as in the drain or source junction of a MOSFET because it is formed on the semiconductor substrate through the field insulating film which is made of, for example, a silicon dioxide film. Therefore, the resistors composed of polycrystalline silicon layers afford only comparatively small stray capacitances to the common data lines CD and $\overline{CD}$ and do not substantially limit the signal variation speeds on these common data lines CD and $\overline{CD}$.

Even when the leakage current of the MOSFET Q_{20} for setting the bias potentials of the common data lines CD and $\overline{CD}$ exists at, for example, a long chip non-selection period of a high temperature, it is absorbed by the high resistance of the resistors R_3 and R_4 , so that the bias voltages can be prevented from rising.

In the activation of the sense amplifier 4 based on the turn-on of the power switch MOSFET Q_{17} , accordingly, the bias voltages of the common data lines CD and $\overline{CD}$ are fixed to be constant, and hence, the recession of the output signal V_{OUT} becomes small and constant as shown by the broken line in Figure 3. Thus, the stable enhancement of the speed of the read-out operation can be realized.

Enhancement-mode MOSFETs Q_5 , Q_6 , Q_7 and Q_8 for data line loads are respectively located between the data lines D_1 , $\overline{D_1}$, D_n and $\overline{D_n}$ and the power source terminal V_{DD} . In addition, the resistors R_5 , R_6 , R_7 and R_8 constructed of polycrystalline silicon layers and having a purpose similar to that of the resistors R_3 and R_4 are located between the respective data lines and earth.

Accordingly, the respective data lines are supplied with voltages whose levels have been shifted by the MOSFETs for the data line loads. Since the leakage currents of the load MOSFETs Q_5 , Q_6 etc., can be absorbed by the similar high resistances of the resistors R_5 , R_6 etc., the level rises of the data lines D_1 , $\overline{D_1}$ etc., can be prevented.

In the above description, amongst the MOSFETs $Q_1 - Q_{22}$, those MOSFETs whose channel region parts are

assigned arrows toward the gates as in, for example, the MOSFET Q_1 are n-channel MOSFETs, and those MOSFETs whose channel region parts of which are assigned arrows in the opposite sense as in, for example, the MOSFET Q_{15} are p-channel MOSFETs. Accordingly, the circuit is constructed of a C-MOS (complementary MOS) circuit. The illustrated n-channel MOSFETs have their body gates coupled to earth potential of the circuit, whilst the p-channel MOSFETs have their body gates coupled to the power source terminal V_{DD} .

The memory cells have a structure as illustrated in Figures 2A to 2C. Figure 2A shows the layout pattern of the memory cells before evaporated aluminium layers are formed, and Figure 2B shows the layout pattern of the evaporated aluminium layers. Figure 2C shows a sectional view of the part of a semiconductor substrate seen in the direction of arrows A-A' in Figure 2A.

The semiconductor substrate 11 shown in Figure 2C is a single-crystal silicon substrate, for example, having a resistivity of 10 ohm-cm and with its surface being parallel to the crystal plane (100). That part of the surface of the semiconductor substrate 11 which is to form the memory array is made a p-type well region 12 of a depth of, e.g. 4 μm which is formed

by the implantation of boron ions and the subsequent drive-in diffusion. Those parts of the surface of the semiconductor substrate 11 which are other than surface parts corresponding to active regions such as MOSFET forming regions and semiconductor wiring regions are formed with field oxide films 13 having a comparatively great thickness of, e.g. about $0.95\text{ }\mu\text{m}$ by the known selective oxidation. The surface of the p-type well region 12 is formed with n-type semiconductor regions 14b, 14d etc, which serves as the drain region and source region of the MOSFET. On the channel region of the MOSFET, a gate oxide film 13' having a comparatively small thickness of, e.g. about 50 nm is formed. The field oxide film 13 and the gate oxide film 13' are overlaid with polycrystalline silicon layers 15b, 15c₃ etc., which have a thickness of, e.g. about $0.35\text{ }\mu\text{m}$ and which serves as a wiring and a gate electrode. The polycrystalline silicon layer 15c₃ is directly coupled with the n-type semiconductor region 14d. In addition, the polycrystalline silicon layer 15c₃ has a portion R₁ which does not substantially contain a conductivity type-determining impurity, and a portion which contains an n-type impurity. The portion R₁ is utilized as a high

resistance element. The surface of the semiconductor substrate 11 is covered with an insulating film 16 which is, e.g. about 0.6 μm thick and made of phosphosilicate glass.

The structure shown in Figure 2C can be obtained by the following method of manufacture:

First, the semiconductor substrate 11 which is formed with the p-type well region 12 and then with the field oxide film 13 is prepared.

The surface parts to form the active regions, that is, the semiconductor substrate surface parts which are not covered with the field oxide film 13 are formed with the thin oxide film to serve as the gate oxide films of the p-channel MOSFETs and n-channel MOSFETs.

Those parts of the thin oxide film formed which correspond to direct contact portions as shown by DC_2 in Figure 2C are removed by the selective etching.

The surface of the resultant semiconductor substrate 11 is formed with a polycrystalline silicon layer by the known chemical vapour deposition (CVD) technique.

On the polycrystalline silicon layer formed, a first silicon oxide film being, e.g. about $0.3\ \mu\text{m}$ thick is formed by the CVD technique. This silicon oxide film is used as a mask in the case where an n-type impurity is diffused into the polycrystalline silicon layer.

The first silicon oxide film is selectively etched and removed so as to be left on those parts of the polycrystalline silicon layer in which the high resistance elements R_1 etc. are to be formed.

Subsequently, phosphorus as the n-type impurity is diffused into the polycrystalline layer. In this case, the first silicon oxide film functions as the impurity diffusion mask, and hence, the phosphorus is not diffused into those parts of the polycrystalline silicon layer which correspond to the high resistance elements R_1 etc.

Subsequently, the polycrystalline silicon layer other than its parts which are to form the wiring layers, the high resistance elements and the gate electrodes of the p-channel and n-channel MOSFETs is etched and removed by the selective etching.

On the surface of the semiconductor substrate 11, a second silicon oxide film for an impurity diffusion mask is formed by the CVD technique again.

Those parts of the second silicon oxide film which overlies the substrate parts to form the p-channel MOSFETs and p-type polycrystalline silicon wiring layers are selectively etched and removed. In this etching step, the polycrystalline silicon layer and the field oxide films function substantially as an etching mask. As a result, the gate oxide films overlying those parts of the semiconductor substrate surface in which the drain regions and source regions of the p-channel MOSFETs are to be formed are etched and removed.

Subsequently, boron is diffused into the exposed polycrystalline layer and semiconductor substrate surface as a p-type impurity. Thus, p-type semiconductor regions as the drain regions and source regions of the p-channel MOSFETs are formed in the surface of the semiconductor substrate. Since the polycrystalline silicon layer and the field oxide films function as the impurity diffusion mask, the p-type semiconductor regions are self-aligned with respect to the polycrystalline silicon layer and the field oxide films. The polycrystalline silicon layer having been made the n-type by the previous diffusion of the n-type impurity is turned into the p-type by the diffusion of the boron.

After removing the second silicon oxide film, a third silicon oxide film for an impurity diffusion mask is formed on the surface of the semiconductor substrate by the CVD technique.

Those parts of the third silicon oxide film which overlie the substrate parts to form the n-channel MISFETs and n-type polycrystalline silicon wiring layers are selectively etched and removed. In this etching step, the gate oxide films overlying those parts of the p-type well region surface in which the drain regions and source regions of the n-channel MOSFETs are to be formed are also etched and removed.

Subsequently, phosphorus as an n-type impurity is diffused into the exposed polycrystalline silicon layer and p-type well region surface. Thus, n-type semiconductor regions as the drain regions and source regions of the n-channel MOSFETs are formed in the surface of the p-type well region. The impurity is not introduced into those parts of the polycrystalline silicon layer which correspond to the high resistance elements R_1 etc., because the second and third silicon oxide films function as the impurity diffusion mask.

After etching and removing the third silicon oxide film, an oxide film having a thickness of, e.g. $400\text{\AA}$ (light oxide film, not shown) is formed on the exposed polycrystalline layer by the thermal oxidation.

Subsequently, the insulating film 16 made of phosphosilicate glass is formed on the surface of the resultant semiconductor substrate. Since the light oxide film is formed, phosphorus in the insulating film 16 is not diffused into the polycrystalline layer.

Subsequently, the contact holes as shown in Figure 2C are provided in the insulating film 16 and the underlying light oxide film (not shown) by the selective etching.

An evaporated aluminium layer having a thickness of, e.g. $0.8\ \mu\text{m}$ is formed on the surface of the semiconductor substrate, and it is thereafter selectively etched and removed.

In Figure 2A, the n-type semiconductor regions are indicated by broken-line patterns 14a - 14d, and the finished polycrystalline silicon layers of solid-line patterns. Parts with rightward rising hatching as in areas CH_1 and CH_2 indicate the channel regions of the MOSFETs, while parts with crosshatching as in areas DC_1 and DC_2 indicate the direct contact portions where the polycrystalline silicon layers and the n-type semiconductor regions are directly coupled. Parts with leftward rising hatching as in areas R_1 and R_2 indicate those portions of the polycrystalline silicon layers in which substantially no impurity is introduced, that is,

the portions which serve as the high resistance elements.

The polycrystalline silicon layer 15b constitutes the word line W_2 , and also constitutes the gate electrodes of the transfer gate MOSFETs in the memory cell. The transfer gate MOSFET Q_3 as shown in Figure 1 is formed from the n-type semiconductor region 14a, the channel region CH_3 , the polycrystalline silicon layer 15b which extends on the channel region CH_3 , and the n-channel semiconductor region 14c. Likewise, the transfer gate MOSFET Q_4 is formed from the n-type semiconductor regions 14b and 14d, the channel region CH_4 , and the polycrystalline silicon layer 15b.

The driving MOSFET Q_1 is formed from the n-type semiconductor regions 14c and 14e, the channel region CH_1 and the polycrystalline silicon layer 15c₃, whilst the driving MOSFET Q_2 is formed from the n-type semiconductor regions 14d and 14e, the channel region CH_2 and the polycrystalline silicon layer 15c₂.

QWA The polycrystalline silicon layer 15c₂ is directly coupled with the n-type semiconductor region 14c serving as the source region and drain region of the MOSFETs Q_3 and Q_1 in the contact portion DC_1 , whilst the polycrystalline silicon layer 15c₃ is directly coupled with the n-type semiconductor region serving as the source region and drain region of the MOSFETs Q_4 .

and Q_2 in the contact portion DC_2 . One memory cell is thus formed as described above.

The polycrystalline silicon layers $15c_1$ constitutes the power source wiring layer V_{DD} , and is continuous to the polycrystalline silicon layers $15c_2$ and $15c_3$ of the memory cell.

The n-type semiconductor regions $14a$, $14b$, $14e$ etc., are provided with contact portions C_1 , C_2 , C_3 etc.,

On the insulating film 16 shown in Figure 2C, evaporated aluminium layers 17a to 17f in a pattern as shown in Figure 2B are extended. The evaporated aluminium layer 17a is coupled with the n-type semiconductor region $14a$ in the contact portion C_1 , and constitutes the data line D_1 in one memory cell column. Likewise the evaporated aluminium layer 17c is coupled with the n-type semiconductor region $14b$ in the contact portion C_2 and constitutes the data line $\overline{D_1}$ in one memory cell column. The evaporated aluminium layer 17b is coupled with the n-type semiconductor region $14e$ serving as the common source region of the MOSFETs Q_1 and Q_2 in the contact portion C_3 , and constitutes the earth connection GND.

The evaporated aluminium layer 17e constitutes the data line D_2 in the next memory cell column.

The pattern of memory cells in one memory cell

row and the pattern of memory cells in another memory cell row adjacent thereto are substantially symmetrical as shown in Figure 2A.

Figure 4A shows the layout pattern of the respective elements constituting the bias circuit 7 shown in Figure 1, whilst Figure 4B shows the section of a semiconductor substrate portion seen in the direction of arrows A-A' in Figure 4A. In Figure 4A, semiconductor regions such as a p-type well region 12a regions of a p-channel MOSFET and n-channel MOSFET and the drain and source have their patterns indicated by broken lines, and polycrystalline silicon layers have their patterns indicated by solid lines. In addition, evaporated aluminium layers have their patterns indicated by two-dot chain lines. These regions are formed simultaneously with the respective regions which constitute the memory array.

The n-channel MOSFET Q_{20} is formed from n-type drain regions 14f and 14h and an n-type source region 14g which are formed in the surface of the p-type well region 12a, and an n-type polycrystalline silicon layer 15d which serves as a gate electrode. The p-channel MOSFET Q_{21} is formed from a p-type drain region 14i and a p-type source region 14j which are formed in the surface of the semiconductor substrate 11, and a p-type polycrystalline silicon layer 15e which

serves as a gate electrode, whilst the p-channel MOSFET Q_{22} is formed from a p-type drain region 14k, the p-type source region 14j and the polycrystalline silicon layer 15e.

The drain regions 14f and 14h of the MOSFET Q_{20} are coupled to an evaporated aluminium layer 17g serving as the power source wiring V_{DD} through contact portions C_{61} to C_{64} and C_{81} to C_{84} . Similarly, the polycrystalline silicon layer 15d is coupled to the evaporated aluminium layer 17g through a contact portion C_{10} .

The drain region 14g of the MOSFET Q_{20} is coupled to an evaporated aluminium layer 17h through contact portions C_{71} to C_{73} . The evaporated aluminium layer 17h is coupled to the common source region 14j of the MOSFETs Q_{21} and Q_{22} through contact portions C_{91} etc. The polycrystalline silicon layer 15e is coupled through a contact portion C_{11} to an evaporated aluminium layer 17i which is supplied with the control signal CS.

The drain regions 14i and 14k of the MOSFETs Q_{21} and Q_{22} are respectively coupled to evaporated aluminium layers 17j and 17k serving as the common data lines through contact portions C_{101} etc, and C_{111} etc.

Polycrystalline silicon layers 15f and 15g are arranged on the field oxide film 13. The polycrystalline silicon layer 15f has one of its ends coupled to the evaporated aluminium layer 17j through a contact portion C_{121} , whilst the polycrystalline silicon layer 15g has one of its ends similarly coupled to the evaporated aluminium layer 17k through a contact portion C_{122} . The polycrystalline silicon layers 15f and 15g have their respective other ends coupled to an evaporated aluminium layer 17_l serving as the earth connection GND through contact portions C_{131} and C_{132} .

Likewise to the polycrystalline silicon layers shown in Figures 2A to 2C, the polycrystalline silicon layers 15f and 15g have portions R_3 and R_4 in which substantially no impurity is introduced, respectively. The remaining portions of the polycrystalline silicon layers 15f and 15g are of the n-type.

Regarding the biasing n-channel MOSFET Q_{20} , the leakage current between the drain and source thereof is proportional to the area of the drain regions thereof. In the case where the length and width of the drain regions 14f and 14h and source region 14g are 50 μm and 9 μm , respectively, the leakage current reaches a magnitude of about 10^{-11} ampere at 100°C. Herein, this leakage current is absorbed comparatively well by affording a comparatively great resistance of the order of 10^{11} ohm to each of the polycrystalline silicon

layers 15f and 15g. In this case, the length and width of the portion R_3 and R_4 in the polycrystalline silicon layers 15f and 15g are respectively made, for example 5 μm and 3 μm .

Figure 5 shows an alternative embodiment of the bias circuit 7. Instead of the polycrystalline-silicon high resistances R_3 and R_4 in the embodiment of Figure 1 for absorbing the leakage current of the MOSFET Q_{20} in the bias circuit 7, MOSFETs Q_{23} and Q_{24} whose gates and sources are connected are arranged between the common data lines CD and $\overline{\text{CD}}$ and the reference potential.

The MOSFETs Q_{23} and Q_{24} cause drain leakage currents which absorb the leakage current of the MOSFET Q_{20} . As a result, in spite of the leakage current of the MOSFET Q_{20} , the potentials of the common data lines CD and $\overline{\text{CD}}$ are made the desired values as in the previous embodiment. The MOSFETs Q_{23} and Q_{24} should preferably have a structure in which the combined drain leakage current thereof becomes greater than the leakage current of the MOSFET Q_{20} . In other words, it is preferable that the size of the drain regions of the MOSFETs Q_{23} and Q_{24} is equal to or greater than the size of the drain region of the MOSFET Q_{20} .

The MOSFETs Q_{23} and Q_{24} can have a channel type opposite to that of the MOSFET Q_{20} . However, it is preferable that the MOSFETs Q_{23} and Q_{24} are the same as the MOSFET Q_{20} in the channel type and that they are manufactured simultaneously with the MOSFET Q_{20} . Under these conditions, the leakage current levels of the MOSFETs Q_{23} and Q_{24} correspond favourably to the leakage current level of the MOSFET Q_{20} irrespective of their deviations and temperature-dependencies.

As a result, the undersirable potential rises of the common data lines can be favourably prevented.

Although no illustration is made, the resistors R_5 , R_6 , R_7 , R_8 etc., in Figure 1 can also be replaced with MOSFETs similar to the MOSFETs Q_{23} and Q_{24} in Figure 5.

Figure 6 shows an alternative embodiment of the writing circuit 6. The MOSFETs Q_{18} and Q_{19} for transmitting write-down signals are held in the "off" states by the control signal $\overline{WE}$ during the chip non-selection, and their leakage currents are utilized to prevent the excessive rises of the potentials of the common data lines CD and $\overline{CD}$.

The writing circuit 6 is constituted by a NAND (or NOR) gate circuit of 2 inputs so that both the pair of output terminals can be held at the low level during the chip non-selection.

The writing circuit 6 includes a first 2-input gate circuit MOSFETs Q_{25} to Q_{28} , a second 2-input gate circuit comprising MOSFETs Q_{29} to Q_{32} , and an inverter circuit IV.

The chip selection signal $\overline{CS}$ is applied in common to the gates of the MOSFETs Q_{26} , Q_{28} and Q_{30} , Q_{32} which are the inputs of the first and second gate circuits on one side.

The write-down input signal D_{IN} is applied to the gates of the MOSFETs Q_{29} and Q_{31} which are the inputs of the second gate circuit on the other side. A write-down input signal $\overline{D_{IN}}$ inverted by the inverter circuit IV is applied to the gates of the MOSFETs Q_{25} and Q_{27} which are the inputs of the first gate circuit on the other side.

In the circuit of this embodiment, the chip selection signal $\overline{CS}$ is held at the high level during the

chip non-selection, so that the MOSFETs Q_{28} and Q_{32} are held in the "on" states, while the MOSFETs Q_{26} and Q_{30} in the "off" states. Consequently, both the outputs of the first and second gate circuit are respectively made the low level irrespective of the write-down signal D_{IN} .

During the chip non-selection, accordingly, the leakage current supplied from the MOSFETs Q_{20} to the common data lines CD and $\overline{CD}$ through the MOSFETs Q_{21} and Q_{22} is supplied to the reference potential side through the MOSFETs Q_{18} and Q_{19} held in the "off" states and the MOSFETs Q_{32} and Q_{28} held in the "on" states at this time. As a result, the bias voltages on the common data lines can be prevented from rising.

During the chip selection, the MOSFETs Q_{26} and Q_{30} are held in the "on" states and the MOSFETs Q_{28} and Q_{32} in the "off" states by the low level of the chip selection signal CS , so that the output levels of the writing circuit 6 are determined in accordance with the write-down signal D_{IN} .

The circuit of this embodiment can favourably prevent the undersirable rises of the potentials of the common data lines, likewise to the embodiment shown in Figure 5. In addition, according to the present embodiment, the elements which increase stray capacitances as in the preceding embodiment are not

coupled to the common data lines CD and $\overline{\text{CD}}$. It is therefore possible to increase the speed of read-out of data.

The memory cells may be any known construction as long as they utilize a static flip-flop circuit.

Each memory cell may be formed of only p-channel or n-channel MOSFETs, in addition to the C-MOS circuit.

Furthermore, in the case where the level rises of the data lines as referred to above are not an important problem, as in the case where the capacitance value of the common data lines is large relative to that of the data lines, the resistors R_5 to R_8 etc., for the leakage current absorption with which the data lines are provided can be omitted.



CLAIMS:

1. A static memory including:

a static memory cell which has a selection terminal and a data terminal;

a signal line which is supplied with a data
5 signal delivered from said static memory cell;

a sense amplifier which is supplied with said data signal through said signal line;

a bias circuit which includes a MOSFET for applying a bias voltage to said signal line, said
10 bias voltage having a value lowered with respect to a power source voltage fed to a power source line; and

resistance means for supplying a current to said MOSFET to prevent an abnormal rise of a potential
15 of said signal line by a leakage current of said MOSFET, said resistance means being connected between said MOSFET and a reference potential point.

2. A static memory according to claim 1, wherein said resistance means is formed from a polycrystalline
20 silicon layer formed on a semiconductor substrate in which said static memory cell, said sense amplifier and said bias circuit are formed.



3. A static memory according to Claim 1, wherein said resistance means is constituted by a MOSFET formed in a semiconductor substrate in which said static memory cell, said sense amplifier and said bias circuit are formed.

4. A static memory according to Claim 3, wherein said MOSFET serving as said resistance means has the same channel conductivity type as that of said MOSFET in said bias circuit.

5. A static memory according to Claim 4, wherein said MOSFET serving as said resistance means has its gate coupled to its source.

6. A static memory including:

a plurality of static memory cells which are arranged in the form of a matrix and each of which has a selection terminal and a pair of data terminals;

a plurality of word lines each of which has the selection terminals of the static memory cells connected in common;

a plurality of paired data lines each of which has the paired data terminals of the static memory cells connected in common;

a pair of common data lines;

a switch circuit which coupled the paired data line to be selected amongst said plurality of



paired data lines, to said pair of common data lines;

a sense amplifier which has a pair of input terminals coupled to said pair of common data lines;

a bias circuit which includes a MOSFET for
5 applying bias voltages to said pair of common data lines, said bias voltages having values reduced with respect to a power source voltage fed to a power source line; and

resistance means for supplying a current to
10 said MOSFET to prevent an abnormal rise of a potential of said signal line by a leakage current of said MOSFET, said resistance means being connected between said MOSFET and a reference potential point.

7. A static memory according to Claim 6,
15 wherein said each static memory cell includes a pair of MOSFETs whose gates and drains are cross-coupled to each other, and a pair of resistance elements which are formed from polycrystalline silicon layers and which are respectively connected to the drains
20 of said pair of MOSFETs, and wherein said resistance means is also formed from a polycrystalline silicon layer.

8. A static memory according to Claim 6,
wherein said resistance means is constituted by a
25 MOSFET.



9. A static memory according to Claim 8, wherein said MOSFET serving as said resistance means has the same channel conductivity type as that of said MOSFET in said bias circuit.

10. A static memory according to Claim 6, wherein said bias circuit further includes a pair of MOSFETs which are switched-controlled by a chip selection signal, and wherein said pair of common data lines are brought to potentials equal to each other in such a way that said pair of MOSFETs in said bias circuit are rendered conductive.

11. A static memory according to Claim 6, further including:

a plurality of MOSFETs for applying bias voltages to the respective paired data lines, said bias voltages having values lowered with respect to said power source voltage fed to said power source line, and

a plurality of resistance elements which are connected between said respective paired data lines and said reference potential point.

12. A static memory according to Claim 6 or 7, wherein said resistance means comprises first and second resistors connected between the respective common data lines and the reference potential point.



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13. A static memory according to Claim 12, wherein said first and second resistors are formed from polycrystalline silicon layers.

14. A static memory according to Claim 6 or 7, wherein said resistance means comprises first and second MOSFETs.

15. A static memory according to any one of the preceding claims, wherein said sense amplifier comprises a pair of differential MOSFETs a constant-current element which supplies a constant current to sources of said differential MOSFETs connected in common, and load elements which are connected to drains of said differential MOSFETs.

16. A static memory according to Claim 15, wherein said sense amplifier is formed as a CMOS circuit.

17. A static memory constructed substantially as herein described with reference to and as illustrated in Figures 1 to 4, or in Figures 1 to 4 as modified by either Figure 5 or Figure 6 of the accompanying drawings.