METHOD TO FORM AN ELEVATED S/D CMOS DEVICE BY CONTACTING S/D THROUGH THE CONTACT OF OXIDE

Abstract

A method of fabrication of an elevated source / drain (S/D) for a MOS device. A first insulating layer having a gate opening and source/drain openings is formed over a substrate. The first insulating layer between the gate opening and the source / drain (S/D) openings are spacer blocks. We form a LDD resist mask having opening over the source/drain openings over the first insulating layer. Ions are implanted through the source/drain openings to form first lightly doped drain regions in the substrate. Then we remove the LDD resist mask. A first dielectric layer is formed on the substrate in the gate opening and source/drain openings. A gate is formed in the gate opening and raised source / drain (S/D) blocks in the source/drain openings. We remove the spacer blocks to form spacer block openings. We form second LDD regions by implanting ions through the spacer block openings. We form second spacer blocks in the spacer block openings. Plug opening are formed through the raised source / drain (S/D) blocks. Contact plugs are formed in the form plug opening. The invention's first and second LDD, contact plugs and elevated S/D regions reduce the Short Channel Effect (SCE).

Fig. 8