CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming pillar bump above a metallization system of a semiconductor chip; and

forming a plurality of notches in said pillar bump, wherein said plurality of notches are adapted to adjust a flexibility of said pillar bump when said pillar bump is exposed to a lateral force.

2. The method of claim 1, wherein forming said plurality of notches comprises positioning each of said plurality of notches along a side of said pillar bump in a substantially vertical alignment.

3. The method of claim 1, wherein forming said plurality of notches comprises positioning each of said plurality of notches along a side of said pillar bump that is oriented substantially away from a center of said semiconductor chip.

4. The method of claim 1, wherein forming said plurality of notches comprises forming at least three notches.

5. The method of claim 1, wherein forming said plurality of notches comprises forming an asymmetrically shaped notch.

6. The method of claim 1, wherein forming said plurality of notches comprises forming at least one of said plurality of notches with a tool having a radiused tip.

7. The method of claim 1, wherein forming said plurality of notches comprises forming at least one of said plurality of notches with a first tool having a first tool profile so as to form said at least one of said plurality of notches with a first notch profile, and using a second tool having a second tool profile to adjust a profile of said at least one of said plurality of notches from said first notch profile to a second notch profile.

8. The method of claim 7, wherein forming said at least one of said plurality of notches with said first tool comprises performing a lateral force test on said pillar bump with a test probe having said first tool profile.

9. The method of claim 1, wherein forming said plurality of notches comprises forming at least two first notches along a first side of said pillar bump and forming at least one second notch on a second side of said pillar bump, said second side being on an opposite side of said pillar bump from said first side.

10. The method of claim 9, further comprising positioning each of said at least two first notches on said pillar bump so that said first side is oriented substantially away from a center of said semiconductor chip and positioning said at least one second

notch on said pillar bump so that said second side is oriented substantially toward said center of said semiconductor chip.

11. The method of claim 1, further comprising supporting said pillar bump with a pillar bump support device while forming said plurality of notches.

12. The method of claim 11, wherein supporting said pillar bump with a pillar bump support device comprises positioning said pillar bump support device to be in contact with a first side of said pillar bump while forming one of said plurality of notches on a second side of said pillar bump, said pillar bump support device being adapted to resist a force imposed on said pillar bump by a tool that is used to form said one of said plurality of notches.

13. A method, comprising:

positioning a pillar bump support device in contact with a first side of a pillar bump formed above a metallization system of a semiconductor chip;

positioning a pillar bump repair device adjacent to a second side of said pillar bump;

forming a first notch on said second side of said pillar bump with said pillar bump repair device, wherein forming said first notch comprises imposing a force on said second side with said pillar bump repair device; and

supporting said pillar bump with said pillar bump support device while forming said first notch, wherein supporting said pillar bump comprises resisting,

with said pillar bump support device, said force being imposed on said second side of said pillar bump by actuation of said pillar bump repair device.

14. The method of claim 13, wherein positioning said pillar bump repair device adjacent to said second side comprises positioning said pillar bump repair device adjacent to an opposite side of said pillar bump from said first side.

15. The method of claim 13, wherein forming said first notch on said second side of said pillar bump comprises forming said first notch on a side of said pillar bump that is oriented substantially away from a center of said semiconductor chip,

16. The method of claim 13, further comprising forming at least one second notch on said second side of pillar bump with said pillar bump repair device while supporting said pillar bump with said pillar bump support device, wherein said at least one second notch is substantially vertically aligned with said first notch.

17. The method of claim 13, further comprising:

positioning said pillar bump support device in contact with said second side of said pillar bump;

positioning said pillar bump repair device adjacent to said first side of said pillar bump;

forming at least one further notch on said first side of said pillar bump with said pillar bump repair device by imposing a force on said first side with said pillar bump repair device; and

supporting said pillar bump with said pillar bump support device while forming said at least one further notch by resisting, with said pillar bump support collar, said force imposed on said first side of said pillar bump.

18. A device, comprising:

a plurality of pillar bumps formed above a metallization system of a semiconductor chip; and

a plurality of first notches formed on a first side of at least one of said plurality of pillar bumps, wherein each of said plurality of first notches is positioned along said first side in a substantially vertical alignment.

19. The device of claim 18, wherein said first side of said at least one of said plurality of pillar bumps is oriented substantially away from a center of said semiconductor chip.

20. The device of claim 18, further comprising a plurality of second notches formed on a second side of said at least one of said plurality of pillar bumps, wherein each of said plurality of second notches is positioned along said second side in a substantially vertical alignment.

21. The device of claim 18, wherein said metallization system comprises a plurality of metallization layers, and wherein at least one of said metallization layers comprises one of a low-k dielectric material and an ultra-low-k dielectric material.

22. The device of claim 18, wherein said at least one of said plurality of pillar bumps comprises copper.

23. A pillar bump support device, comprising:

a pillar bump contact surface that is adapted to contact an outer surface of a pillar bump formed above a metallization system of a semiconductor chip, wherein said pillar bump support device is adapted to substantially support said pillar bump when a force is imposed on said pillar bump during a pillar bump repair process.

24. The pillar bump support device of claim 23, wherein a contour of said pillar bump contact surface substantially conforms to a contour of at least a portion of said outer surface of said pillar bump.

25. The pillar bump support device of claim 24, wherein said contour of said pillar bump contact surface comprises a sector of a circle.

26. The pillar bump support device of claim 23, wherein said pillar bump support device is adapted to be positioned on a first side of said pillar bump when said

force is imposed on said pillar bump from a second side of said pillar bump that is opposite of said first side, said pillar bump support device being further adapted to substantially prevent said force from being transferred to said metallization system.

27. The pillar bump support device of claim 23, wherein said pillar bump support device comprises a resilient material.

CLAIMS

1. A method, comprising:

forming pillar bump above a metallization system of a semiconductor chip; and

forming a plurality of notches in said pillar bump, wherein forming each one of said plurality of notches comprises contacting a lateral side of said pillar bump with a notch-forming tool and imposing a substantially lateral force on said pillar bump with said tool, said plurality of notches being adapted to adjust a flexibility of said pillar bump when said pillar bump is exposed to a chip packaging interaction force.

2. The method of claim 1, wherein forming said plurality of notches comprises positioning each of said plurality of notches along said lateral side of said pillar bump in a substantially vertical alignment.

3. The method of claim 1, wherein forming said plurality of notches comprises positioning each of said plurality of notches along a lateral side of said pillar bump that is oriented substantially away from a center of said semiconductor chip.

4. The method of claim 1, wherein forming said plurality of notches comprises forming at least three notches.

5. The method of claim 1, wherein forming said plurality of notches comprises forming an asymmetrically shaped notch.

6. The method of claim 1, wherein forming said plurality of notches comprises forming at least one of said plurality of notches with a tool having a radiused tip.

7. The method of claim 1, wherein forming said plurality of notches comprises forming at least one of said plurality of notches with a first tool having a first tool profile so as to form said at least one of said plurality of notches with a first notch profile, and using a second tool having a second tool profile to adjust a profile of said at least one of said plurality of notches from said first notch profile to a second notch profile.

8. The method of claim 7, wherein forming said at least one of said plurality of notches with said first tool comprises performing a lateral force test on said pillar bump with a test probe having said first tool profile.

9. The method of claim 1, wherein forming said plurality of notches comprises forming at least two first notches along a first lateral side of said pillar bump and forming at least one second notch on a second lateral side of said pillar bump, said second lateral side being on a substantially opposite side of said pillar bump from said first lateral side.

10. The method of claim 9, further comprising positioning each of said at least two first notches on said pillar bump so that said first lateral side is oriented substantially away from a center of said semiconductor chip and positioning said at least one second notch on said pillar bump so that said second lateral side is oriented substantially toward said center of said semiconductor chip.

11. The method of claim 1, further comprising supporting said pillar bump with a pillar bump support device while forming said plurality of notches.

12. The method of claim 11, wherein supporting said pillar bump with a pillar bump support device comprises positioning said pillar bump support device to be in contact with a first lateral side of said pillar bump while forming one of said plurality of notches on a second lateral side of said pillar bump with said tool, said pillar bump support device being adapted to resist said substantially lateral force imposed on said pillar bump by said tool while forming said one of said plurality of notches.

13. The method of claim 1, further comprising, after forming said plurality of notches in said pillar bump, performing a flip-chip operation to attach said semiconductor chip to a carrier substrate.

14. A method, comprising:

positioning a pillar bump support device in contact with a first lateral side of a pillar bump formed above a metallization system of a semiconductor chip;

positioning a pillar bump repair device adjacent to a second lateral side of said pillar bump;

forming a first notch on said second lateral side of said pillar bump with said pillar bump repair device, wherein forming said first notch comprises imposing a substantially laterally oriented force on said second lateral side with said pillar bump repair device; and

supporting said pillar bump with said pillar bump support device while forming said first notch, wherein supporting said pillar bump comprises resisting, with said pillar bump support device, said substantially laterally oriented force being imposed on said second lateral side of said pillar bump by actuation of said pillar bump repair device.

15. The method of claim 14, wherein positioning said pillar bump repair device adjacent to said second lateral side comprises positioning said pillar bump repair device adjacent to an opposite side of said pillar bump from said first lateral side.

16. The method of claim 14, wherein forming said first notch on said second lateral side of said pillar bump comprises forming said first notch on a lateral side of said pillar bump that is oriented substantially away from a center of said semiconductor chip.

17. The method of claim 14, further comprising forming at least one second notch on said second lateral side of pillar bump with said pillar bump repair device while supporting said pillar bump with said pillar bump support device, wherein said at least one second notch is substantially vertically aligned with said first notch.

18. The method of claim 14, further comprising:

positioning said pillar bump support device in contact with said second lateral side of said pillar bump;

positioning said pillar bump repair device adjacent to said first lateral side of said pillar bump;

forming at least one further notch on said first lateral side of said pillar bump with said pillar bump repair device by imposing a further substantially laterally oriented force on said first lateral side with said pillar bump repair device; and

supporting said pillar bump with said pillar bump support device while forming said at least one further notch by resisting, with said pillar bump support collar, said force imposed on said first lateral side of said pillar bump.

19. The method of claim 14, further comprising, after forming said first notch in said pillar bump, performing a flip-chip operation to attach said semiconductor chip to a carrier substrate.

20. A method, comprising:

forming pillar bump above a metallization system of a semiconductor chip; and

forming a plurality of notches in said pillar bump, wherein forming at least one of said plurality of notches comprises using a first tool having a first tool profile to form said at least one of said plurality of notches with a first notch profile and using a second tool having a second tool profile to adjust a profile of said at least one of said plurality of notches from said first notch profile to a second notch profile, said plurality of notches being adapted to adjust a flexibility of said pillar bump when said pillar bump is exposed to a lateral force.

21. The method of claim 20, wherein forming said at least one of said plurality of notches with said first tool comprises performing a lateral force test on said pillar bump with a test probe having said first tool profile.

22. A method, comprising:

forming pillar bump above a metallization system of a semiconductor chip;

forming a plurality of notches in said pillar bump, wherein said plurality of notches are adapted to adjust a flexibility of said pillar bump when said pillar bump is exposed to a lateral force; and

supporting said pillar bump with a pillar bump support device while forming said plurality of notches, wherein supporting said pillar bump comprises positioning said pillar bump support device to be in contact with a first side of said pillar bump while forming each of said plurality of notches on a second side of said pillar bump, said pillar bump support device being adapted to resist a force imposed on said pillar bump by a tool that is used to form each of said plurality of notches.

23. A method, comprising:

positioning a pillar bump support device in contact with a first side of a pillar bump formed above a metallization system of a semiconductor chip;

positioning a pillar bump repair device adjacent to a second side of said pillar bump that is oriented substantially away from a center of said semiconductor chip;

forming a first notch on said second side of said pillar bump with said pillar bump repair device, wherein forming said first notch comprises imposing a force on said second side with said pillar bump repair device; and

supporting said pillar bump with said pillar bump support device while forming said first notch, wherein supporting said pillar bump comprises resisting, with said pillar bump support device, said force being imposed on said second side of said pillar bump by actuation of said pillar bump repair device.

24. The method of claim 23, wherein said first side of said pillar bump is laterally opposite of said second side.

25. A semiconductor devices formed in accordance with any one of the preceding claims.