Claims

1. A method for the manufacture of a semiconductor device, which comprises:

providing a first substrate;

providing a doped layer in a surface region of the first substrate;

providing a buried oxide layer on the doped layer;

providing a semiconductor layer on the buried oxide layer to obtain a semiconductor-on-insulator (SeOI) wafer;

removing the buried oxide layer and the semiconductor layer from a first region of the SeOI wafer while maintaining the buried oxide layer and the semiconductor layer in a second region of the SeOI wafer, wherein the buried oxide layer and the semiconductor layer in the second region are arranged only on parts of the doped layer;

providing an upper transistor in the second region by forming a back gate in or by the doped layer; and

providing a lower transistor in the first region by forming source and drain regions in or by the doped layer.

2. The method according to claim 1, wherein the lower transistor is a recessed channel array transistor.

3. The method according to claim 1, wherein the first region represents a memory cell area of a dynamic random-access memory (DRAM) device and the second region represents a core region or a region of periphery circuits of the DRAM device.

4. The method according to claim 1, wherein the SeOI wafer is provided by

forming the semiconductor layer on or as part of a second substrate;

forming the buried oxide layer by providing an oxide layer either on the semiconductor layer, on the doped layer of the first substrate, or on both layers;

bonding the first and the second substrates to provide the buried oxide layer in-between the semiconductor layer and the doped layer; and

removing the second substrate.

5. The method according to claim 1, wherein the providing of the doped layer comprises doping the surface region of the first substrate.

6. The method according to claim 1, wherein the providing of the doped layer comprises forming or epitaxially growing the doped layer on the surface of the first substrate.

7. The method according to claim 1, wherein one of the semiconductor layer or the first substrate or both includes or is silicon.

8. The method according to claim 1, wherein the doped layer includes an n or n+ dopant or a p or p+ dopant.

9. The method according to claim 1, wherein the removing of the buried oxide layer and the semiconductor layer from the first region of the SeOI wafer comprises:

providing a mask layer on the first and second regions;

providing a photoresist on the mask layer in the second region and exposing the first region;

removing the mask layer and the semiconductor layer in the first region;

removing the photoresist layer;

removing the mask layer in the second region; and

removing the buried oxide layer in the first region;

wherein the buried oxide layer is removed in the first region after removal of the mask layer in the second region.

10. The method according to claim 9 which further comprises providing an oxide layer on the first and second regions before providing the mask layer, with the oxide layer later being removed with the mask layer and the semiconductor layer in the first region.

11. The method according to claim 9, which further comprises:

providing a trench in the second region to separate a region where a p-channel transistor is present from a region where an n-channel transistor is present;

providing a trench separating the first from the second region;

providing a p-well and an n-well region of the first region; and

providing a recessed channel array transistor trench in the first region such that it extends into the p-well region that is present below the doped layer in the first region.

12. The method according claim 1, wherein the providing of the source and drain regions of the transistor in the first region is performed without further implanting dopants in the doped layer.

13. The method according to claim 1, wherein the providing of the source and drain regions of the transistor in the first region comprises implanting dopants in the doped layer to adjust the doping profile.

14. The method according to claim 1, which further comprises provided a doped silicon layer on the silicon layer adjacent to gate structures of the transistors present in the first and second regions in order to form source and drain regions.

15. The method according to claim 14, wherein the doped silicon layer on the silicon layer if provided by epitaxial growth of the doped silicon layer.

16. A method for the manufacture of a semiconductor device, which comprises:

providing a first substrate;

providing a doped layer in a surface region of the first substrate;

providing a second substrate;

forming the semiconductor layer on or as part of a second substrate;

forming the buried oxide layer by providing an oxide layer either on the semiconductor layer, on the doped layer of the first substrate, or on both layers;

bonding the first and the second substrates to provide the buried oxide layer in-between the semiconductor layer and the doped layer; and removing the second substrate, wherein the second substrate has a zone of weakness that defines the semiconductor layer, and the semiconductor layer is transferred to the first substrate by detaching at the zone of weakness;

removing the buried oxide layer and the semiconductor layer from a first region of the SeOI wafer while maintaining the buried oxide layer and the semiconductor layer in a second region of the SeOI wafer;

providing an upper transistor in the second region by forming a back gate in or by the doped layer; and

providing a lower transistor in the first region by forming source and drain regions in or by the doped layer.

17. A semiconductor on insulator (SeOI) wafer, comprising:

a substrate having a doped surface layer, wherein the substrate has three active regions including, one region where an n-channel FET will, be formed, one region where a p-channel FET will be formed and one region where a memory cell array will be formed;

a buried oxide layer arranged only on part but not all of the doped layer; and

a semiconductor layer arranged on the buried oxide layer that is arranged on the part of the doped layer.

18. The SeOI wafer according to claim 17, wherein the substrate and the semiconductor layer includes or is silicon and the doped layer comprises a refractory metal of Co, Ni, Ti, Mo, W or Ta.

19. The SeOI wafer according to claim 17, which further comprises a plurality of regions of buried oxide and semiconductor layers arranged on only parts of the doped layer and a plurality of regions wherein doped surface layer is exposed.

20. A dynamic random-access memory (DRAM) device comprising:

the SeOI wafer according to claim 17;

one or more p-channel or n-channel transistors in the region where the semiconductor layer and the buried oxide layer are provided, with the doped layer providing the back gate for the p-channel and/or n-channel transistors; and

a recessed channel array transistor for a memory cell array in the region of the wafer where no semiconductor layer and buried oxide layer are provided with the doped layer at least partly providing the source and drain regions for the recessed channel array transistor.

21. A method for the manufacture of a semiconductor device, which comprises:

providing a first substrate;

forming a doped layer on a surface region of the first substrate;

providing an oxide layer on the doped layer;

providing a semiconductor layer on the oxide layer to obtain a buried oxide layer and semiconductor-on-insulator (SeOI) wafer;

removing the buried oxide layer and the semiconductor layer from a first region of the SeOI wafer while maintaining the buried oxide layer and the semiconductor layer in a second region of the SeOI wafer; and

providing an upper transistor in the second region by forming a back gate in or by the doped layer; and

providing a lower transistor in the first region by forming source and drain regions in or by the doped layer.

22. The method of claim 21, which further comprises

forming or otherwise providing a p-well and an n-well region of the first region; and

forming or otherwise providing a recessed channel array transistor trench in the first region such that it extends into the p-well region formed below the doped layer in the first region.

23. The method of claim 22, wherein the p-well and n-well region in the first region are formed by implantation.

Claims

1. Method for the manufacture of a semiconductor device, comprising

providing a first substrate;

arranging a doped layer in a surface region of the first substrate;

arranging a buried oxide layer on the doped layer;

arranging a semiconductor layer on the buried oxide layer to obtain an SeOI wafer;

removing the buried oxide layer and the semiconductor layer from a first region of the SeOI wafer while maintaining the buried oxide layer and the semiconductor layer in a second region of the SeOI wafer;

forming an upper transistor in the second region;

forming a lower transistor, in particular, a recessed channel array transistor in the first region; wherein

forming the upper transistor in the second region comprises forming a back gate in or by the doped layer; and

forming the lower transistor, in particular, a recessed channel array transistor in the first region comprises forming source and drain regions in or by the doped layer.

2. The method according to claim 1, wherein the first region represents a memory cell area of a DRAM device and the second region represents a core region or a region of periphery circuits of the DRAM device.

3. The method according to claim 1 or 2, further comprising

providing a second substrate;

forming the semiconductor layer on the second substrate;

forming the buried oxide layer on the semiconductor layer and/or the doped layer;

bonding the first and the second substrate by the buried oxide layer; and

detaching the second substrate.

4. The method according to one of the preceding claims, wherein the step of forming the doped layer comprises doping the surface region of the first substrate.

5. The method according to one of the preceding claims, wherein the step of forming the doped layer comprises forming, in particular, epitactically growing, the doped layer on the surface of the first substrate.

6. The method according to one of the preceding claims, wherein the semiconductor layer consists of or comprises silicon and/or the first substrate consists of or comprises silicon.

7. The method according to one of the preceding claims, wherein the dopant of the doped layer is an n dopant, in particular, an n^+ dopant or a p dopant, in particular, a p^+ dopant.

8. The method according to one of the preceding claims, wherein removing the buried oxide layer and the semiconductor layer from the first region of the SeOI wafer comprises

forming a mask layer on the oxide layer in the first and second regions;

forming a photoresist on the mask layer in the second region and exposing the first region;

removing the mask layer and the semiconductor layer in the first region;

removing the photoresist layer;

removing the mask layer in the second region;

removing the oxide layer in the second region; and

removing the buried oxide layer in the first region; wherein

the buried oxide layer is removed in the first region after removal of the mask layer in the second region.

9. The method according to claim 8, further comprising

forming a trench in the second region to separate a region where a p-channel transistor is formed from a region where an n-channel transistor is formed;

forming a trench separating the first from the second region;

forming a p-well and an n-well region of the first region; and

forming a recessed channel array transistor trench in the first region such that it extends into the p-well region formed below the doped layer in the first region.

10. The method according to one of the preceding claims, wherein forming the source and drain regions of the transistor in the first region is performed without further implanting dopants in the doped layer.

11. The method according to one of the claims 1 to 9, wherein forming the source and drain regions of the transistor in the first region comprises implanting dopants in the doped layer to adjust the doping profile.

12. The method according to one of the preceding claims, further comprising forming a doped silicon layer, in particular, by epitactic growth, on the silicon layer adjacent to gate structures of the transistors formed in the first and second regions in order to form source and drain regions.

13. Semiconductor on insulator, SeOI, wafer, comprising

a substrate;

a doped layer formed in the region of a surface of the substrate;

a buried oxide layer arranged only on a part of the doped layer; and

a semiconductor layer arranged on the buried oxide layer arranged on the part of the doped layer to obtain the SeOI wafer.

14. The SeOI wafer according to claim 13, wherein the substrate and the semiconductor layer consists of or comprises silicon and the doped layer comprises a refractory metal, in particular, Co, Ni, Ti, Mo, W or Ta.

15. DRAM device comprising

the SeOI wafer according to claim 13 or 14;

one or more p-channel and/or n-channel transistors in the region where the semiconductor layer and the buried oxide layer are formed and wherein the doped layer provides the back gate for the p-channel and/or n-channel transistors; and

a recessed channel array transistor for a memory cell array in the region of the wafer where no semiconductor layer and buried oxide layer are provided and wherein the doped layer at least partly provides the source/drain regions for the recessed channel array transistor.