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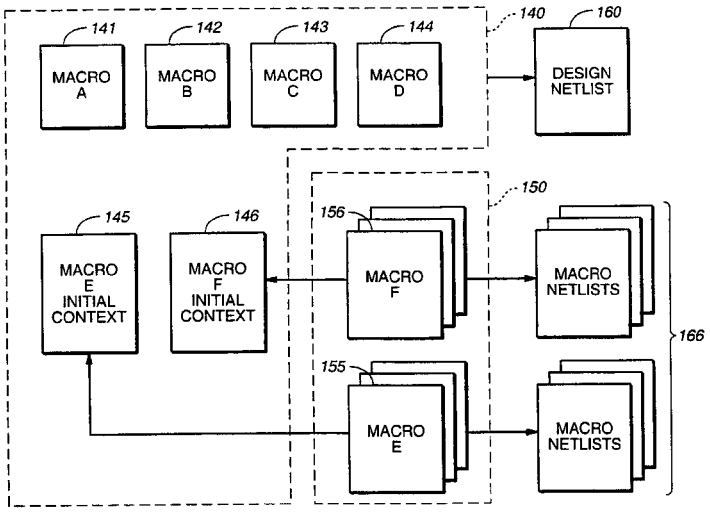
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(54) Title: METHOD FOR IMPLEMENTING A PHYSICAL DESIGN FOR A DYNAMICALLY RECONFIGURABLE LOGIC CIRCUIT



(57) Abstract: A method for implementing the physical design for a dynamically reconfigurable logic circuit. The method is carried out using software that forms a physical design flow to take a design specification from a schematic or high-level description language (HDL) through to FPGA configuration bitstream files. The method involves reading a design netlist (160) that was entered, the design netlist (160) including a set of static macros (140) and a set of reconfigurable macro contexts (150). Then, each of the reconfigurable macros (150) are compiled and an initial device context is placed and routed. The device context is updated by arbitrarily selecting a context for each reconfigurable macro, placing and routing the updated device context and repeating the steps of updating, placing and routing until all of the reconfigurable macro contexts have been placed and routed. Then, after the compilation process is complete, full, partial, and incremental bitstream files are generated.

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