ABSTRACT

QUAD FLAT NO-LEAD (QFN) GRID ARRAY PACKAGE, METHOD OF MAKING AND MEMORY MODULE AND COMPUTER SYSTEM INCLUDING SAME

A quad flat no-lead (QFN) grid array semiconductor package and method for making the same. The package includes a semiconductor die and a lead frame having conductive elements patterned in a grid-type array. A plurality of bond pads on the semiconductor die are coupled to the plurality of conductive elements, such as by wire bonding. The semiconductor die and a portion of at least a portion of the lead frame are encapsulated in an insulative material leaving the conductive elements exposed along a bottom major surface of the package for subsequent electrical connection with higher level packaging. Individual conductive lead elements, as well as the grid array pattern, are formed by wire bonding multiple bond pads to a single lead at different locations and subsequently severing the leads between the bonding locations to form multiple conductive elements from each individual lead.

[Figure 1]