a second portion of the electrically conductive layer extending from a second contact pad of the one of the second semiconductor die toward a center of the one of the second semiconductor die; and

a plurality of bumps formed on the electrically conductive layer over the second semiconductor die including a first bump disposed over the encapsulant and a second bump disposed between the first contact pad and second contact pad.

2. The semiconductor manufacturing system of claim 1, wherein the second semiconductor die are tested to confirm as known good semiconductor die.

3. The semiconductor manufacturing system of claim 1, wherein the surface area of the reconstituted wafer is 10-50% greater than the surface area of the semiconductor wafer.

4. The semiconductor manufacturing system of claim 1, wherein a surface of the encapsulant between the second semiconductor die is planar with a surface of the second semiconductor die.

5. A semiconductor manufacturing system, comprising:

a semiconductor wafer within the semiconductor manufacturing system and including a plurality of first semiconductor die arranged across a surface area of the semiconductor wafer to yield a first number of the first semiconductor die disposed on the semiconductor wafer given the surface area of the semiconductor wafer;

a reconstituted wafer within the semiconductor manufacturing system and including a plurality of second semiconductor die arranged across a surface area of the

portion of the encapsulant opposite the reconstituted wafer; and

a plurality of bumps formed on the electrically conductive layer over the second semiconductor die and over the encapsulant.

7. The system of claim 6, further including a mold as part of the semiconductor manufacturing system, wherein the mold is configured to shape the encapsulant to have the less than 5% deviation in distance between the first surface of the encapsulant and the second surface of the encapsulant by using a molding temperature of 80-150 °C, a molding time of 250-1000 seconds, a molding cure temperature of 100-180 °C, and a molding cure time of 20-120 minutes.

8. The system of claim 6, wherein a second portion of the electrically conductive layer extends from a second contact pad of the one of the second semiconductor die toward a center point of the one of the second semiconductor die.

9. The semiconductor manufacturing system of claim 6, wherein the second semiconductor die are tested to confirm as known good semiconductor die.

10. The semiconductor manufacturing system of claim 6, wherein the surface area of the reconstituted wafer is 10-50% greater than the surface area of the semiconductor wafer.