

ABSTRACT

The present invention aims to provide a liquid crystal display panel having a structure in which a plurality of gate electrodes are arranged on a continuous semiconductor layer and still capable of suppressing increase of a parasitic capacitance between a source region and a drain region. The liquid crystal display panel of the invention includes a thin film transistor (3) in a main surface (201u) of a first transparent substrate (201). The thin film transistor (3) includes: a base insulating film (4); a semiconductor layer (5) extending linearly at least from a first portion (51) to a second portion (52); a source electrode (7); a drain electrode (8); and gate electrodes (9) arranged at two or more locations along the semiconductor layer, respectively, to cover the semiconductor layer (5) with a gate insulating film (6) therebetween. Between the base insulating film (4) and the first transparent substrate (201), a light shielding film (11) is arranged to cover each projection region (10) of the main surface (201u), which is a region corresponding to projection of the gate electrode (9) on the main surface. The light shielding film (11) is arranged in the form of a plurality of light shielding film elements (12). The light shielding film elements (12) each cover one or more projection regions (10).