Method of Forming $CoSi_x$

TECHNICAL FIELD

[0001] The present invention relates generally to the manufacturing of semiconductor devices, and more particularly to a method of forming cobalt silicide.

BACKGROUND

[0002] In semiconductor device manufacturing, silicide formation is commonly used to reduce the resistance of semiconductor materials. Silicide formation typically comprises forming a metal on top of a surface of the semiconductor material, such as polysilicon. Silicides are often formed on gates, sources, and drains of transistors, and also on local interconnects, as examples. Silicide formed on source and drain regions reduces the sheet resistance of the path between an adjacent metal contact and the channel edge of the transistor, for example. One type of silicide is referred to as a salicide, or self-aligned silicide.

[0003] Figures 1A through 1D show a prior art method of forming a silicide over a silicon surface in a cross-sectional view. Referring first to Figure 1A, a semiconductor device 100 comprising a workpiece 101 has a silicon region 102 on a top surface thereof. The silicon region 102 has a native oxide 103 formed thereon. An argon sputter is used to remove the native oxide 103, and a cobalt layer 104 is deposited over the silicon region 102, as shown in Figure 1B. A titanium nitride (TiN) cap 106 is deposited over the cobalt layer 104. The workpiece 100 is annealed in a first anneal process to form cobalt silicide ($CoSi_x$) 108 at the top surface of the silicon region 102, as shown in Figure 1C. A selective etch is then performed to remove the TiN cap 106 and any unreacted cobalt 104 from the top surface of the workpiece 100, leaving behind a layer of $CoSi_x$ 108 on the top surface of the silicon region 102, as shown in Figure 1D. The

workpiece 100 is then annealed in a second anneal process, typically at a higher temperature than the first anneal process, to convert the $CoSi_x$ 108 to a lower resistance phase of the $CoSi_x$ material.

[0004] One problem with the method shown in Figures 1A through 1D is that it results in the formation of poor quality $CoSi_x$. Another problem with the prior art silicide formation process shown in Figures 1A through 1D is that the argon sputter cleaning process can cause device failures, due to $CoSi_x$ residue forming under the spacer film, as shown in Figure 1E. Figure 1E illustrates a transistor 112 having silicon regions 102 that comprise a source S, drain D and gate G. A gate oxide 114 resides beneath the gate G. A thin oxide 116 is formed over the gate G sidewalls and over the top surface of a portion of the source S and drain D, as shown. A spacer 118 which may comprise polysilicon is formed over the thin oxide 116, over the gate G sidewalls.

[0005] The argon sputter process may over-etch the thin oxide 116, forming a reentrant profile 120 beneath the spacers 118, as shown. During the argon sputter process, silicon atoms may lodge or be formed in the reentrant profile 120, to form an undesired silicide region beneath the bottom of the spacers 118, as shown in Figure 1E. When the cobalt layer 104 (not shown in Figure 1E; see Figure 1B) is deposited, cobalt is also deposited into the reentrant profile 120. Thus, during the anneal process, undesired cobalt silicide 122 is also formed beneath the spacers 118, which can cause shorts and which may also induce a leakage problem, if the undesired cobalt silicide 122 is not removed in subsequent chemical strip processes.

[0006] Another prior art method for forming $CoSi_x$ is shown in Figures 2A through 2C in cross-sectional views. A workpiece 201 having a silicon region 202 has a native oxide 203 formed thereon, as shown in Figure 2A. In this method, the native oxide 203 is not removed. A

cobalt layer 204 is deposited over the oxidized silicon region 202. A titanium (Ti) cap layer 224 is deposited over the cobalt layer 204. The workpiece 201 is then annealed in a first anneal process to form $CoSi_x$ 208, as shown in Figure 2B. As in the first prior art process described, the Ti cap layer 224 is removed, along with any unreacted cobalt 204, leaving the structure shown in Figure 2C. The workpiece 201 is then annealed again in a second anneal process to convert the $CoSi_x$ 208 formed to a less resistive phase material.

[0007] However, there are problems with the prior art process shown in Figures 2A through 2C. In this process, the titanium 224, or a portion thereof, diffuses through the cobalt 204 during the first anneal step in order to remove the native oxide 203. However, it is difficult to control the amount of titanium 224 that diffuses through the cobalt 204 to the silicon region 202 surface. Furthermore, the diffusion of the titanium 224 through the cobalt 204 impacts deleteriously the resistance of the $CoSi_x$ material 208 formed. Thus, if the native oxide 203 is not removed by an argon sputter clean process, this results in resistance "R_s tailing", or an increase in the cumulative probability of an increase in the resistance of the resulting conductive material formed, in particular the combined silicon region 201 and the $CoSi_x$ formed 208.

[0008] Therefore, what is needed in the art is an improved method of forming $CoSi_x$ over silicon regions of a semiconductor device.

SUMMARY OF THE INVENTION

[0009] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention, which provide a method of forming a $CoSi_x$ layer on a silicon region by first depositing a thin titanium layer over the silicon region, depositing a cobalt layer over the thin titanium layer, and

depositing a TiN layer over the cobalt layer. The thin titanium layer reduces the oxide on the surface of the silicon region, and therefore results in a $CoSi_x$ layer having reduced resistance and increased conductivity.

[0010] In accordance with a preferred embodiment of the present invention, a method of forming a silicide layer over a semiconductor surface includes providing a workpiece, the workpiece having a top surface with a semiconductor region exposed, and depositing an oxide reduction layer on the semiconductor surface. A cobalt layer is deposited over the oxide reduction layer, a titanium nitride layer is deposited over the cobalt layer, and the workpiece is annealed to form cobalt silicide over the semiconductor region top surface.

[0011] In accordance with another preferred embodiment of the present invention, a method of forming a silicide layer over a semiconductor surface includes providing a workpiece, the workpiece having a top surface with a silicon region exposed, the silicon region having a native oxide thereon. Without cleaning the silicon region with an argon sputter clean process, an oxide reduction layer is deposited on the native oxide. A cobalt layer is deposited over the oxide reduction layer, a titanium nitride layer is deposited over the cobalt layer, and the workpiece is annealed to form cobalt silicide over the semiconductor region top surface.

[0012] In accordance with yet another preferred embodiment of the present invention, a method of forming cobalt silicide includes providing a workpiece, the workpiece having a top surface with a silicon region exposed, the silicon region having a native oxide thereon. Without first cleaning the silicon region with an argon sputter clean process, 30 Angstroms or less of titanium are deposited over the native oxide, 50 to 100 Angstroms of cobalt are deposited over the titanium, and 100 to 200 Angstroms of titanium nitride are deposited over the cobalt. The workpiece is annealed to form 350 to 600 Angstroms of cobalt silicide over the semiconductor

region top surface, the titanium nitride and unreacted cobalt are removed from over the cobalt silicide, and the workpiece is annealed to reduce the resistance of the cobalt silicide.

[0013] Embodiments of the invention achieve technical advantages by providing an improved method of forming $CoSi_x$ over silicon regions of a semiconductor device. Because an argon sputter cleaning process is not used to clean the native oxide from the surface, there is reduced risk of device failures and poor cobalt formation. The thickness of thin titanium layer that comprises the oxide reduction layer is easily controllable and easy to optimize. Furthermore, the method does not require the diffusion of titanium through the cobalt layer.

[0014] The foregoing has outlined rather broadly the features and technical advantages of embodiments of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of embodiments of the invention will be described hereinafter, which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0016] Figures 1A through 1E show cross-sectional views of a prior method of forming $CoSi_x$, wherein a titanium nitride cap layer is formed over a cobalt layer prior to an annealing step;

[0017] Figures 2A through 2C illustrate another prior art method of forming $CoSi_x$, wherein a titanium cap layer is disposed over a cobalt layer, and the titanium diffuses through the cobalt layer to reduce native oxide at the semiconductor surface;

[0018] Figures 3-7 illustrate cross-sectional views of a method of forming $CoSi_x$ in accordance with an embodiment of the present invention, wherein a thin titanium layer formed over the semiconductor surface reduces any native oxide residing on the surface; and

[0019] Figure 8 shows a transistor having silicon regions that have been silicided using an embodiment of the method described herein.

[0020] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0021] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0022] With reference now to Figure 3, therein is shown a semiconductor device 300 including a workpiece 301. The workpiece 301 may comprise silicon oxide disposed over a

single crystal silicon wafer. The workpiece 301 may include other conductive layers or other semiconductor elements, e.g., transistors, diodes, etc. (not shown). Compound semiconductors such as GaAs, InP, Si/Ge, SiC, for example, may be used in place of silicon.

[0023] The workpiece 301 includes a semiconductor region 302 formed at a top surface thereof. Only one semiconductor region 302 is shown in Figure 3; however, there may be several over semiconductor regions 302 and other elements and conductive or insulating material regions formed within the top surface of the workpiece 301, not shown. The semiconductor region 302 in a preferred embodiment comprises a region of silicon, such as polycrystalline silicon, although alternatively, the silicon region 302 may comprise amorphous silicon, for example.

[0024] The top surface of the silicon region 302 is next cleaned to remove or reduce any native oxide formed on the silicon region 302 top surface. The cleaning step preferably comprises a 100:1 HF acid solution for 60 to 90 seconds, for example. Alternatively, the silicon region 302 may be cleaned with alternative cleaning solutions and methods, as examples. Preferably, however, in particular, in accordance with embodiments of the present invention, the silicon region 302 is not cleaned with an argon sputter cleaning, which can cause damage to the silicon region 302 surface. The cleaning process for the top surface of the silicon region 302 removes some of the native oxide 303 present on the silicon region 302 surface, for example. While the cleaning step is preferred, the cleaning step is optional, in accordance with an embodiment of the invention.

[0025] An oxide reduction layer 330 is then formed or deposited over the silicon region 302, as shown. The oxide reduction layer 330 preferably comprises a thin layer of titanium, and alternatively may comprise other materials adapted to reduce the oxide, for example, a native

oxide 303 in the amount of 15 Angstroms or less that may reside over the top surface of the silicon region 302, for example. In one embodiment, the oxide reduction layer 330 may comprise a thickness of 30 Angstroms or less, for example, although more preferably, the oxide reduction layer 330 comprises a thickness of 10 Angstroms or less. The oxide reduction layer 330 may be deposited using a sputter process, for example. Advantageously, the oxide reduction layer 330 reacts with any native oxide 303 residing on the top surface of the silicon region 302 in a subsequent anneal step, to be described further herein.

[0026] Next, a cobalt layer 332 is deposited over the oxide reduction layer 330. For example, the cobalt layer 332 may be deposited in a thickness of 50 to 100 Angstroms, and more preferably, the cobalt layer 332 is deposited in a thickness of about 80 Angstroms. The cobalt layer 332 may be deposited by a sputter deposition process, as an example.

[0027] A titanium nitride (TiN) layer 334 is next deposited over the cobalt layer 332, as shown in Figure 5. The TiN layer 334 is preferably 100 to 200 Angstroms thick and may be deposited by a sputter deposition, as examples.

[0028] The workpiece 301 is then subjected to a first anneal process. In the first portion, e.g., in the first few seconds, of the first anneal process, the oxide reduction layer 330 reacts with the native oxide to form a layer of $Ti_xSi_yO_z$ 335 over the silicon region 302 surface, as shown in Figure 4. The mechanism of the reaction can be represented by Eq. 1:

Eq. 1: $$Ti+SiO_2 \Rightarrow Ti_xSi_yO_z$$

As the first anneal process continues, the cobalt 332 diffuses through the $Ti_xSi_yO_z$ 335 layer to form a layer of $CoSi_x$ 336 over and abutting the silicon region 302 surface, as shown in Figure 5.

By the end of the first anneal process, the $Ti_xSi_yO_z$ 335 layer has moved to the top of the $CoSi_x$ 336 layer, as shown in Figure 6.

[0029] Thus, during the first anneal process, a layer of $CoSi_x$ 336 is formed over the top surface of the silicon region 302, as shown in Figure 6. During the first anneal process, which is preferably at a temperature of 500 °C for about 30 seconds, as an example, the oxide reduction layer 330 (shown in Figure 3) is caused to react with any native oxide 303 on the surface of the silicon region 302, and diffuse up through the cobalt layer 332. The first anneal process also results in the formation of a layer of unreacted cobalt 332 over the $CoSi_x$ layer 336, and a portion of the TiN layer 334 is left residing over the unreacted cobalt layer 332 and $Ti_xSi_yO_z$ 335 layer, as shown in Figure 6.

[0030] A selective etch is performed on the workpiece 301 to remove the TiN layer 334, the $Ti_xSi_yO_z$ 335 layer, and the unreacted cobalt 332 from over the $CoSi_x$ layer 336, as shown in Figure 7. Next, the workpiece 301 is subjected to a second anneal process, for example, at a temperature of 850°C for about 30 seconds. The second anneal process is used to convert the $CoSi_x$ layer 336 to a low resistance phase material. The workpiece 301 is then exposed to subsequent processes to continue of the manufacturing of the semiconductor device 300.

[0031] A semiconductor device 300 comprising a transistor 340 manufactured in accordance with an embodiment of the present invention is shown in Figure 8. $CoSi_x$ 336 is formed over silicon regions 302, which comprise a source S, drain D, and gate G, using the method described with reference to Figures 3 through 7. Advantageously, there is no formation of undesired silicided regions beneath the spacers 318.

[0032] Embodiments of the invention provide an improved method of forming $CoSi_x$ 336 over silicon regions 302 of a semiconductor device. Because an argon sputter cleaning step is

not used to clean the native oxide 303 from the silicon region 302 surface, there is reduced risk of device failures and poor cobalt formation. The thin titanium layer that comprises the oxide reduction layer 330 has a thickness that is easy to control and to optimize. The method does not require the diffusion of titanium through the cobalt layer 332 because a TiN cap layer 334 is used.

[0033] Although embodiments of the present invention and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, it will be readily understood by those skilled in the art that the materials and processes described herein may be varied while remaining within the scope of the present invention. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. A method of forming a silicide layer over a semiconductor surface, the method comprising:

providing a workpiece, the workpiece having a top surface with a semiconductor region exposed;

depositing an oxide reduction layer on the semiconductor surface;

depositing a cobalt layer over the oxide reduction layer;

depositing a titanium nitride layer over the cobalt layer; and

annealing the workpiece to form cobalt silicide over the semiconductor region top surface.

2. The method according to Claim 1, wherein depositing the oxide reduction layer comprises depositing Ti.

3. The method according to Claim 2, wherein depositing the oxide reduction layer comprises sputtering the oxide reduction layer material.

4. The method according to Claim 2, wherein depositing the oxide reduction layer comprises depositing the oxide reduction layer in a thickness of 30 Angstroms or less.

5. The method according to Claim 1, wherein the workpiece is not cleaned with an argon sputter clean process before depositing the oxide reduction layer.

6. The method according to Claim 1, further comprising cleaning the semiconductor surface with a 100:1 HF acid for 60 to 90 seconds, before depositing the oxide reduction layer.

7. The method according to Claim 1, wherein the workpiece further comprises a native oxide layer formed over the semiconductor region, wherein the oxide reduction layer reduces the native oxide layer on the semiconductor region surface.

8. The method according to Claim 1, wherein the semiconductor region comprises silicon, polycrystalline silicon, or amorphous silicon.

9. The method according to Claim 1, further comprising:

removing the titanium nitride layer and unreacted cobalt from the workpiece; and

annealing the workpiece to reduce the resistance of the cobalt silicide.

10. The method according to Claim 1, wherein annealing the workpiece further comprises:

forming $Ti_xSi_yO_z$ over and abutting the semiconductor region top surface; and

diffusing the cobalt layer through the $Ti_xSi_yO_z$ to form the cobalt silicide over the semiconductor region top surface.

11. A method of forming a silicide layer over a semiconductor surface, the method comprising:

providing a workpiece, the workpiece having a top surface with a silicon region exposed, the silicon region having a native oxide thereon;

without cleaning the silicon region with an argon sputter clean process, depositing an oxide reduction layer on the native oxide;

depositing a cobalt layer over the oxide reduction layer;

depositing a titanium nitride layer over the cobalt layer; and

annealing the workpiece to form cobalt silicide over the semiconductor region top surface.

12. The method according to Claim 11, wherein depositing the oxide reduction layer comprises depositing Ti.

13. The method according to Claim 12, wherein depositing the oxide reduction layer comprises a sputtering process.

14. The method according to Claim 13, wherein depositing the oxide reduction layer comprises depositing Ti in a thickness of 30 Angstroms or less.

15. The method according to Claim 11, further comprising cleaning the semiconductor surface with a 100:1 HF acid for 60 to 90 seconds, before depositing the oxide reduction layer.

16. The method according to Claim 11, wherein the oxide reduction layer reduces the native oxide layer on the semiconductor region surface.

17. The method according to Claim 11, further comprising:

removing the titanium nitride layer and unreacted cobalt from the workpiece; and

annealing the workpiece to reduce the resistance of the cobalt silicide.

18. The method according to Claim 17, wherein annealing the workpiece to form cobalt silicide comprises an anneal process of about 500 degrees C for about 30 seconds, and wherein annealing the workpiece to reduce the resistance of the cobalt silicide comprises an anneal process of about 850 degrees C for about 30 seconds.

19. The method according to Claim 11, wherein annealing the workpiece further comprises forming $Ti_xSi_yO_z$ over and abutting the semiconductor region top surface, in a first portion of the annealing step.

20. The method according to Claim 19, wherein the cobalt layer diffuses through the $Ti_xSi_yO_z$ during the annealing step.

21. The method according to Claim 20, further comprising:

removing the titanium nitride layer, $Ti_xSi_yO_z$, and unreacted cobalt from the workpiece; and

annealing the workpiece to reduce the resistance of the cobalt silicide.

22. A method of forming cobalt silicide, the method comprising:

providing a workpiece, the workpiece having a top surface with a silicon region exposed, the silicon region having a native oxide thereon;

without first cleaning the silicon region with an argon sputter clean process, depositing 30 Angstroms or less of titanium over the native oxide;

depositing 50 to 100 Angstroms of cobalt over the titanium;

depositing 100 to 200 Angstroms of titanium nitride over the cobalt; and

annealing the workpiece to form 350 to 600 Angstroms of cobalt silicide over the semiconductor region top surface;

removing the titanium nitride and unreacted cobalt from over the cobalt silicide; and

annealing the workpiece to reduce the resistance of the cobalt silicide.

23. The method according to Claim 22, further comprising cleaning the semiconductor surface with a 100:1 HF acid for 60 to 90 seconds, before depositing the titanium over the native oxide.

24. The method according to Claim 22, wherein annealing the workpiece to form cobalt silicide comprises an anneal process of about 500 degrees C for about 30 seconds, and wherein annealing the workpiece to reduce the resistance of the cobalt silicide comprises an anneal process of about 850 degrees C for about 30 seconds.

25. The method according to Claim 22, wherein annealing the workpiece further comprises forming $Ti_xSi_yO_z$ over and abutting the semiconductor region top surface, in a first portion of the annealing step.

26. The method according to Claim 25, wherein the cobalt layer diffuses through the $Ti_xSi_yO_z$ during the annealing step.

27. The method according to Claim 26, wherein removing the titanium nitride and unreacted cobalt further comprises removing the $Ti_xSi_yO_z$ from the workpiece.