

SEMICONDUCTOR PACKAGE AND METHOD OF FABRICATION THEREOF

5 FIELD OF INVENTION

The present invention relates broadly to a semiconductor package and to a method of fabrication thereof.

10 BACKGROUND

The semiconductor industry is currently aiming at complying with several ongoing initiatives to promote or regulate electronic products that are free of pollutants. One such initiative is the European Directive for Restriction of Hazardous Substances (RoHS),
15 which calls for the reduction or removal of lead as well as several other elements and compounds which are liable for causing hazards to the environment.

The typical plating method used in fabrication of semiconductor packages is to solder plate a leadframe with lead and tin after an encapsulation/molding process. In line
20 with the ongoing initiative to reduce pollutants, some environmentally friendly tin-based materials such as tin, tin/bismuth, tin/silver are proposed to replace the lead content in solder. However, the presence of tin without lead triggers whisker formation which causes short circuits between leads of the leadframe. Such whisker formation is difficult to eradicate in an ongoing production. In addition, alloys of tin with bismuth, copper or
25 silver are also known to be liable for whisker formation. Thus, the current post-encapsulating plating techniques have not been successful in providing a satisfactory lead-free method of fabricating semiconductor packages.

One suggested lead-free semiconductor package fabrication method is to plate
30 the entire leadframe with nickel (Ni), palladium (Pd) and gold (Au) as a solderable finish before the encapsulation/molding process. However, this method results in poor or lower adhesion values between a molding compound and the entirely-Ni-Pd-Au-plated

leadframe and this poses problems like water seepage into the package and consequently reducing the moisture sensitivity level (MSL) performance for the package.

5 To improve the adhesion, the leadframes are roughened by treating the leadframes with an additive containing a peroxide based micro-etch to form an organo-metallic layer based on copper on top of the roughened leadframe. This can provide mechanical and chemical bonding for increased adhesion to the molding compounds.

10 Another suggested lead-free semiconductor package fabrication method is to plate the leadframe selectively with nickel, palladium and gold as a solderable finish. The method involves reel-reel selectively plating the leadframe or a metal substrate comprising the steps of applying onto the substrate a polymeric resist layer followed by removing selected areas of the resist layer according to a predetermined pattern and subjecting the substrate to metal electroplating at the exposed areas thereof, where said
15 selective removal is effected by means of a laser beam.

This can for example be achieved by first masking the leadframe with a electrophoretic coating. The coating resist on the areas to be plated can then be removed using laser irradiation which passes through the coating resist and heating the
20 leadframe and thereby causing ablative removal of the plating resist over the selectively laser irradiated areas of the leadframe. Only the areas without the coating or photoresist are then plated with Nickel, Palladium and Gold.

The above method reduces wastage of plating materials and saves cost and may
25 improve the adhesion between the moulding compound and the leadframe. However, the removal of the coating or photoresist by laser irradiation is slow and tedious as the throughput or speed of the laser to remove the areas of coating or photoresist is limited.

Furthermore, practically, it is difficult to ensure that the mask is fully aligned with
30 the later package dimensions. Mis-alignment between the masked area and the package may reduce the MSL performance of the package.

Hence, there is a need to provide a method which addresses at least one of the above-mentioned problems.

SUMMARY

5 In accordance with a first aspect of the present invention there is provided a method of fabricating a semiconductor package, the method comprising the steps of encapsulating a die mounted on a metal leadframe using a moulding compound; and plating leads of the metal leadframe with a coating comprising Ni, Pd, and Au after the encapsulation of the die.

10 The method may further comprise the step of trimming of tie bars between the leads of the leadframe before or after plating the leads.

The plating may be performed mask-less directly on the metal leadframe with the encapsulated die thereon.

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The plating step may comprise electro-plating of the metal leadframe substantially exactly from the periphery of a moulding encapsulation of the encapsulated die.

20 An encapsulation material for the die is substantially non-conductive, and the coating is formed only on exposed areas of the leadframe substantially exactly from the periphery of the moulding encapsulation of the encapsulated die.

25 The step of plating the leads of the leadframe may comprise forming the coating of Ni, Pd and Au on all exposed surfaces of the leads.

The step of encapsulating the die may comprise forming a moulding on top and bottom surfaces of the leadframe.

30 In accordance with a second aspect of the present invention there is provided a semiconductor package comprising a metal leadframe; an encapsulated die mounted on the leadframe; and a coating comprising Ni, Pd, and Au on the leads of the leadframe; wherein the coating is formed substantially exactly from a periphery of a moulding encapsulation of the encapsulated die.

The leads of the leadframe may be coated with Ni, Pd, Au in areas where tie bars have been trimmed before the plating of the leads.

5 The leads may be coated on all exposed surfaces thereof.

The moulding encapsulation may comprise a moulding on top and bottom surfaces of the leadframe.

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BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

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Figure 1 shows a photo of a leadframe of a semiconductor package according to an example embodiment.

20 Figures 2a) to d) are schematic cross-sectional drawings illustrating a leadframe preparation process according to an example embodiment.

Figure 3 shows a step of trimming of tie bars from leads of a leadframe according to an example embodiment.

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Figures 4a) to c) are schematic cross-sectional drawings illustrating a leadframe finishing process according to an example embodiment.

Figure 5 shows a schematic diagram of a set-up for electro-plating according to an example embodiment.

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DETAILED DESCRIPTION

The example embodiments described herein provide a method of lead-free plating of nickel, palladium and gold onto a leadframe after an encapsulation process.

Figure 1 shows a diagram of a metal leadframe 102 in an example embodiment.

- 5 The leadframe 102 comprises of a die pad 104 and a plurality of leads 106. The die pad 104 is attached to the leadframe 102 by supporting members 108. The plurality of leads 106 are secured by the respective tie bars 110. The leadframe 102 is usually supplied in reels and is cut into the desired size for assembly purposes.
- 10 Figures 2a) to d) show the various steps of a leadframe preparation process in the example embodiment. At step (a), the leadframe 102 is provided with silver bond pads 202. The leadframe may be formed from A42 alloy or copper. The silver bond pads 202 facilitate a wire bonding process, for example using gold wires. At step (b), a die 204 is mounted on the die pad 104 of the leadframe 102. Each die (e.g. 204) comprises an
- 15 individual printed integrated circuit. At step (c), wire bonding is carried out. Wire bonding provides electrical connection between the die 204 and the leads (106 of Figure 1) of the leadframe 102 by using wires 206. The wires 206 used in wire bonding are usually made of gold or aluminium. At step (d), encapsulation is carried out, the moulding encapsulation comprising a moulding 208 on top and bottom surfaces of the leadframe
- 20 102. Encapsulation protects the various components in the moulding 208 from physical and chemical damage. An example of the moulding compound is an epoxy compound.

- Figure 3 shows the step of trimming of the tie bars 110 from the leads 106 of the leadframe 102 in the example embodiment. The tie bars 110 are trimmed after
- 25 encapsulation and can be trimmed before or after the process of plating of the leads 106. If the tie bars 110 are trimmed before plating, this enables the whole of the leads 106 to be plated and advantageously prevents exposure of copper portions 302 of the leads 106 to air, which could result in corrosion if the trimming is performed after plating.

- 30 Figure 4a) to e) shows the various steps of a leadframe finishing process in the example embodiment. At step (a), the surface of the leadframe 102 is treated by chemical and/or mechanical means for preparation of plating of the leadframe 102. At step (b), all exposed surfaces of the leads (106 of Figure 1) of the leadframe 102 are electro-plated with nickel to form a nickel-plated surface 402. At step (c), palladium is

electro-plated on the nickel-plated surface 402 to form a palladium-plated surface 404. At step (d), gold is electro-plated on the palladium-plated surface 404 to form a gold-plated surface 406.

5 In the example embodiment, the moulding 208 is used as the mask during the electro-plating of the leads of the lead from 102. Plating is thus carried out substantially exactly from the periphery of the moulding 208. The Ni/Pd/Au coating 402, 404, and 406 is formed directly adjacent and extends outwardly from sidewalls 405 of the moulding 208. Therefore, the plating is advantageously self-aligned with the moulding 208
10 dimensions. This can ensure a high MSL performance of the resulting semiconductor package.

 Further, advantageously fewer process steps are involved in the example embodiment compared to existing selective Ni/Pd/Au plating techniques, as the steps of
15 masking and removal of coating or photoresist are not required in the example embodiment. Also, the moulding 208 in addition to the areas underneath the moulding 208 are not electro-plated with nickel, palladium and gold as the moulding 208 material is not conductive. This reduces wastage of materials and saves costs.

20 A schematic diagram of a set-up for electro-plating is shown in Figure 5 in the example embodiment. To facilitate plating of the leads 106 of the leadframe 102, an anode 502 and the leadframe 102 are immersed in a plating solution 504. The plating solution 504 in a plating tank 506 contains a salt of the metal e.g. nickel, palladium or gold, which are to be plated on the leads 106 of the leadframe 102. The
25 anode 502 and the leadframe 102 are connected to a power supply 508, with the leadframe 102 being a cathode. An example voltage and current are about 5V and about 20A respectively.

 Referring back to Figure 4, lead forming is carried out at step (e). The plated
30 leads (106 of Figure 1) of the leadframe 102 are formed into the desired shape for mounting onto a circuit board (not shown). After step (e), the assembled semiconductor package 408 is sent for electrical testing.

The example embodiment described above with reference to Figures 2 to 5 provides a lead-free semiconductor package fabrication process in which the leadframe is plated after moulding compound encapsulation of the die. Importantly, unlike previous post-encapsulating plating techniques, the Ni/Pd/Au coating used
5 was found to not exhibit whisker formation while achieving better solderability and bondability.

Further, as mentioned above, example embodiments of the present invention can achieve an assembly process with fewer steps than in existing selective plating
10 techniques, and using existing equipments and processes. This is achieved by using the moulding as the mask and plating the leadframe exactly from the periphery of the moulding. The plating is thus preferably exactly aligned with the moulding dimensions. The steps of masking and removal of coating or resist are not required in this process. This can also reduce wastage of photoresist. Further, the moulding area in addition to
15 the areas underneath the moulding compound encapsulation are not plated with nickel, palladium and gold, reducing wastage of those precious materials and saving costs.

Example embodiments of the present invention can also reduce damage of the plated surfaces if the tie bars are trimmed from the leads before plating is performed
20 and due to less handling of the plated leads if the leads are plated after the encapsulating of the die.

It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific
25 embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

For example, the shape and configuration of the leadframe is not limited to that
30 shown in the example embodiments. Other shapes, configurations, or both can be used in different embodiments, including differently shaped die pads, leads and bond pads.

Furthermore, it will be appreciated that different materials for the leadframe and the moulding compound for encapsulation of the die may be used in different embodiments.

CLAIMS

1. A method of fabricating a semiconductor package, the method comprising the steps of:
 - 5 encapsulating a die mounted on a metal leadframe using a moulding compound;
and
 plating leads of the metal leadframe with a coating comprising Ni, Pd, and Au after the encapsulation of the die.
- 10 2. The method as claimed in claim 1, further comprising the step of trimming of tie bars between the leads of the leadframe before or after plating the leads.
3. The method as claimed in claims 1 or 2, wherein the plating is performed mask-less directly on the metal leadframe with the encapsulated die thereon.
- 15 4. The method as claimed in any one of the preceding claims, wherein the plating step comprises electro-plating of the metal leadframe substantially exactly from the periphery of a moulding encapsulation of the encapsulated die.
- 20 5. The method as claimed in claim 4, wherein an encapsulation material for the die is substantially non-conductive, and the coating is formed only on exposed areas of the leadframe substantially exactly from the periphery of the moulding encapsulation of the encapsulated die.
- 25 6. The method as claimed in any one of the preceding claims, wherein the step of plating the leads of the leadframe comprises forming the coating of Ni, Pd and Au on all exposed surfaces of the leads.
7. The method as claimed in any one of the preceding claims, wherein the step of
30 encapsulating the die comprises forming a moulding on top and bottom surfaces of the leadframe.
8. A semiconductor package comprising:
 a metal leadframe;

an encapsulated die mounted on the leadframe; and

a coating comprising Ni, Pd, and Au on the leads of the leadframe;

wherein the coating is formed substantially exactly from a periphery of a moulding encapsulation of the encapsulated die.

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9. The semiconductor device as claimed in claim 8, wherein the leads of the leadframe are coated with Ni, Pd, Au in areas where tie bars have been trimmed before the plating of the leads.

10 10. The semiconductor device as claimed in claim 9, wherein the leads are coated on all exposed surfaces thereof.

11. The semiconductor device as claimed in any one claims 8 to 10, wherein the moulding encapsulation comprises a moulding on top and bottom surfaces of the
15 leadframe.