predetermined number of cycles, and the reset frequency is compared with the reference clock related signal.

[0017] An input divider can be coupled to the reference clock input for dividing the reference clock signal to one of a plurality of preset dividing rates. An output divider can be coupled to the oscillator output for dividing the oscillator output signal to one of a plurality of preset dividing rates. Each of the dividers may have a control input for selecting a respected dividing rate.

[0018] The digital controlled oscillator comprises a plurality of decoder logic cells. A first group of the ~~logic delay~~ decoder cells provide a relatively large signal delay; a second group of ~~logic delay~~ decoder cells provide a relatively smaller delay. The basic delay cell of this ring oscillator comprise NAND gates, which can totally reset DCO in a very short pulse. Logic load elements, having control inputs, are included in the oscillator for fine adjustment of the oscillator output.

[0019] The digital ~~phase and frequency~~ detector comprises a control signal generator that can generate a plurality of binary control signals respectively output to the plurality of decoder logic cells of the oscillator. The control signal generator is responsive to the divided reference clock signal. A first comparator input is coupled to the input divider, a second comparator input is coupled to the counter, and the output of the comparator is coupled to the control signal generator. A first input of a shift generator is coupled to the input divider and a second input of the shift generator is coupled to the comparator output. The shift generator applies additional control signals to the oscillator. The shift generator may comprise a plurality of flip-flops connected in series, each flip-flop having an output coupled to a respective control input of the oscillator.

[0020] The digital phase and frequency detector further comprises an asynchronous cycle control generator having one input coupled to the oscillator output and another input coupled to the divided reference clock signal. The control signal generator binary output control signals are fixed to capture the frequency of the reference clock signal and the asynchronous cycle control generator is responsive to the phase of the oscillator output signal relative to the divided reference signal.

[0021] Initially, a binary search can be performed during comparison of the divided reference clock signal and oscillator feedback to determine the states of the various binary control signals for the decoder logic ~~delay~~ cells and logic load elements. These binary control signals adjust the frequency and phase of the oscillator output. Cycles of the oscillator output signal are counted, cycle count reset after a predetermined number of cycles. Comparison of the oscillator output with the divided reference clock signal is made at each reset count. A lock detector is responsive to the dividing rates of the input divider and output divider to generate a lock output signal. If a change in the dividing rates of either the input divider or output divider has been detected, an unlock generator will output a reset signal to reinitiate the binary search.

[0022] The PLL system, shown in block diagram in Fig. 1, receives a reference clock input signal "clkin" and produces an output signal "clkout." The PLL circuit comprises modules which are purely composed of logic components, with no capacitors, resistors, or other analog components. Divider 12 receives input clock signal "clkin" and divides its frequency by 2DR to produce an output clock signal "clk2r" having a duty cycle of 50%. In Fig. 1, the value of DR may vary between 1 to 15, as set by input DR. Output clock signal "clk2r" is coupled to an input of digital phase and frequency detector (DPFD) 14. DPFD 14

produces binary control signals that are received by digital controlled oscillator (DCO) 16. An optional output clock divider 18 can be used to receive DCO output signal “dco_out” and generate an output clock signal with a lower frequency. The output divider value can be set, for example, at 1, 2, 4, 8, by input DP. An input of counter 20 is coupled to the output of DCO 16. Output “clkf”of counter 20 is applied to DPFD 14. DCO output signal “dco_out” is also coupled to another input of DPFD 14. Divider 12 also generates an output enable DCO output signal “dco_out” signal “Dco_en” that is used to reset the DCO and counter(F) at the beginning of each clk2r cycle.

[0023] During operation, DPFD 14 will detect whether the DCO output clock frequency dco_out is higher or lower than expected by comparing the clk2r signal with a clkf output signal from counter 20. If the DCO output clock signal dco_out is not within an acceptable range, the DPFD 14 generates digital control signals c, asc and postc which are used to increase or decrease the DCO output clock frequency. Control signals c, asc and postc are in the form of binary numbers. In the exemplary embodiment of Fig. 1, c consists of 14 binary characters c[0] to c[13], asc consist of a single binary character while post c has six characters ~~postc0~~ postc[0] to ~~postc5~~ postc[5]. DCO: Digital Control Oscillator. A ring oscillator, by digitally changing the delay of the ring oscillator loop based on the values of c, asc and postc, the DCO output clock frequency can be adjusted.

[0024] When input signal “pll_en” turns high, the PLL system in Fig. 1 will start to oscillate. Divider 12 divides input clock signal clkin by 2DR to produce an output clock signal clk2r with a 50% duty cycle clock. Clock signal clk2r is fed to the DPFD 14. The dco_en signal generated by divider 12 is a very small pulse (for example, around 200ps) that

occurs just before the rising edge of clk2r. The dco_en signal is used to reset DCO 16 and Counter 20 at the beginning of every clk2r cycle.

[0025] The DCO output dco_out is a high frequency signal that is used as the clock of counter 20. Counter 20 will start to count from 0 at the beginning of every clk2r cycle. When the count arrives at DF[7:0], the counter's output clkf will turn high. DF[7:0] is an 8 character user defined binary number. As shown in Fig. 6, output signal dco_en from divider 12resets clkf to low at the rising edge of a clk2r clock cycle.

[0026] At each falling edge of "clk2r", DPFD 14 will detect whether clkf is high or low. If clkf is high, this means that the DCO output clock frequency is higher than expected. If clkf is low, this means that the DCO output clock frequency is lower than expected. If the DCO output clock frequency is higher or lower than expected, DPFD 14 will adjust the digital control bits c[13:0], asc, postc[5:0] accordingly, which will make the DCO output frequency change until, in a certain clk2r cycle, the clk2r falling edge and the clkf rising edge are perfectly matched. In that condition, the DCO output clock dco_out frequency will be equal to DF/DR times the frequency of clkin. The frequency of the output divider 18 clock "pll_clk" will be equal to (DF/DR)/ 2^{DP} times of the frequency of "clkin". The PLL output "clkout" is generated by multiplexer 22, A "bypass" signal is used ~~is used~~ to control multiplexer 22 to select whether the its pll_clk input or its clkin input is provided as the PLL output clkout signal.

[0027] Fig. 2 is a detailed schematic of a DCO 16 which may be used in the PLL circuit of Fig. 1. DCO 16 is a ring oscillator used to generate the frequency adjustable output clock. Although this DCO is completely composed of logic cells, it is designed to tune some of the transistor parameters. In general, the frequency of the DCO may be tuned by selecting the

[0032] The 6 AND cells ~~36~~ of the LDC and SDC decoders circled in Fig. 2 are used to switch off unused cells so as to avoid unnecessary power consumption when DCO is oscillating. These cells server to remove glitch and assure that the whole loop is not blocked upon start DCO oscillation. Two signals "dco_en_w" and "dco_en_n" will be generated by the AND cells 36 from dco_en. Signal dco_en_w as a pulse turns low ahead of dco_en_n and turns high behind dco_en_n. Signal dco_en_w is connected to NAND gate N1, while signal dco_en_n is connected to other NAND gates in the loop. Thus it output clock glitch can be removed to make sure when DCO starts to oscillate that the whole loop is not blocked.

[0033] Fig. 4 is a detailed schematic of a DPFD which may be used in the PLL circuit of Fig. 1. The DPFD receives input signals dco_out from the ~~16~~ DCO, clk2r from divider 12R, clkf from counter 20, and rstn. These signals are coupled to, or interact with, the following circuit modules in DPFD 14.

[0034] A plus_num generator 40 generates the signal plus_num[3:0] which helps to determine for every twelve dco_out cycles how many dco_out cycles asc is to be set at a 1'logic state. An asc generator 42 generates output signal "asc" for DCO 16. A c generator 44 generates output signal c[13:0] for DCO 16. A postc generator 46 generates output signal postc[5:0] for DCO 16. A ud generator 48 generates the signals uda and ud_postc, which are indicative of whether the DCO 16 is to oscillate faster or slower. A lock detector 50 detects whether the PLL is locked. An unlock detector 52 detect whether or not the PLL lock is lost.

[0035] The ud generator 48 module checks if clkf is high or low at each falling edge of the clk2r signal. If clkf is high, output signal uda from the ud generator 48 will be a logic '1' state, otherwise uda will be a logic '0' state. The uda signal is fed to the c generator 44, which

generates values for the c[13:0] binary output string based on the uda value at each clk2r cycle after pll_en is enabled (switched to high).

[0036] Operation is explained more particularly with respect to the data flow chart of Fig. 5 and the waveforms shown in Fig. 6. The c generator 44 uses a binary search to determine the values for c[13:0] and to achieve a fast lock. When binary search is initiated, c[13:0] and c_ready are both set to a logic state 0, at step 100 in Fig. 4. These states are illustrated in the waveform depiction of Fig. 5. At the next rising edge of clk2r, c[13] is set to logic state 1 at step 102. At the falling edge of clk2r, the uda generator 48 will update its value. Step 104 is a logic decision block for the value of uda. At the next rising edge of clk2r, if uda is at a logic state 1, signal c[13] is fixed to logic state 1. If not, c[13] is fixed to logic state 0 as step 106. At the same time, signal c[12] is set to logic state 1. Step 108 is a logic decision block to determine whether N is equal to zero, indicating that the search has progressed through all c signal settings. If not, N is decremented by 1 at step 110 and the data flow reverts to step 102. The steps are repeated to fix the value for c[12] and the remaining c[11:0] until c[0] is fixed as determined at step 108. At this point c_ready will be turned high by c generator 44 at step 112. From c[13] to c[0], each control pin has a different weight for adjusting the DCO output clock period, c[13] having the largest and c[0] the smallest. Step 114 is a logic decision block to determine whether the ~~PPL~~ PLL is locked for the values of c obtained in the binary search. If the system is not unlocked, the flow returns to step 108. If a determination is made that the system is unlocked, unlock detector 52 issues a reset signal to return the flow to step 100.

[0037] In theory, the weight of signal c[12] should be equal to 50% of signal c[13], the weight of signal c[11] should be equal to 50% of signal c[12], and so on, so that the weight of signal c[0] will be equal to $1/2^{13}$ that of c[13], around 0.012%. Extreme accuracy would

thereby be provided. However, considering that there may be process variations, temperature variations, and voltage variations, the actual ratio may not exactly equal to 50%. The ratio can be adjusted slightly higher to assure that such variations are not detrimental. The following table shows possible different weights for c[13] to c[0](unit: ps): c[13] - 640, c[12] - 321, c[11] - 185, c[10] - 94.7, c[9] - 49.3, c[8] - 29.3, c[7] - 18.4, c[6] - 11.2, c[5] - 7.86, c[4] - 5.66, c[3] - 4.14, c[2] - 2.69, c[1] - 2.13, c[0] - 1.41.

[0038] After the value of "c[13:0]" is fixed, a coarse capturing of the expected frequency is established. However, this frequency is still not sufficiently accurate and further tuning has to be done. Although the DCO can be designed such that changing the value of "c[0]" allows an adjustment of as small as 1.4ps to be applied to the DCO output clock cycle time, a 1.4ps tuning accuracy provided by the c control signal is still insufficient. This is because jitter is multiplied after passing through the feedback counter Counter(F) and can be accumulated to cause a jitter of 2*DF*1.4ps at the last dco_out cycle within a clk2r period. A jitter of 2*DF*1.4ps is quite significant.

[0039] To reduce or eliminate DCO output clock jitter, cycle control is effected in the following manner. When the PLL is locked, one period of clk2r T_{clk2r} is equal to 2*DF times of each dco_out period, T_{dco}. Assuming that c[0] switched off, that is, its associated DL0 shown in the Fig. 2 DCO is deactivated and does not load the DCO ring oscillator, the first 2*DF-1 dco_out cycles will each have a period of T_{dco}-1.4ps. Since dco_en sets dco_out to '0' at its falling edge and rising edge of clk2r ~~(see [1] od Fig. 7A~~, 2*DF cycles of dco_out will have to be fitted into one clk2r period. Therefore, the period of the last cycle of dco_out ~~denoted by the reference numeral "1"~~ will be

$$T_{lcd}=T_{clk2r} - (2*DF-1)(T_{dco}-1.4ps)$$

[0040] As shown in FIG. 7A, the period of this last dco_out cycle is longer compared to the other 2*DF-1 cycles before it and the difference can correspond to a jitter of 2*DF*1.4ps

$$T_{lcd} - (T_{dco}\text{-}1.4ps) = T_{clk2r} - (2*DF\text{-}1)(T_{dco}\text{-}1.4ps) - (T_{dco}\text{-}1.4ps)$$

$$= 2*DF* T_{dco} - (2*DF\text{-}1)(T_{dco}\text{-}1.4ps) - (T_{dco}\text{-}1.4ps)$$

$$= 2*DF*1.4ps$$

[0041] Similarly, if c[0] is switched on, an accumulated jitter of 2*DF*1.4ps will also be present in the last dco_out cycle but the period of this last cycle will be shorter compared to the other 2*DF-1 cycles before it. Since the load cell associated with c[0] is already very small in size, there is little room for accuracy improvement through device shrinkage and as such alternative methods of addressing the jitter method has to be deployed.

[0042] A new method, called cycle control, is used to reduce the DCO output clock jitter. In general terms, cycle control involves adjusting the "dco_out" time period of some cycles within a single clk2r time period in response to feedback from the "ud generator" as to whether the dco_out frequency is faster or slower than the target value. Therefore, unlike the c[13:0] control signals produced by the "c_generator" where the settings within a single clk2r cycle are not modified, the load settings applied to the DCO can be varied within a clk2r period by having the "asc" signal take on different values within a single clk2r cycle. This allows for greater precision in tuning the DCO to the required frequency.

[0043] The signal responsible for reducing the DCO output "~~lock~~ clock jitter is the output signal asc generated by the asc generator module 42 shown in Fig. 4. asc follows the clock of dco_out which has a higher frequency compared to the frequency of clk2r that c[13] to c[0] follow. In this way, multiple changes in the asc value may be made within one clk2r period. When asc is switched on , the period of each DCO output clock cycle will be increased by a

changes in value. The maximum jitter of dco_out happens at the last dco_out cycle of each clk2r period.

[0047] After the binary search, c[13:0] are fixed, ~~(i.e., locked)~~ the cycle control procedure is initiated. The module lock detector 50 will then detect whether the uda signal will toggle between logic states (0->1, or 1->0) at every clk2r cycle. If uda toggles to the opposite value for three continuous clk2r cycles, lock detector 52 will generate a logic high lock signal, which indicates that the PLL system is locked. If, thereafter, the reference input clock frequency, the input divider rate DR, or ~~the output divider rate DP~~ the counter number setting DF is changed, the module unlock detector 52 will detect whether the skew of clk2r and clkf is larger than the threshold delay. If so, a short positive pulse unlockt_rst will be generated to reset the PLL system. The lock signal returns to the low logic state, and the PLL system will restart the binary search procedure to again fix the c[13:0] signals. The system can again attain the locked state in a maximum of twenty five divided reference clock cycles (clk2r).

[0048] While the PPL system is in the locked state, the postc generator module 46 is operative to increase the input clock jitter tolerance. The function of the postc generator module is to increase the PLL's tolerance to input clock jitter by generating an binary output signal postc[5:0] which is fed into the DCO and used to make minor adjustments to the DCO frequency so that it can track the input clock frequency, clkin.

[0049] In the present described embodiment, postc[5:0] is a 6 digit binary string. As shown in the DCO schematic in Fig. 2, each digit in the postc[5:0] binary string is associated with a respective digital load DL0. A '0' value deactivates the associated load cell while a "1" value activates it. The value of the is changeable based on the value of the ud_postc[1:0] signal fed into the postc generator from the ud generator. The value of the

range with smaller jitter than existing ~~PPL~~ PLL arrangements. The ~~uses~~ binary search is used to achieve fastest lock. After the PLL is locked, a shift scan chain is used to trace the reference frequency change so as to get better input clock jitter tolerance. This PLL system uses NAND gates as the basic delay cells, which can totally disable and reset DCO in a very short time, thereby avoiding jitter accumulation to the next reference clock cycle. Stable DCO oscillation is provided. For example, in one example of the disclosed embodiment, the PLL can be been silicon validated using Global Foundries 65nmG process, the PPL uses only 5255um^2 (or 3% the a PLL chip area). DCO frequency could range in 900MHz~1.8GHz in all PVT corners. When DCO frequency at 1.8GHz, the working current is around 1.0mA using only one 1.0V power supply. This PLL could can be locked very fast in 50 divided reference clock cycle (5us @10MHz divided reference clock), and its output clock jitter is smaller than 40ps.

[0053] In this disclosure there are shown and described only preferred embodiments of the invention and but a few examples of its versatility. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein. For example, it is within contemplation that equivalent logic elements can be substituted for those described.

~~WHAT IS CLAIMED IS:~~

1. A phase locked loop control system comprising:

a reference clock input for receiving a reference clock signal;

a digital controlled oscillator configured to output an adjustable clock signal; and

a digital detector coupled between the reference clock input and an input of the controlled oscillator, the detector coupled to an output of the oscillator and configured for applying control signals to the oscillator for setting output operating signal frequency in accordance with detected frequency of the oscillator output clock signal;

wherein the phase of the output signal is selectively adjusted by the digital detector control signals during each input clock cycle.

2. A phase locked loop control system as recited in claim 1, further comprising:

an input divider coupled to the reference clock input for dividing the reference clock signal to one of a plurality of preset dividing rates; and

an output divider coupled to the oscillator output for dividing the oscillator output signal to one of a plurality of preset dividing rates.

3. A phase locked loop control system as recited in claim 2, wherein the input divider comprises a control input for selecting a dividing rate for the received reference clock signal and the output divider comprises a control input for selecting a dividing rate for the output signal.

4. A phase locked loop control system as recited in claim 2, wherein:

the digital detector comprises a control signal generator configured to generate a plurality of binary control signals respectively output at a plurality of control signal generator output terminals; and

the oscillator comprises a plurality of decoder logic cells having inputs respectively coupled to the control signal generator output terminals.

5. A phase locked loop control system as recited in claim 4, wherein the control signal generator is responsive to the divided reference clock signal.

6. A phase locked loop control system as recited in claim 4, further comprising a counter coupled to the oscillator output;

wherein the digital detector comprises a comparator having a first comparator input coupled to the input divider, a second comparator input coupled to the counter, and a comparator output coupled to the control signal generator.

7. A phase locked loop control system as recited in claim 6, wherein the digital detector further comprises a shift generator having a first input coupled to the input divider and a second input coupled to the comparator and an output coupled to the oscillator.

8. A phase locked loop control system as recited in claim 7, wherein the shift generator comprises a plurality of flip-flops connected in series, each flip-flop having an output coupled to a respective control input of the oscillator.

9. A phase locked loop control system as recited in claim 4, wherein the oscillator further comprises a first group of large delay cells and a second group of small delay cells.

10. A phase locked loop control system as recited in claim 9, wherein the DCO comprise NAND gates as its basic delay cell.

11. A phase locked loop control system as recited in claim 9, wherein the oscillator further comprises a plurality of logic load elements having inputs respectively connected to output terminals of the control signal generator;

wherein the logic elements are coupled to the detector for receiving the control signals for adjusting the phase of the output signal.

12. A phase locked loop control system as recited in claim 4, wherein the wherein the digital detector further comprises an asynchronous cycle control generator having an input coupled to the oscillator output signal;

wherein the control signal generator binary output control signals are fixed to capture the frequency of the reference clock signal and the asynchronous cycle control generator is responsive to the phase of the oscillator output signal relative to the divided reference signal.

13. A phase locked loop control system as recited in claim 12, wherein the digital detector further comprises a lock detector responsive to the dividing rates of the input divider and output divider to generate a lock output signal.

~~14. A phase locked loop control system as recited in claim 13, wherein the digital detector~~ further comprises an unlock generator for outputting a reset signal in response to the lock output signal if a change in the dividing rates of either the input divider or output divider has been detected by the lock detector.

15. A method for generating an output signal that is locked in frequency and phase with a reference clock signal, the method comprising:

coupling the reference clock signal to a digital ring oscillator to produce the output signal;

controlling a plurality of decoder logic cells in the ring oscillator to set the frequency of the output signal;

controlling a plurality of logic load cells in the ring oscillator during each reference clock cycle to adjust delay loading of the decoder logic cells to change the phase of the output signal accordingly.

16. A method as recited in claim 15, wherein the step of controlling the decoder logic cells comprises:

counting cycles of the output signals of the oscillator and comparing the signal of the oscillator at preset counted cycle intervals with the reference signal; and

generating a plurality of binary control signals in response to the comparing step.

17. A method as recited in claim 16, wherein the step of generating comprises applying a binary search with respect to each decoder logic cell.

18. A method as recited in claim 17, further comprising:

~~sensing a change in the frequency rate of the reference clock signal; and~~

resetting the binary search in response to the sensed change.

19. A method as recited in claim 15, wherein the step of controlling the plurality of logic load cells comprises changing the state of a binary asynchronous cycle control signal applied to the logic load cells during a determined percentage of reference clock cycle time.

20. A method as recited in claim 19, wherein the determined percentage is selectively preset.

WHAT IS CLAIMED IS:

1. A phase locked loop control system comprising:

a reference clock input for receiving a reference clock signal;

a digital controlled oscillator configured to output an adjustable clock signal;

a digital detector coupled between the reference clock input and an input of the controlled oscillator, the detector coupled to an output of the oscillator and configured for applying control signals to the oscillator for setting output operating signal frequency in accordance with detected frequency of the oscillator output clock signal; and

a counter coupled to the oscillator output; wherein:

the digital detector comprises a control signal generator configured to generate a plurality of binary control signals respectively output at a plurality of control signal generator output terminals, a comparator having a first comparator input coupled to the reference clock input, a second comparator input coupled to the counter, and a comparator output coupled to the control signal generator; and

the oscillator comprises a plurality of decoder logic cells having inputs respectively coupled to the control signal generator output terminals;

wherein the phase of the output signal is selectively adjusted by the digital detector control signals during each input clock cycle.

2. A phase locked loop control system as recited in claim 1, wherein the control signal generator is responsive to the divided reference clock signal.

3. A phase locked loop control system comprising:

a reference clock input for receiving a reference clock signal;

a digital controlled oscillator configured to output an adjustable clock signal;

an input divider coupled to the reference clock input for dividing the reference clock signal to one of a plurality of preset dividing rates; and

an output divider coupled to the oscillator output for dividing the oscillator output signal to one of a plurality of preset dividing rates; and

a digital detector coupled between the reference clock input and an input of the controlled oscillator, the detector coupled to an output of the oscillator and configured for applying control signals to the oscillator for setting output operating signal frequency in accordance with detected frequency of the oscillator output clock signal;

wherein the phase of the output signal is selectively adjusted by the digital detector control signals during each input clock cycle;

the digital detector comprises a control signal generator configured to generate a plurality of binary control signals respectively output at a plurality of control signal generator output terminals; and

the oscillator comprises a plurality of decoder logic cells having inputs respectively coupled to the control signal generator output terminals;

and further comprising a counter coupled to the oscillator output;

wherein the digital detector comprises a comparator having a first comparator input coupled to the input divider, a second comparator input coupled to the counter, and a comparator output coupled to the control signal generator.

4. A phase locked loop control system as recited in claim 3, wherein the input divider comprises a control input for selecting a dividing rate for the received reference clock signal and the output divider comprises a control input for selecting a dividing rate for the output signal.

5. A phase locked loop control system as recited in claim 3, wherein the digital detector further comprises a shift generator having a first input coupled to the input divider and a second input coupled to the comparator and an output coupled to the oscillator.

6. A phase locked loop control system as recited in claim 5, wherein the shift generator comprises a plurality of flip-flops connected in series, each flip-flop having an output coupled to a respective control input of the oscillator.

7. A phase locked loop control system comprising:

a reference clock input for receiving a reference clock signal;

a digital controlled oscillator configured to output an adjustable clock signal;

an input divider coupled to the reference clock input for dividing the reference clock signal to one of a plurality of preset dividing rates; and

an output divider coupled to the oscillator output for dividing the oscillator output signal to one of a plurality of preset dividing rates; and

a digital detector coupled between the reference clock input and an input of the controlled oscillator, the detector coupled to an output of the oscillator and configured for applying control signals to the oscillator for setting output operating signal frequency in accordance with detected frequency of the oscillator output clock signal;

wherein the phase of the output signal is selectively adjusted by the digital detector control signals during each input clock cycle;

the digital detector comprises a control signal generator configured to generate a plurality of binary control signals respectively output at a plurality of control signal generator output terminals; and

the oscillator comprises a plurality of decoder logic cells having inputs respectively coupled to the control signal generator output terminals;

and wherein the plurality of decoder logic cells comprises a first group of large delay cells and a second decoder group of small delay cells.

8. A phase locked loop control system as recited in claim 7, wherein the DCO comprise NAND gates as its basic delay cell.

9. A phase locked loop control system as recited in claim 7, wherein the oscillator further comprises a plurality of logic load elements having inputs respectively connected to output terminals of the control signal generator;

wherein the logic elements are coupled to the detector for receiving the control signals for adjusting the phase of the output signal.

10. A phase locked loop control system comprising:

a reference clock input for receiving a reference clock signal;

a digital controlled oscillator configured to output an adjustable clock signal;

an input divider coupled to the reference clock input for dividing the reference clock signal to one of a plurality of preset dividing rates; and

an output divider coupled to the oscillator output for dividing the oscillator output signal to one of a plurality of preset dividing rates; and

a digital detector coupled between the reference clock input and an input of the controlled oscillator, the detector coupled to an output of the oscillator and configured for applying control signals to the oscillator for setting output operating signal frequency in accordance with detected frequency of the oscillator output clock signal;

wherein the phase of the output signal is selectively adjusted by the digital detector control signals during each input clock cycle;

the digital detector comprises a control signal generator configured to generate a plurality of binary control signals respectively output at a plurality of control signal generator output terminals; and

the oscillator comprises a plurality of decoder logic cells having inputs respectively coupled to the control signal generator output terminals;

and wherein the wherein the digital detector further comprises an asynchronous cycle control generator having an input coupled to the oscillator output signal; and

wherein the control signal generator binary output control signals are fixed to capture the frequency of the reference clock signal and the asynchronous cycle control generator is responsive to the phase of the oscillator output signal relative to the divided reference signal.

11. A phase locked loop control system as recited in claim 10, wherein the digital detector further comprises a lock detector responsive to the dividing rates of the input divider and output divider to generate a lock output signal.

12. A phase locked loop control system as recited in claim 11, wherein the digital detector further comprises an unlock generator for outputting a reset signal in response to the lock output signal if a change in the dividing rates of either the input divider or output divider has been detected by the lock detector.