Description

Title of Invention: MULTILAYER WIRING BOARD, AND METHOD FOR MANUFACTURING MULTILAYER WIRING BOARD

Technical Field

[0001]

The present invention is related to a multilayer wiring board and a method for manufacturing a multilayer wiring board.

Background Art

[0002]

In recent years, a technique used for three-dimensionally mounting semiconductor elements employs a packaging substrate in which circuit boards are stacked. In such a packaging substrate, a through electrode may be formed in the circuit boards. The through electrode is formed by forming a through hole in a substrate configured with an insulating body and disposing a conductor in the through hole. As circuit boards become more and more highly integrated, there is also a demand for further miniaturizing such a through hole.

[0003]

Generally speaking, ceramics or resin may be selected as a material for such a packaging substrate. However, because ceramic substrates have a high resistance value or high permittivity, it is not easy to install thereon a semiconductor element having a radio frequency. In contrast, although resin substrates are relatively suitable for a semiconductor element having a radio frequency, there is a limit to reducing pitch widths of wirings.

[0004]

In recent years, studies are underway regarding application of silicon or glass to high-end packaging substrates. By forming a through hole in a silicon or glass substrate and injecting a conductive substance into the through hole, it is possible to keep short the length of a wiring between a device and a mother board and to thus achieve excellent electric characteristics. Examples of the studies regarding packaging substrates include Patent Literature 1 to 3 listed below.

[0005]

Patent Literature 1 addresses the problem of strengthening a power source for a wiring board and discloses the following as a wiring board and a method for manufacturing a wiring board.

"A wiring board 1 of an embodiment comprises: a core substrate 10; a first build-up layer 11 formed by alternately stacking a first inter-layer insulating layer 32 and a first conductor layer 31; and a second build-up layer 12 formed by alternately stacking a second inter-layer insulating layer 42 and a second conductor layer 41. Among the first conductor layers 31 and the second conductor layers 41, regarding

conductor layers positioned on the same sequential rank from the core substrate 10, the area and the thickness of the conductor layer in the second build-up layer 12 is larger than the area and the thickness of the conductor layer in the first build-up layer 11".

Patent Literature 2 addresses the problem of providing a printed wiring board capable of improving mountability of a plurality of electronic component parts to be mounted on the printed wiring board via solder and discloses the following as a printed wiring board and a semiconductor apparatus including the same.

"Formed on a surface of a printed wiring board 1A are a plurality of first conductor pads 51 and 52 connected by top surfaces 51a and 52a thereof to a first electronic component part 7 via solder 70 and a plurality of second conductor pads 61 and 62 connected by top surfaces 61a and 62a thereof to a second electronic component part 8 via solder 80. The top surfaces 51a and 52a of the first conductor pads 51 and 52 have the same shape and the same size as the top surfaces 61a and 62a of the second conductor pads 61 and 62. The top surfaces 51a and 52a of the first conductor pads 51 and 52 and the top surfaces 61a and 62a of the second conductor pads 61 and 62 are formed on mutually the same plane F3".

Patent Literature 3 discloses the following as a semiconductor packaging glass substrate, a semiconductor packaging substrate, and a semiconductor apparatus.

"A semiconductor packaging glass substrate comprises: a glass substrate having a first surface and a second substrate that are opposite each other; and a large number of core vias penetrating the glass substrate in the thickness direction. A plain line is a straight line connecting together locations where no core via is formed on the first surface of the glass substrate. A via line is a straight line connecting together locations where the core vias are formed on the first surface of the glass substrate. The semiconductor packaging glass substrate has a stress difference value (P) equal to or smaller than 1.5 MPa, as calculated by using Formula (1) presented below.

Formula (1): $P = Vp - Np$

In Formula (1), P denotes the stress difference value measured on the same glass substrate. Vp denotes the difference between a maximum value and a minimum value of the stress measured on the via line. Np denotes the difference between a maximum value and a minimum value of the stress measured on the plain line".

Citation List

Patent Literature

[0006]

Patent Literature 1: Japanese Patent Publication No. 7288339

Patent Literature 2: Japanese Patent Laid-Open Publication No. 2016-66745

Patent Literature 3: Japanese Patent Publication No. 7087205

Summary of Invention

Technical Problem

[0007]

In the packaged substrates disclosed in Patent Literature 1 and 2, a glass epoxy substrate is expected to be used as a core material. However, Patent Literature 1 and 2 do not discuss a high-end packaged substrate, i.e., a large-area packaged substrate in which a plurality of semiconductor elements are installed via a silicon interposer. High-end packaged substrates in recent years have the problem of warping of the packaged substrates, because a plurality of semiconductor elements are installed via a silicon interposer and, at the time of joining to the packaged substrate, the silicon interposer and the packaged substrate have mutually-different linear expansion coefficients, and because an elastic modulus upper limit of glass epoxy substrates is 40 GPa. To prevent joint defects caused by such warping of packaged substrates, there is a demand for a package using glass, which has similar physical property values to silicon.

[0008]

Further, although Patent Literature 3 shows an example of a packaged substrate using glass, glass is a fragile material. It has been confirmed that, when the same design concept and steps as those of a glass epoxy substrate are applied to a glass substrate, the glass may be cracked in the vicinity of a wiring layer due to stress caused by the difference in linear expansion coefficients between the material used for the wiring layer and the glass; and further, when the glass substrate is divided into pieces by using the same step (called blade dicing) as that used for a glass epoxy substrate, a phenomenon may occur in which the glass is broken because stress gets concentrated at microcracks occurring on end faces of the divided pieces. For this reason, when a glass substrate is used in a packaged substrate, problems regarding reliability still remain.

Further, as for packaged substrates using a ceramic material, it is difficult to perform dicing processing in the state in which wiring layers are stacked. As a result, a problem remains with dividing a multilayer wiring board using a ceramic material into pieces.

[0009]

In view of the circumstances described above, an object of the present invention is to provide a multilayer wiring board of which it is possible to prevent warping and which has high reliability, and a method for manufacturing the multilayer wiring board.

Solution to Problem

[0010]

To solve the problems described above, one of the representative multilayer wiring boards of the present invention includes: an inorganic substrate which has a first surface, a second surface opposite the first surface, and a lateral face connecting a peripheral edge portion of the first surface to a peripheral edge portion

of the second surface, and which has formed therein at least one through hole penetrating from the first surface to the second surface; a protection resin portion disposed in the through hole of the inorganic substrate and disposed so as to cover the lateral face of the inorganic substrate; and a through electrode which includes a conductor portion extending inside the through hole and establishes an electric connection between the first surface and the second surface.
[0011]

Further, one of the representative methods for manufacturing a multilayer wiring boards of the present invention includes: a first step of dividing a base substrate into pieces and forming inorganic substrates each of which has a first surface, a second surface opposite the first surface, and a lateral face connecting a peripheral edge portion of the first surface to a peripheral edge portion of the second surface, the inorganic substrates each having formed therein at least one through hole penetrating from the first surface to the second surface; a second step of arranging the inorganic substrates on a glass epoxy substrate resulting from a window opening process, disposing a resin material on the first surface, the second surface, and the lateral face and in the through hole of the inorganic substrate, forming a first surface first layer on the first surface, and forming a second surface first layer on the second surface; a third step of using a laser inside the through hole and forming a sub through hole being a through hole formed in the resin material; a fourth step of disposing a conductor portion in the sub through hole, the first surface first layer, and the second surface first layer; a fifth step of forming, on the first surface side, at least two wiring layers in addition to the first surface first layer and forming, on the second surface side, at least two wiring layers in addition to the second surface first layer; and a sixth step of obtaining divided pieces by performing dicing processing using blade dicing between the inorganic substrates arranged on the glass epoxy substrate.

Advantageous Effects of Invention

[0012]

According to the present invention, it is possible to provide a multilayer wiring board of which it is possible to prevent warping and which has high reliability, and a method for manufacturing the multilayer wiring board. Other problems, configurations, and advantageous effects besides those described above will become clear from the following Description of Embodiments.

Brief Description of Drawings

[0013]

[FIG. 1] FIG. 1 is a cross-sectional view showing an example of a multilayer wiring board according to an embodiment of the present invention.
[FIG. 2] FIG. 2 is a cross-sectional view showing an example of a semiconductor apparatus including the multilayer wiring board.

[FIG. 3] FIG. 3 is a drawing showing a modification example of the multilayer wiring board according to the embodiment of the present invention.
[FIG. 4] FIG. 4 is a drawing showing a step of preparing a base substrate.
[FIG. 5] FIG. 5 is a drawing showing a step of forming through holes in the base substrate.
[FIG. 6] FIG. 6 is a cross-sectional view showing, in enlargement, one of the through holes formed in the base substrate.
[FIG. 7] FIG. 7 is a cross-sectional view showing, in enlargement, another example of the through hole formed in the base substrate.
[FIG. 8] FIG. 8 is a drawing showing a step of arranging inorganic substrates obtained as divided pieces, on a glass epoxy substrate resulting from a window opening process.
[FIG. 9] FIG. 9 is a drawing showing a step of stacking a resin material on a glass epoxy substrate.
[FIG. 10] FIG. 10 is a cross-sectional view of a state arrived at by arranging inorganic substrates 10 on a glass epoxy substrate resulting from a window opening process and subsequently injecting a resin material.
[FIG. 11] FIG. 11 is a drawing showing a step (a third step) of forming a sub through hole, which is a through hole formed in the resin material, by using a laser inside the through hole.
[FIG. 12] FIG. 12 is a cross-sectional view showing an example of a processing shape of the sub through hole.
[FIG. 13] FIG. 13 is a drawing showing a step (a fourth step) of disposing a conductor on the sub through holes, a first surface first layer, and a second surface first layer.
[FIG. 14] FIG. 14 is a drawing showing a step (a fifth step) of forming, on the first surface side, at least two wiring layers in addition to the first surface first layer and forming, on the second surface side, at least two wiring layers in addition to the second surface first layer.
[FIG. 15] FIG. 15 is a drawing schematically showing a glass epoxy substrate and alignment marks used for dicing processing.
[FIG. 16] FIG. 16 is a cross-sectional view showing a multilayer wiring board in Comparison Example 1.
[FIG. 17] FIG. 17 is a cross-sectional view showing a multilayer wiring board in Comparison Example 2.

Description of Embodiments
[0014]

Embodiments of the present invention will be explained below, with reference to the drawings. The embodiments and the examples described below are examples of embodiments of the present invention. Thus, interpretation of the present invention is not to be limited by those embodiments and examples.

In the drawings referenced in the embodiments of the present invention, some of the elements that are the same as each other will be referred to by using the same reference signs or similar reference signs (numerals simply followed by A, B, and so on), and duplicate explanations thereof may be omitted. Further, for the convenience in explanations and references, the description of dimensions and proportions of the drawings may be different from those in actuality or may be omitted from certain parts of the configurations.

[0015]

Also, to facilitate comprehension of the invention, the positions, sizes, shapes, ranges, and the like of the constituent elements depicted in the drawings may not necessarily represent the positions, sizes, shapes, ranges, and the like in actuality. For this reason, the present invention is not necessarily limited by the positions, sizes, shapes, ranges, and the like disclosed in the drawings.

[0016]

In the present disclosure, the term "surface" may denote not only a surface of a plate-like member, but also, with regard to any layer included in a plate-like member, an interface of the layer substantially parallel to a surface of a plate-like member. Further, the terms "top surface" and "bottom surface" denote surfaces depicted at the top and the bottom in the drawings, when a plate-like member or a layer included in a plate-like member is depicted. It should be noted that the "top surface" and the "bottom surface" may also be referred to as a "first surface" and a "second surface".

[0017]

Further, the term "a lateral face" denotes a face or a part corresponding to the thickness of a plate-like member or a layer included in a plate-like member. Furthermore, a part of a surface and a lateral face may collectively be referred to as an "end portion".

The phrase "a lateral face of a through hole" denotes, regarding a through hole provided in an object, an interface of the object forming the through hole.

The term "above" denotes the direction perpendicularly upward when a plate-like member or a layer is placed horizontally. Further, "above" and "below" being opposite thereof may be referred to as a "Z axis positive direction" and a "Z axis negative direction". For horizontal directions, the terms "X axis direction" and "Y axis direction" may be used.

[0018]

In addition, a distance in a Z axis direction will be referred to as a "height". A distance on an XY plane defined by the X axis direction and the Y axis direction will be referred to as a "width". Further, the height of an object in the form of a layer may be referred to as a "thickness".

Furthermore, a "through electrode 15" denotes a conductive path provided for making electric conductivity between the first surface and the second surface of a glass substrate when the glass substrate is used as a part of a multilayer wiring

board 1. It is not necessarily requisite that the glass substrate is completely penetrated by a single conductive material. Examples of the through electrode 15 include any configuration in which a conductive channel from the first surface is connected to a conductive channel from the second surface. Further, possible modes of the through electrode 15 include both a filled structure in which a through hole is filled with a conductive material and a conformal structure in which only the lateral wall part of a through hole is covered by a conductive material.
[0019]

Also, the terms "planar shape" and "planar view" refer to a shape observed as a surface or a layer is viewed from above. Further, the terms "cross-sectional shape" and "cross-sectional view" refer to a shape as viewed from a horizontal direction when a plate-like member or a layer has been sectioned in a specific direction.

In addition, the term "center portion" refers to a portion at the center that is not a peripheral portion of a surface or a layer. Also, the term "center direction" refers to a direction from a peripheral portion of a surface or a layer toward the center of the planar shape of the surface or the layer.
[0020]

Further, as for numerical ranges, for example, the phrase "a range of 3 to 10 ppm/°C" denotes the range equal to or greater than 3 ppm/°C and equal to or lower than 10 ppm/°C. This also applies to other numerical ranges.
[0021]

<Embodiments of the present invention>

(A structure of a multilayer wiring board)

FIG. 1 is a cross-sectional view showing an example of the multilayer wiring board 1 according to an embodiment of the present invention. FIG. 2 is a cross-sectional view showing an example of a semiconductor apparatus 200 including the multilayer wiring board 1.
[0022]

As shown in FIG. 1, the multilayer wiring board 1 according to the embodiment of the present invention includes: an inorganic substrate 10 which has a first surface 10a, a second surface 10b opposite the first surface 10a, and lateral faces 10c each connecting a peripheral edge portion of the first surface 10a to a peripheral edge portion of the second surface 10b, and which has formed therein at least one through hole 11 penetrating from the first surface 10a to the second surface 10b; a protection resin portion 25 disposed in the through hole 11 of the inorganic substrate 10 and disposed so as to cover the lateral faces 10c of the inorganic substrate 10; and through electrodes 15 each of which includes a conductor portion extending inside the through hole 11 and establishes an electric connection between the first surface 10a and the second surface 10b. The length of the multilayer wiring board 1 will be expressed as L.
[0023]

(A configuration of the inorganic substrate 10)

The first surface 10a of the inorganic substrate 10 is a surface that extends in a direction parallel to the XY plane and is positioned at the Z axis positive direction. The second surface 10b of the inorganic substrate 10 is a surface that extends in a direction parallel to the XY plane and is positioned at the Z axis negative direction. Further, the lateral faces 10c of the inorganic substrate 10 are each a surface connecting a peripheral edge portion of the first surface 10a to a peripheral edge portion of the second surface 10b. In the cross-sectional views in FIG. 1 and FIG. 2, of the inorganic substrate 10, the lateral faces 10c correspond to the surfaces that are positioned on two end sides in the X axis direction, while extending in the Z axis direction. Although FIG. 1 and FIG. 2 depict an example in which the inorganic substrate 10 has eight through holes 11 and eight through electrodes 15 formed, the numbers of the through holes 11 and the through electrodes 15 are not limited to those depicted in the drawings. Depending on how a cross-section is taken, positional arrangements of the through holes 11 and the through electrodes 15 may vary. Further, generally speaking, when viewed from the Z axis direction, the multilayer wiring board 1 and the semiconductor apparatus 200 each have a square or rectangular shape.

[0024]

The inorganic substrate 10 is configured from glass or a ceramic material. The material being used is a composite material containing at least one selected from among: quartz, alkali-free glass, alkali glass, Al_2O_3, SiO_2, CaO, MgO, SrO, BaO, ZrO_2, and so on. As for primary physical property values of the inorganic substrate 10, it is possible to configure a composition ratio thereof as appropriate, as long as the linear expansion coefficient thereof falls in the range of 3 to 10 ppm/°C, and the elastic modulus thereof is equal to or greater than 40 GPa, and preferably, approximately 60 GPa. Further, the thickness of the inorganic substrate 10 will be expressed as T1. Because the inorganic substrate 10 structures a part being a foundation of the multilayer wiring board 1, the inorganic substrate 10 may be referred to as a "core substrate".

[0025]

(A configuration of the through electrodes)

In each of the through holes 11, a conductor portion is covered by the protection resin portion 25. A conductor portion of each of the through electrodes 15 is provided for the purpose of electrically connecting together the first surface 10a and the second surface 10b of the inorganic substrate 10 and is configured by using at least one type of metal material. Representative examples of the metal material include Cu, Ni, Al, Ti, Cr, Mo, W, Ta, Au, Ir, Ru, Pd, Pt, AlSi, AlSiCu, AlCu, NiFe, ITO, IZO, AZO, ZnO, PZT, TiN, and Cu_3N_4. It is possible to use any single material or a combination of two or more materials selected from among these. The conductor portion is formed by implementing an electrolytic plating method, after a seed layer is formed by implementing electroless plating, a sputtering method, or the like.

In this situation, it is desirable that the conductor portion has a linear expansion coefficient in the range equal to or greater than the expansion coefficient of the inorganic substrate 10 and equal to or smaller than the expansion coefficient of the insulating resin portion 25 and preferably in the range of 11 to 18 ppm/°C. Within the abovementioned range, it is possible to configure the linear expansion coefficient of the conductor layer as appropriate.

[0026]

The structure of the conductor portions of the through electrodes 15 may be selected from between a filled structure in which a conductor material is injected into the through hole 11 and a conformal structure in which the conductor material is formed only on the wall surface part of the through hole 11, or the like. From between the filled and the conformal structures, it is possible to select a structure as appropriate, in accordance with an operation frequency, a resistance value, impedance matching, or the like of the semiconductor apparatus 200 including the multilayer wiring board 1.

[0027]

In each of the through holes 11 in the inorganic substrate 10, the thickness d1 of the protection resin portion 25 disposed between the inorganic substrate 10 and the conductor portion is at least 10 μm. If the thickness of the protection resin portion 25 were equal to or smaller than 10 μm, there would be a possibility that the protection resin portion 25 might be damaged and that the advantageous effect of protecting the lateral faces of the inorganic substrate 10 might be lost, at the time of forming through holes 12 in the protection resin portions 25 injected in the through holes 11, as explained later. In addition, if the conductor portion were to be disposed in a through hole 12 while the protection resin portion 25 is damaged, it would be difficult to guarantee close contact between the conductor portion and the protection resin portion 25. Further, in the state in which the protection resin portion 25 is damaged, because electric characteristics would change, it would be difficult to achieve desired electric characteristics (transfer characteristics) of the multilayer wiring board 1. For these reasons, it is necessary to configure the thickness d1 of the protection resin portion 25 provided between each of the through holes 11 of the inorganic substrate 10 and the conductor portion to be at least 10 μm. Although the through holes 11 and the through electrodes 15 are depicted in FIG. 1 and FIG. 2 to be rectangular, details of the shapes will be explained later. The thickness d1 is the dimension at a location where the distance between the through electrode 15 and the through hole 11 is the shortest.

[0028]

(Configurations of a first surface layer structure 21 and a second surface layer structure 22)

The multilayer wiring board 1 further includes a first surface layer structure 21 formed on the first surface 10a of the inorganic substrate 10 and a second surface layer structure 22 formed on the second surface 10b of the inorganic substrate 10.

Each of the first surface layer structure 21 and the second surface layer structure 22 has two or more wiring layers. A first surface first layer 21a included in the first surface layer structure 21 and formed on the inorganic substrate 10 and a second surface first layer 22a included in the second surface layer structure 22 and formed on the inorganic substrate 10 have no metal wiring. One or more wiring layers included in the first surface layer structure 21 and excluding the first surface first layer 21a and one or more wiring layers included in the second surface layer structure 22 and excluding the second surface first layer 22a have metal wirings formed therein.

More specifically, as the wiring layers, the first surface layer structure 21 includes six wiring layers, namely the first surface first layer 21a to a first surface sixth layer 21f, and an outermost layer 21g including a solder resist layer 40. The first surface first layer 21a is disposed on the first surface 21a of the inorganic substrate 10 and has a layer structure formed by the protection resin portion 25. Although the first surface first layer 21a has locations penetrated by the through electrodes 15, the protection resin portion 25 is provided in locations covering the inorganic substrate 10 and the through holes 11. The first surface second layer 21b is disposed on the first surface first layer 21a and has a layer structure which includes metal wirings 21b1 and 21b2 and in which the protection resin portion 25 has been injected. As viewed from the Z axis direction, the metal wirings 21b1 and 21b2 have predetermined wiring patterns. Disposed between the metal wiring 21b1 and the metal wiring 21b2 is a filled-type through electrode extending in the Z axis direction.

Further, the first surface third layer 21c is disposed on the first surface second layer 21b and has a layer structure which includes a metal wiring 21c1 and in which the protection resin portion 25 has been injected. As viewed from the Z axis direction, the metal wiring 21c1 has a predetermined wiring pattern. Disposed between a metal wiring 21c1 and the metal wiring 21b2 in the first surface second layer 21b is a filled-type electrode extending in the Z axis direction.

Similarly, the first surface fourth layer 21d has a layer structure including a metal wiring 21d1, the protection resin portion 25, and a filled-type electrode. The first surface fifth layer 21e has a layer structure including a metal wiring 21e1, the protection resin portion 25, and a filled-type electrode. The first surface sixth layer 21f has a layer structure including a metal wiring 21f1, the protection resin portion 25, and a filled-type electrode.

On the outermost layer 21g being the layer positioned outermost on the first surface 10a side, the solder resist layer 40 and solder bumps 50 are formed.
[0029]

The second surface layer structure 22 has a structure similar to that of the first surface layer structure 21. More specifically, as the wiring layers, the second surface layer structure 22 includes six wiring layers, namely the second surface first layer 22a to a second surface sixth layer 22f, and a solder resist layer 40. Of the six

wiring layers, the second surface first layer 22a is disposed on the second surface 10b of the inorganic substrate 10 and has a layer structure formed by the protection resin portion 25. The second surface second layer 22b has a layer structure including a metal wiring 22b1, a metal wiring 22b2, the protection resin portion 25, and a filled-type electrode. The second surface third layer 22c has a layer structure including a metal wiring 22c1, the protection resin portion 25, and a filled-type electrode. The second surface fourth layer 22d has a layer structure including a metal wiring 22d1, the protection resin portion 25, and a filled-type electrode. The second surface fifth layer 22e has a layer structure including a metal wiring 22e1, the protection resin portion 25, and a filled-type electrode. The second surface sixth layer 22f has a layer structure including a metal wiring 22f1, the protection resin portion 25, and a filled-type electrode. On the outermost layer 22g positioned on the second surface 10b side, the solder resist layer 40 is formed.

[0030]

(An advantageous effect of having no metal wiring in the wiring layers on the inorganic substrate 10)

If a metal wiring were formed on the inorganic substrate 10, the inorganic substrate 10 would be cracked at an end portion of the wiring, because stress from stacked members in the first surface layer structure 21 and the second surface layer structure 22 would be concentrated at the end portion of the metal wiring. Among the wiring layers in the first surface layer structure 21 and the second surface layer structure 22, by providing no metal wiring in the first layers on the inorganic substrate 10, and providing the metal wirings starting with the second layers, it is possible to mitigate the stress of the wiring layers, and it is therefore possible to prevent the inorganic substrate 10 from being cracked.

[0031]

(A configuration of the protection resin portion 25)

The protection resin portion 25 covers the first surface 10a and the second surface 10b of the inorganic substrate 10, the lateral faces of the through holes 11, and the lateral faces 10c of the inorganic substrate 10 and also serves as a constituent element of the wiring layers formed on the first surface 10a and the second surface 10b. In other words, the resin material injected in the through holes 11 and covering the lateral faces of the inorganic substrate 10 is the same as the resin material included in the wiring layers. Further, the resin material contains a filler mixed in to satisfy the range of 40 wt% to 80 wt% inclusive and having an average particle diameter in the range of 0.3 μm to 1.0 μm inclusive. Further, within the abovementioned material range, the resin material may contain a build-up resin or glass cloth.

[0032]

As for the resin material, if the content amount of the filler included in the resin material were less than 40 wt%, there would be a possibility that an inorganic material might be cracked due to stress caused by a difference in the linear

expansion coefficients of the inorganic materials such as the metal wirings and the through electrodes 15, since the resin material would have a linear expansion coefficient of 40 ppm/Deg. C or higher and an elastic modulus of 5 MPa or lower. Further, when the content amount of the filler were 80 wt% or more, an inter-layer delamination would be more likely to occur between the resin material and the inorganic materials due to an increase in the contact area between the filler and the inorganic materials. Within the range of 40 wt% to 80 wt% inclusive, it is possible to configure the content amount of the filler included in the resin material as appropriate, in accordance with the numbers of the wiring layers on the first surface 10a and the second surface 10b of the multilayer wiring board 1.

[0033]

For example, as the protection resin portion 25, it is possible to use a material obtained by adding a filler such as silica, titanium oxide, aluminum oxide, magnesium oxide, zinc oxide, or the like to a resin having mixed therein at least one selected from among epoxy resin, urethane resin, silicon resin, polyester resin, oxetane resin, and polyamide resin. By configuring the protection resin portion 25 to have an elastic modulus in the range of 6 GPa to 15 GPa and a linear expansion coefficient in the range of 11 to 30 ppm/Deg. C, it is possible to mitigate the stress to be imposed on the inorganic substrate 10.

[0034]

The thickness d2 of the protection resin portion 25 disposed on the lateral faces 10c of the inorganic substrate 10 is at least 50 μm. The thickness d2 denotes the dimension of the protection resin portion 25 measured in the direction perpendicular (the x axis direction in the drawing) to a lateral face 10c of the inorganic substrate 10. The protection resin portion 25 disposed on the lateral faces 10c has a function of mitigating the stress to be imposed on the inorganic substrate 10 and is formed by using the same resin material as used for the first surface first layer 21a disposed on the first surface 10a and the second surface first layer 22a disposed on the second surface 10b. If the thickness of the protection resin portion 25 formed on the lateral faces 10c of the inorganic substrate 10 were 50 μm or less, it would be difficult to sufficiently mitigate the stress from the wiring layers on the first surface 10a and the second surface 10b, and the inorganic substrate 10 might be damaged by the stress. Accordingly, it is desirable to configure the thickness of the protection resin portion 25 on the lateral faces 10c of the inorganic substrate 10 to be at least 50 μm.

[0035]

(A configuration of the multilayer wiring board 1)

An outer periphery portion of the multilayer wiring board 1 is covered by the insulating resin portion 25 and an outer periphery protection portion 30 and is structured in such a manner that, after the multilayer wiring board 1 is divided into pieces at a manufacturing stage as explained later, the inorganic substrates 10 are not exposed from the lateral faces of the multilayer wiring board 1. In this situation,

the outer periphery portion denotes a part in the xy plane direction. Also, as explained later, the outer periphery protection portion 30 is obtained by separating a certain part from a glass epoxy substrate. Although the lateral faces 10c of the inorganic substrate 10 are provided with the insulating resin portion 25 of at least 50 μm, if only the protection resin portion 25 were provided, the multilayer wiring board 1 would have a deformation (warping/undulation) due to a thermal history from the time when a semiconductor element 100 was joined to the multilayer wiring board 1. By providing the outer periphery protection portion 30 in the outer periphery portion of the multilayer wiring board 1, it is possible to prevent the deformation that may be caused by the thermal history from the time when the multilayer wiring board 1 and the semiconductor element 100 were joined together. As long as the protection resin portion 25 is formed on the lateral faces 10c of the inorganic substrate 10 with a thickness of 50 μm or larger, it is possible to arbitrarily configure the position to dispose the outer periphery protection portion 30 as appropriate, in accordance with the thickness and the size of the multilayer wiring board 1.

Further, by providing the outer periphery portion of the multilayer wiring board 1 with the outer periphery protection portion 30, it is possible to prevent the inorganic substrate 10 from being exposed from the end faces of the multilayer wiring board 1 and it is therefore possible to ensure reliability of the multilayer wiring board 1.

[0036]

(A utilization example of the multilayer wiring board 1)

Further, as shown in FIG. 2, in the semiconductor apparatus 200, at least one semiconductor element 100 is installed on the multilayer wiring board 1 via an interposer substrate. More specifically, the semiconductor element 100 is connected to the multilayer wiring board 1 via a silicon interposer 90 structured with silicon, for example, for the purpose of carrying out a signal transfer between the multilayer wiring board 1 and the semiconductor element 100. The solder bumps 50 in FIG. 1 are connected to an electrode of the semiconductor element 100 via the silicon interposer 90, as shown in FIG. 2. The silicon interposer 90 includes a fine wiring layer and establishes a connection between the semiconductor element 100 and the multilayer wiring board 1. For the connection between the semiconductor element 100 and the silicon interposer 90 and the connection between the silicon interposer 90 and the multilayer wiring board 1, solder configured with Sn, SnAg, Ni/Sn, Ni/SnAg, Ni/Cu/Sn, Ni/Cu/SnAg, or the like is used.

[0037]

(A modification example of the multilayer wiring board)

Next, a modification example of the embodiment of the present invention shown in FIG. 3 will be explained. FIG. 3 is a drawing showing the modification example of the multilayer wiring board according to the embodiment of the present invention. In the multilayer wiring board 1 shown in FIG. 1 and FIG. 2, no metal wiring is formed on the first surface 10a and the second surface 10b of the inorganic substrate 10. Also, no metal wiring is included in the first surface first layer 21a and

the second surface first layer 22a. For this reason, for example, like in a multilayer wiring board 1a shown in FIG. 3, it is possible to dispose a circuit component part such as a capacitor 60 on the inorganic substrate 10. By disposing the capacitor 60 on the inorganic substrate 10, the connection distance between the semiconductor element 100 and the capacitor 60 is shortened as compared to the connection distance between the semiconductor element 100 and the capacitor being disposed on the multilayer wiring board 1. By shortening the connection distance, it is possible to enhance stability of power source voltage of the semiconductor element 100.

[0038]

<A method for manufacturing the multilayer wiring board 1 according to an embodiment of the present invention>

The method for manufacturing the multilayer wiring board 1 according to the embodiment of the present invention will be explained with reference to FIG. 4 to FIG. 15.

[0039]

In this situation, the thickness T1A of a base substrate 10A may be configured as appropriate in accordance with the purpose of use, while taking into consideration the thickness T1 of the inorganic substrate 10 observed after an etching step performed for forming the through holes. For example, T1A may be in the range of 300 μm to 500 μm. T1 may be in the range of 200 μm to 300 μm.

[0040]

(A configuration of the through holes)

FIG. 4 is a drawing showing a step of preparing the base substrate 10A. FIG. 5 is a drawing showing a step of forming the through holes 11 in the base substrate 10A. FIG. 4 and FIG. 5 show a first step of dividing the base substrate 10A into pieces and forming the inorganic substrate 10 which has the first surface 10a, the second surface 10b opposite the first surface 10a, and the lateral faces 10c connecting the peripheral edge portions of the first surface 10a to the peripheral edge portions of the second surface 10b, and which has formed therein at least one through hole 11 penetrating from the first surface 10a to the second surface 10b. The base substrate 10A is divided (separated) into the pieces, so that one part of the base substrate 10A divided into the pieces becomes the inorganic substrate 10. The first surface 10a of the inorganic substrate 10 is a surface to be exposed as a result of etching a first surface of the base substrate 10A. The second surface 10b of the inorganic substrate 10 is a surface to be exposed as a result of etching a second surface of the base substrate 10A. Accordingly, also when the base substrate 10A is described, the terms a first surface 10a and a second surface 10b shall be used.

[0041]

In the base substrate 10A shown in FIG. 4, the through holes 11 are formed as shown in FIG. 5. Examples of methods for forming the through holes 11 include a

method by which start points of the through holes are formed by laser processing and are expanded by etching. As for the laser processing, for example, it is desirable, when a femtosecond laser or a picosecond laser is used, to use an oscillation wavelength selected from among 1064 nm, 532 nm, and 355 nm. Alternatively, it is also possible to form the start points of the through holes 11, by implementing processing that uses a CO_2 laser or discharge machining. As for the base substrate 10A resulting from the laser processing, the through holes 11 are formed by immersing the base substrate 10A in hydrogen fluoride or a high-concentration alkaline etching solution (e.g., a sodium hydroxide aqueous solution or a potassium hydroxide aqueous solution) and further etching the base substrate 10A along start point parts of the through holes 11. Generally speaking, on an xy plane, etching advances isotropically. The degree of advancement of the etching varies in accordance with the thickness direction (the Z axis direction) of the inorganic substrate 10. Accordingly, spaces each having a circular cylindrical shape and having been formed in the base substrate 10A after the etching serve as the through holes 11. After the through holes 11 have been formed, the base substrate 10A is divided into the pieces, so as to form the inorganic substrate 10. It is possible to divide the base substrate 10A into the pieces by performing, for example, dicing processing using a dicing blade, scribing, laser scribing, or the like. It is also acceptable to adopt other methods for obtaining the divided pieces as appropriate.
[0042]

FIG. 6 is a cross-sectional view showing, in enlargement, one of the through holes 11 formed in the base substrate 10A. FIG. 6(a) is a cross-sectional view of the through hole 11. FIG. 6(b) is a chart showing tilt angles of the through hole 11. A method for measuring the tilt angles will be explained later. FIG. 7 is a cross-sectional view showing, in enlargement, another example of the through hole formed in the base substrate 10A. FIG. 7(a) presents a cross-sectional view of the other example of the through hole. FIG. 7(b) is a chart showing tilt angles of the other example of the through hole. The cross-sections of the through hole 11 shown in FIG. 6 and FIG. 7 are results of exposing a cross-section (a cut surface) of the through hole 11 by dividing (cutting) the base substrate 10A in the thickness direction through a scribing process and analyzing a Scanning Electron Microscope (SEM) image observed with an SEM by using image analysis software. As for the through holes 11 formed in the base substrate 10A, examples of the shape thereof include a truncated cone shape as shown in FIG. 6 in which the lateral face of the through hole 11 has a constant angle or an hourglass shape as shown in FIG. 7 in which the angle of the lateral face of the through hole 11 is vertically inverted while the 50% position being a central portion is used as a reference. As for the shape of the through holes 11, possible shapes are not limited to the above examples. It is possible to configure the shapes as appropriate, so long as the through holes 11 penetrate the first surface 10a and the second surface 10b of the base substrate 10A. The shapes of the through holes 11 are examples of through holes that are obtainable by

implementing laser processing and etching. Thus, the present disclosure is not limited by the above shapes.

[0043]

The through hole 11 shown in FIG. 6 has a truncated cone shape. The diameter of the through hole 11, which is the dimension in a direction parallel to the xy plane, exhibits a maximum value on the first surface 10a side, becomes smaller from the first surface 10a toward the second surface 10b, and exhibits a minimum value on the second surface 10b side. In FIG. 6(b), the graduations 5%, 10%, . . . and 95% indicate the distances from the first surface 10a to the second surface 10b of the inorganic substrate 10 with the percentage values. To measure the tilt angle of the lateral face of the through hole 11, at a center portion of an opening portion of the inorganic substrate 10 on the second surface 10b side, a centerline TC is drawn perpendicularly to the second surface 10b. After that, the centerline TC is shifted in a parallel displacement toward one of the two sides of the through hole 11 as indicated by the arrow A1 so as to come into contact with a point where the diameter of the through hole 11 has a minimum value. The contact point will be referred to as a reference point RP. Next, from the reference point RP, a tangent line SS is drawn on the lateral face in correspondence with each of the positions of the graduations 5% to 95%, so as to measure tilt angles θ of the tangent lines SS (i.e., the angles that are each equal to the angle between the centerline TC and the tangent line SS). The tilt angles θ are determined as the tilt angles at the cross-section positions respectively corresponding to 5% to 95%. In this situation, the positive direction of the tilt angles θ is the direction in which the diameter of the through hole 11 increases upwards. As shown in FIG. 6(b), the tilt angles θ are values between 14° and 15° approximately, on all of the positions corresponding to 5% to 95%.

[0044]

The shape of the through hole 11 shown in FIG. 7(a) has a substantially vertically symmetrical structure with respect to the position corresponding to the 50% graduation. As for the method for measuring the tilt angle of the lateral face of the through hole 11, for the section in which the distance from the first surface 10a is in the range of 5% to 50%, a centerline TC is drawn perpendicularly to the first surface 10a, in a center portion of an opening portion of the inorganic substrate 10 on the first surface 10a side, as shown in FIG. 7(b). Next, as indicated by the arrow A1, the centerline TC is shifted in a parallel displacement towards the two sides of the through hole 11, so as to come into contact with a point at which the diameter of the through hole 11 has a minimum value. The contact point will be referred to as a reference point RP. After that, from the reference point RP, a tangent line SS is drawn on the lateral face in correspondence with each of the positions of the graduations 5% to 50%, so as to measure tilt angles θ of the tangent lines SS. The tilt angles θ are determined as the tilt angles at the cross-section positions respectively corresponding to 5% to 50%. The positive direction of the tilt angles θ is the direction in which the diameter of the through hole 11 increases upwards.

Further, also for the section in which the distance from the first surface 10a is in the range of 50% to 95%, the centerline TC is shifted in a parallel displacement to the reference point RP, and a tangent line SS is drawn on the lateral face in correspondence with each of the positions of the graduations 50% to 95%. After that, the tilt angles θ of the tangent lines SS are measured. The tilt angles θ are determined as the tilt angles at the cross-section positions respectively corresponding to 50% to 95%. The negative direction of the tilt angles θ is the direction in which the diameter of the through hole 11 increases downwards.

As shown in FIG. 7(b), the tilt angles θ change from positive values to negative values, at the boundary being the 50% position. The absolute values of the tilt angles θ are between 14° and 15° approximately.

[0045]

Among the diameters of the through hole 11, the minimum diameter will be expressed as φ1, whereas the maximum diameter will be expressed as φ2. In the example in FIG. 6(a), φ1 corresponds to the opening portion on the second surface 10b side, whereas φ2 corresponds to the opening portion on the first surface 10a side. In the example in FIG. 7(a), φ1 corresponds to the diameter in the vicinity of the middle of the thickness T1, whereas φ2 corresponds to the opening portion on the second surface 10b side. The diameter φ1 is in the range of 25 μm to 100 μm. The diameter φ2 is in the range of 75 μm to 300 μm.

[0046]

(A window opening process on a glass epoxy substrate)

Next, FIG. 8 is a drawing showing a step of arranging inorganic substrates 10 obtained as divided pieces, on a glass epoxy substrate resulting from a window opening process. The inorganic substrate 10 having the through holes 11 formed therein are divided (split) into the pieces each having a prescribed shape, by using a scribing process, a laser, or the like. As shown in FIG. 8, the window opening process is performed on the glass epoxy substrate 30A having the same thickness as the thickness T1 of the inorganic substrate 10. The inorganic substrates 10 in the form of the divided pieces are arranged in space parts (which hereinafter may be referred to as window opening portions) formed by the window opening process. As for the glass epoxy substrate 30A, the substrate remains at a gap G1 between the window opening portions. The gap G1 may also be regarded as a gap between the inorganic substrates 10 arranged on the glass epoxy substrate 30A. The gap G1 is at least 50 μm or larger. Further, with regard to the sizes of the inorganic substrates 10 in the form of the divided pieces, the window opening process is performed so that a gap G2 equal to or greater than 100 μm is formed, for example, between the inorganic substrates 10 and the glass epoxy substrate 30A. For the window opening process, a router, a laser, or the like may be used. In addition, a counterboring process has been applied to the window opening portions. The processing scheme described above is merely an example. It is also possible to select from among other processing schemes, as appropriate. When divided pieces

of the multilayer wiring board 1 are obtained from the base substrate 10A, the outer periphery protection portion 30 of the multilayer wiring board 1 is configured by a part separated from the glass epoxy substrate 30A.

[0047]

(Positioning of the protection resin portions)

Next, FIG. 9 is a drawing showing a step of stacking the resin material on the glass epoxy substrate 30A. More specifically, FIG. 9 shows a second step of arranging the inorganic substrates 10 on the glass epoxy substrate 30A resulting from the window opening process; disposing the resin material on the first surface 10a, the second surface 10b, and the lateral faces 10c and in the through holes 11 of the inorganic substrates 10; forming the first surface first layer 21a on the first surface 10a; and forming the second surface first layer 22a on the second surface 10b. As shown in FIG. 9, to the glass epoxy substrate 30A arranged on the inorganic substrates 10, the resin material is injected from both surfaces in the Z axis positive direction and in the Z axis negative direction. As a result of injecting the resin material, the protection resin portions 25 are stacked thereon. As the resin material, it is possible to use, for example, a material obtained by adding a filler such as silica, titanium oxide, aluminum oxide, magnesium oxide, zinc oxide, or the like to at least one resin selected from among epoxy resin, urethane resin, silicon resin, polyester resin, oxetane resin, and polyamide resin. The resin material has an elastic modulus in the range of 6 GPa to 15 GPa and a linear expansion coefficient in the range of 11 to 30 ppm/Deg. C and is preferably a thermosetting resin. Further, it is also acceptable to use a material containing glass cloth as necessary.

Examples of methods for injecting the resin material onto the glass epoxy substrate 30A include vacuum pressure press, heat press, compression molding, and transfer molding methods. As long as it is possible to inject the resin material into the gap G1 formed between the glass epoxy substrate 30 resulting from the window opening process and the inorganic substrates 10 without any air bubbles, it is possible to select a processing scheme as appropriate. In this situation, it is preferable that the injection is performed by using a vacuum pressure press scheme and to select a processing scheme by which heat and pressure are applied at the same time in a vacuum.

Before the step shown in FIG. 9, when the inorganic substrates 10 has been arranged on the glass epoxy substrate 30A resulting from the window opening process, it is also possible to form a multilayer wiring board 1a having the capacitor 60 shown in FIG. 3 built in, by injecting the resin material after arranging the capacitor 60 on the inorganic substrates 10.

[0048]

FIG. 10 is a cross-sectional view of a state arrived at by arranging the inorganic substrates 10 on the glass epoxy substrate 30A resulting from the window opening process and subsequently injecting the resin material. FIG. 10 is a cross-sectional view taken at line AA in FIG. 9, for example. Because the resin material is

one part structuring the protection resin portions 25, the resin material is shown as a protection resin portion 25 in FIG. 10. Further, the resin material disposed on the first surface 10a of the inorganic substrate 10 forms the first surface first layer 21a. The resin material disposed on the second surface 10b of the inorganic substrate 10 forms the second surface first layer 22a.

As shown in FIG. 10, the resin material has been injected into the gap G2 between the glass epoxy substrate 30A and the inorganic substrate 10 and into the through holes 11 formed in the inorganic substrates 10. In this situation, to ensure close contact between the inorganic substrates 10 and the protection resin portions 25 and between the glass epoxy substrate 30A and the protection resin portions 25, it is also possible to enhance the close contact characteristics by applying a silane coupling process or the like to the inorganic substrates 10 and the glass epoxy substrate 30A. It is possible to configure the silane coupling process as appropriate in accordance with the resin material being used. Further, if the silane coupling process is not performed, it is acceptable to roughen the surfaces of the inorganic substrates 10 and the glass epoxy substrate 30A and to implement a close contact process using an anchoring effect. It is possible to configure a close contact process as appropriate in accordance with the purpose of use of the multilayer wiring board 1. In this situation, because the counterboring process has been applied at the time of performing the window opening process on the glass epoxy substrate 30A, a region Rc of the glass epoxy substrate 30A has a roughened surface due to the counterboring process. By performing a counterboring process, it is also possible to enhance the close contact characteristics between the glass epoxy substrate 30A and the resin material.

Further, although FIG. 10 shows the example in which the resin material is left on the surfaces of the inorganic substrates 10, as the first surface first layer 21a and the second surface first layer 22a, the resin material on the surfaces of the inorganic substrates 10 may be omitted. As long as the resin material is injected in the through holes 11, the first surface first layer 21a and the second surface first layer 22a may be omitted, or only one of the two may be present. (The same applies to the following disclosure referring to FIG. 11 and thereafter.)

[0049]

FIG. 11 is a drawing showing a step (a third step) of forming a sub through hole 12, which is a through hole formed in the resin material, by using a laser inside the through hole 11.

The sub through hole 12 penetrates the protection resin portion 25 that has been injected into the through hole 11 of the inorganic substrate 10. Besides the laser processing, it is also possible to form the sub through hole 12 by drill machining, for example. To form the sub through hole 12 in the protection resin portion 25, position alignment is carried out by using the through hole 11 formed in the inorganic substrate 10 as an alignment mark. A processing diameter of the sub through hole 12 to be formed in the protection resin portion 25 is configured to be

smaller than the processing diameters φ1 and φ2 of the through hole 11 formed in the inorganic substrate 10 and so that, with respect to the diameter φ1 being the minimum value among the processing diameters of the through hole 11, some resin is left around the sub through hole 12 with a thickness of at least 10 μm. When the sub through hole 12 is to be formed by laser processing, it is possible to use either a CO_2 laser or a UV laser. To penetrate the protection resin portion 25, it is acceptable to perform the processing multiple times.

[0050]

Next, with reference to FIG. 12, a relationship between processing shapes of the through hole 11 formed in the inorganic substrate 10 and the sub through hole 12 formed in the protection resin portion 25 will be explained. FIG. 12 is a cross-sectional view showing an example of a processing shape of the sub through hole 12. The shape of the through hole 11 formed in the inorganic substrate 10 may be a truncated cone shape or an hourglass shape. The shape of the sub through hole 12 formed in the protection resin portion 25 is a truncated cone shape. As for combinations of the through hole 11 and the sub through hole 12, possible combinations are shown as (a) to (f) in FIG. 12. FIG. 12(a) shows an example in which the through hole 11 has an hourglass shape, whereas the sub through hole 12 has a truncated cone shape of which the diameter decreases toward the Z axis negative direction. FIG. 12 (b) shows an example in which the through hole 11 has a truncated cone shape of which the diameter decreases toward the Z axis negative direction, whereas the sub through hole 12 has a truncated cone shape of which the diameter decreases toward the Z axis negative direction. FIG. 12 (c) shows an example in which the through hole 11 has a truncated cone shape of which the diameter decreases toward the Z axis positive direction, whereas the sub through hole 12 has a truncated cone shape of which the diameter decreases toward the Z axis negative direction. FIG. 12(d) to FIG. 12(f) show examples which correspond to FIG. 12(a) to FIG. 12(c) respectively and in which the direction toward which the sub through hole 12 becomes smaller has been changed to the Z axis positive direction.

[0051]

The sub through hole 12 is formed for the purpose of disposing the through electrode 15 which electrically connects the first surface 10a side to the second surface 10b side of the inorganic substrate 10. As long as the joining of the through electrode 15 is possible and connection reliability is ensured, it is possible to configure a combination of the processing shapes of the through hole 11 and the sub through hole 12, as appropriate. In accordance with a wiring density of the first surface layer structure 21 and the second surface layer structure 22 of the multilayer wiring board 1, it is possible to configure processing diameters of the through hole 11 and the sub through hole 12 (in other words, the opening diameter of the sub through hole 12 on a yz plane) and a processing pitch (in other words, the distance between any two through holes 12 positioned adjacent to each other). In this situation, as

shown in FIG. 12, the thickness d1 of the protection resin portion 25 is the thickness of the location where the distance between the through hole 11 and the through hole 12 is the shortest. In the examples in FIG. 12(a) and FIG. 12(d), the thickness d1 is in an approximately middle portion of the inorganic substrate 10. In the examples in FIG. 12(b) and FIG. 12(e), the thickness d1 is on the second surface 10b side. In the examples in FIG. 12(c) and FIG. 12(f), the thickness d1 is on the first surface 10a side.

[0052]

Regarding the combination of the processing shapes of the through hole 11 and the sub through hole 12, when the distance between the sub through hole 12 and the through hole 11 is shorter (in other words, when the thickness d1 of the protection resin portion 25 present between the sub through hole 12 and the through hole 11 is smaller), there is a higher possibility of a failure due to an impact of stress caused by the difference in linear expansion coefficients between the wiring layers, the semiconductor element and the protection resin portion 25. Among the relationships shown in FIG. 12, the combinations (a), (b), (d), and (f) are preferable. In consideration of routing the wirings of the semiconductor element and the wiring layers, the combinations (d) and (f) are even more preferable. It is possible to configure a combination of the shapes as appropriate in accordance with the purpose of use.

[0053]

With reference to FIG. 13, the following will explain a step of forming a conductor portion in the through hole 12 formed in the insulating resin portion 25 that has been injected into the through hole 11 of the inorganic substrate 10. FIG. 13 is a drawing showing a step (a fourth step) of disposing the conductor portions on the sub through holes 12, the first surface first layer 21a, and the second surface first layer 22a. As for disposing the conductor portion into the through hole 12, a seed layer is formed inside the through hole 12 by implementing an electroless plating method and subsequently a wiring pattern is formed by performing a photolithography process, before the conductor portion is formed by performing an electrolytic plating process.

Generally speaking, a sputtering method may be used for forming a seed layer in a through hole; however, for a through hole having a high aspect ratio, it would be difficult to form a sputter seed layer (a seed layer formed by implementing a sputtering method) so as to cover the entire through hole (so as not to have any gap over the entire through hole). If a seed layer were to be formed in the through hole 11 of the inorganic substrate 10, it might require forming a sputter seed layer, subsequently applying an electroless Ni plating process thereto, and once again forming the seed layer over the entire through hole 11. Because it would be difficult to form an electroless plated coating on the inorganic substrate 10, a method might be adopted by which the sputter seed layer is combined with the electroless plating.

In the structure of the present invention, because the seed layer is formed in the sub through hole 12, the seed layer is formed on the protection resin portion 25, and as a result, the seed layer formation using the electroless plating method is adopted.

[0054]

Examples of the material for the metal seed layer formed inside the sub through hole 12 by implementing the electroless plating method include Cu, Ni, Al, Ti, Cr, Mo, W, Ta, Au, Ir, Ru, Pd, Pt, and the like. It is desirable to use Cu. The composition of the solution may include, for example, a copper salt such as copper sulfate or copper chloride, Rochelle salt for retaining copper ions, ethylenediaminetetraacetic acid (EDTA), formalin, and the like. It is possible to adjust the composition of the solution as appropriate, in accordance with chemical resistance of the insulating resin being used. As for the thickness of the metal seed layer formed by implementing the electroless plating method, it is desirable to form the metal seed layer inside the sub through holes 12 with a thickness of at least 0.3 μm. If the thickness were 0.3 μm or smaller, coating characteristics of the metal seed layer formed by implementing the electroless plating would be insufficient, and the conductor layer formed as an electrolytic plated coating would be non-contiguous. As long as the thickness of the metal seed layer formed by implementing the electroless plating is equal to or greater than 0.3 μm, it is possible to configure the thickness of the metal seed layer as appropriate.

[0055]

After the metal seed layer is formed inside the sub through holes 12 by implementing the electroless plating, a resist pattern is formed by performing a photolithography process, and subsequently, the through electrodes 15, the metal wirings 21b1, and the metal wirings 22b1 are formed by implementing an electrolytic plating method. To form the resist pattern by performing the photolithography process, for example, a dry film resist is laminated, and a pattern is drawn with light exposure and developed. The resist pattern formation using the photolithography is a step performed by using materials that are generally used in an FC-BGA wiring forming step. The resist pattern will be delaminated after the electrolytic plating process. Extra portions of the seed layer will be removed by etching. It should be noted that the conductor portion is not formed in the location (which hereinafter may be referred to as "dicing processing portion") where the dicing processing is to be performed. More specifically, the "dicing processing portion" is a certain part of the wiring layer overlapping with a region Rd where the dicing processing is to be performed on the glass epoxy substrate 30A and is the certain part of the wiring layer corresponding to the position in which the alignment mark (explained later) is formed. The dicing processing portion is, for example, a position through which a dicing blade passes and/or a position in which scribing is performed. In the dicing processing portion, no seed layer is formed, and no metal wiring is formed. The same applies to the other wiring layers included in the first surface layer structure 21 and the

second surface layer structure 22. Because metal materials are excluded from the member to be shaved subject to the dicing processing, it is possible in a piece dividing step (explained later), to reduce impacts on processability of the multilayer wiring board.

[0056]

Examples of the material used for the through electrodes 15, the metal wirings 21b1, and the metal wirings 22b1 to be formed by implementing the electrolytic plating method on the sub through holes 12 include Cu, Ni, Al, Ti, Cr, Mo, W, Ta, Au, Ir, Ru, Pd, Pt, and the like. It is desirable to use Cu. The composition of the solution includes, as main ingredients thereof, copper sulfate pentahydrate, sulfuric acid, and chloride ions. To ensure uniformity of the plated coating, the through electrodes 15, the metal wirings 21b1, and the metal wirings 22b1 are formed by using a plating solution of which the solution composition contains at least one additive. It is desirable to form the through electrodes 15, the metal wirings 21b1, and the metal wirings 22b1 so as to have a thickness of at least 2 μm or larger. If the thickness were 2 μm or smaller, the conductor layer would be non-contiguous, which would increase a resistance value observed when the wiring layers on the first surface 10a side and the second surface 10b side are electrically connected via the through electrode 15. Consequently, as long as the conductor layer is formed with a thickness of at least 2 μm or larger, it is possible to configure the thickness as appropriate.

[0057]

Next, with reference to FIG. 14, a wiring layer forming step (a fifth step) performed on the first surface layer structure 21 and the second surface layer structure 22 of the multilayer wiring board 1 will be explained. FIG. 14 is a drawing showing the step (the fifth step) of forming, on the first surface 10a side, at least two wiring layers in addition to the first surface first layer 21a and forming, on the second surface 10b side, at least two wiring layers in addition to the second surface first layer 22a. After the through electrodes 15, the metal wirings 21b1, and the metal wirings 22b1 shown in FIG. 13 are formed, the resin material is disposed on the first surface 10a side and the second surface 10b side, so as to form vias by performing laser processing. Subsequently, a seed layer is formed by performing an electroless plating process or a sputtering process, and a resist pattern is formed by performing a photolithography process. By using the formed resist pattern, a wiring pattern is formed by performing electrolytic plating. After that, the resist pattern is delaminated, and extra portions of the seed layer are removed by etching. As a result, the first surface second layer 21b including the through electrodes connected to the metal wirings 22b1 and the metal wirings 21b2, as well as the second surface second layer 22b including the through electrodes connected to the metal wirings 22b1 and the metal wirings 22b2 are formed. After that, the steps described above are repeatedly performed in accordance with the number of layers being necessary. In the example shown in FIG. 14, six wiring layers in total each (21a to 21f and 22a to

22f) are formed on the first surface 10a side and on the second surface 10b side. On the outermost layers 21g and 22g, the solder resist layers 40 are formed. In the outermost layer 21g, insertion openings for connection terminals of the semiconductor element 100 are formed. Formed inside the insertion openings are solder bumps 50 configured with Sn, SnAg, Ni/Sn, Ni/SnAg, Ni/Cu/Sn, Ni/Cu/SnAg, or the like. The order in which the wiring layers are formed is not limited to the order described above. It is also acceptable to form the wiring layers 22a to 22f and the outermost layer 22g on the second surface 10b side, after forming the wiring layers 21a to 21f and the outermost layer 21g on the first surface 10a side.
[0058]

The resin material used for the wiring layers (21a to 21f and 22a to 22f) included in the first surface layer structure 21 and the second surface layer structure 22 is the same as the resin material injected into the through holes 11. The method for stacking the resin material may be selected from among a vacuum pressure press method, a heat press method, a compression molding method, a transfer molding method, and the like. Preferably, a vacuum pressure press method may be adopted. However, possible embodiments are not limited to the above description. It is acceptable to modify the steps and the methods as appropriate, if necessary.
[0059]

Next, with reference to FIG. 15, the piece dividing step performed on the multilayer wiring board 1 will be explained. FIG. 15 is a drawing schematically showing the glass epoxy substrate 30A and the alignment marks used for the dicing processing. In FIG. 15, alignment marks 31 are indicated with dash-dotted lines. The alignment marks 31 are provided in the locations of the gaps G1 on the glass epoxy substrate 30A. For example, the alignment marks 31 are formed on the solder resist layer 40 in the first surface layer structure 21 in FIG. 14. After the alignment marks 31 are formed, a sixth step is performed in which the dicing processing using blade dicing is performed between the inorganic substrates 10 disposed on the glass epoxy substrate 30A, so as to obtain the divided pieces. More specifically, as a result of the piece dividing process implementing the dicing processing which uses the dicing blade along the alignment marks 31, the multilayer wiring board 1 is separated from the glass epoxy substrate 30A. Because the processing is performed along the glass epoxy substrate 30A, it is possible to obtain the multilayer wiring board 1 without bringing the blade into contact with the inorganic substrates 10.

It should be noted that the dicing processing is not limited to the method described above. Alternatively, it is also acceptable to form the alignment marks on the solder resist layers 40 in both the first surface layer structure 21 and the second surface layer structure 22 and to perform the dicing processing from both of the Z axis positive direction and the Z axis negative direction.
[0060]

<Examples according to the embodiments of the present invention and comparison examples>

Multilayer wiring boards were produced to make evaluations. In the following explanations, the multilayer wiring boards 1 according to the embodiments of the present invention will be referred to as Examples 1 to 3. Comparison examples will be referred to as Comparison Examples 1 to 3. Examples 1 to 3 correspond to the configuration of the multilayer wiring board 1 shown in FIG. 1. Comparison Example 1 corresponds to the configuration in FIG. 16. Comparison Examples 2 and 3 correspond to the configuration in FIG. 17.

[0061]

<Example 1>

In Example 1, used as the inorganic substrate 10 was glass which had a linear expansion coefficient of 3.1 ppm/°C and an elastic modulus of 77 GPa and which satisfied the thickness T1 = 0.7 mm. Further, used as the glass epoxy substrate 30A was a glass epoxy substrate (E-705G manufactured by Resonac K. K.) having the same thickness, 0.7 mm, as the thickness T1 of the inorganic substrate 10. Used as the resin material structuring the protection resin portions 25 was a material which had a linear expansion coefficient of 20 ppm/°C and an elastic modulus of 7.5 MPa and of which the filler content amount was 72 wt%. In this situation, eight wiring layers were included in the first surface layer structure 21. Also, eight wiring layers were included in the second surface layer structure 22. Further, in a planar view (i.e., as viewed from the Z axis positive direction), the multilayer wiring board 1 had a square shape, and the length L = 120 mm was true.

(The conditions used for producing Example 1)

The inorganic substrate 10: the glass which had a linear expansion coefficient of 3.1 ppm/°C and an elastic modulus of 77 GPa and which satisfied the thickness T1 = 0.7 mm

The resin material: a linear expansion coefficient of 20 ppm/°C; an elastic modulus of 7.5 MPa; and a filler content amount of 72 wt%

The glass epoxy substrate: E-705G (manufactured by Resonac K. K.) having a thickness of 0.7 mm

The size (the dimensions on an xy plane): 120 mm × 120 mm

The number of wiring layers included in the first surface layer structure 21 and in the second surface layer structure 22: 8 layers

An average percentage of the copper remaining in the wiring layers included in the first surface layer structure 21: 84%

An average percentage of the copper remaining in the wiring layers included in the second surface layer structure: 76%

[0062]

<Example 2>

In Example 2, used as the inorganic substrate 10 was ceramics which had a linear expansion coefficient of 6.1 ppm/°C and an elastic modulus of 57 GPa and

which satisfied the thickness T1 = 0.7 mm. The other configurations besides the above were the same as those in Example 1.
(The conditions used for producing Example 2)

The inorganic substrate 10: the ceramics which had a linear expansion coefficient of 6.1 ppm/°C and an elastic modulus of 57 GPa and which satisfied the thickness T1 = 0.7 mm

The resin material: a linear expansion coefficient of 20 ppm/°C; an elastic modulus of 7.5 MPa; and a filler content amount of 72 wt%

The glass epoxy substrate: E-705G (manufactured by Resonac K. K.) having a thickness of 0.7 mm

The size (the dimensions on an xy plane): 120 mm × 120 mm

The number of wiring layers included in the first surface layer structure 21 and in the second surface layer structure 22: 8 layers

An average percentage of the copper remaining in the wiring layers included in the first surface layer structure 21: 84%

An average percentage of the copper remaining in the wiring layers included in the second surface layer structure 22: 76%

[0063]

The comparison examples of the multilayer wiring board 1 according to the embodiments of the present invention will be explained with reference to FIG. 16 and FIG. 17.

[0064]

<Comparison Example 1>

FIG. 16 is a cross-sectional view showing a multilayer wiring board in Comparison Example 1. A multilayer wiring board 1-1 in Comparison Example 1 was different from Examples 1 and 2 in that an organic substrate 10-1 was used as a core substrate in place of the inorganic substrate 10; the through electrodes 15 were formed without disposing a resin material in the through holes of the organic substrate 10-1; a first surface first layer 21a-1 and a second surface first layer 22a-1 included metal wirings; metal wirings were disposed on the organic substrate 10-1; and there was no configuration corresponding to the outer periphery protection portion 30. In the following sections, explanations of some of the constituent elements that are the same as or similar to those in Example 1 and Example 2 described above will be simplified or omitted.

[0065]

In Comparison 1, used as the organic substrate 10-1 was a glass epoxy substrate 30 (E-705G manufactured by Resonac K. K.) which satisfied a thickness T1-1 = 1.2 mm. Used as the resin material structuring a first surface layer structure 21-1 and a second surface layer structure 22-1 was a material which had a linear expansion coefficient of 20 ppm/°C and an elastic modulus of 7.5 MPa and of which the filler content amount was 72 wt%. The multilayer wiring board 1 was formed so

as to have the structure shown in FIG. 16. The configuration of the multilayer wiring board 1-1 was as follows:
(The conditions used for producing Comparison Example 1)

The organic substrate 10-1: E-705G (manufactured by Resonac K. K.) having a thickness of 1.2 mm

The resin material: a linear expansion coefficient of 20 ppm/°C; an elastic modulus of 7.5 MPa; and a filler content amount of 72 wt%

The size (the dimensions on an xy plane): 120 mm × 120 mm

The number of wiring layers included in the first surface layer structure 21-1 and in the second surface layer structure 21-2: 7 layers

An average percentage of the copper remaining in the wiring layers included in the first surface layer structure 21-1: 84%

An average percentage of the copper remaining in the wiring layers included in the second surface layer structure 22-1: 76%

[0066]

<Comparison Example 2>

FIG. 17 is a cross-sectional view showing a multilayer wiring board 1-2 in Comparison Example 2. The multilayer wiring board 1-2 in Comparison Example 2 was different from Examples 1 and 2 in that the through electrodes 15 were formed without disposing a resin material in the through holes of an inorganic substrate 10-2; a first surface first layer 21a-2 and a second surface first layer 22a-2 included metal wirings; metal wirings were disposed on the inorganic substrate 10-2; and there was no configuration corresponding to the outer periphery protection portion 30. In the following sections, explanations of some of the constituent elements that are the same as or similar to those in Example 1 and Example 2 described above will be simplified or omitted.

[0067]

In Comparison Example 2, used as the inorganic substrate 10-2 was glass which had a linear expansion coefficient of 3.1 ppm/°C, an elastic modulus of 77 GPa, and a thickness of 0.7 mm. Used as the resin material structuring a first surface layer structure 21-2 and a second surface layer structure 22-2 was a material which had a linear expansion coefficient of 20 ppm/°C and an elastic modulus of 7.5 MPa and of which the filler content amount was 72 wt%. The configurations of the wiring layers included in the first surface layer structure 21-2 and the second surface layer structure 22-2 were the same as those in Comparison Example 1.
(The conditions for producing Comparison Example 2)

The inorganic substrate 10-2: the glass which had a linear expansion coefficient of 3.1 ppm/°C and an elastic modulus of 77 GPa and which satisfied the thickness T1 = 0.7 mm

The resin material: a linear expansion coefficient of 20 ppm/°C; an elastic modulus of 7.5 MPa; and a filler content amount of 72 wt%

The size (the dimensions on an xy plane): 120 mm × 120 mm

The number of wiring layers included in the first surface layer structure 21-2 and in the second surface layer structure 22-2: 7 layers

An average percentage of the copper remaining in the wiring layers included in the first surface layer structure 21-2: 84%

An average percentage of the copper remaining in the wiring layers included in the second surface layer structure 22-2: 76%

[0068]

<Comparison Example 3>

Comparison Example 3 had the same configuration as the structure shown in FIG. 17. Comparison Example 3 was different from Comparison Example 2 in that, used as the inorganic substrate 10-2 was ceramics which had a linear expansion coefficient of 6.1 ppm/°C, an elastic modulus of 57 GPa, and a thickness of 0.7 mm. The other configurations were the same as those of Comparison Example 2.

(The conditions used for producing Comparison Example 3)

The inorganic substrate 10-2: the ceramics which had a linear expansion coefficient of 6.1 ppm/°C and an elastic modulus of 57 GPa and which satisfied the thickness T1 = 0.7 mm

The resin material: a linear expansion coefficient of 20 ppm/°C; an elastic modulus of 7.5 MPa; and a filler content amount of 72 wt%

The size (the dimensions on an xy plane): 120 mm × 120 mm

The number of wiring layers included in the first surface layer structure 21-2 and in the second surface layer structure 22-2: 7 layers

An average percentage of the copper remaining in the wiring layers included in the first surface layer structure 21-2: 84%

An average percentage of the copper remaining in the wiring layers included in the second surface layer structure 22-2: 76%

[0069]

<Evaluation Results>

Table 1 presents failure occurrence rates in the piece dividing step observed when the multilayer wiring boards in the examples of the present embodiments and the comparison examples were produced. For both the examples of the present embodiments and the comparison examples, the dicing processing was performed under the conditions presented below. The number n of the multilayer wiring boards produced by performing the dicing processing was 200.

<The conditions for the dicing processing>

The dicing blade: R07-SD600-BB200-75, 56 × 0.15A2 × 40 (manufactured by DISCO CORPORATION)

The blade rotation speed: 30,000 rpm

The blade feed speed: 10 mm/sec

[0070]

As presented in Table 1, in Examples 1 and 2 and Comparison Example 1, no failure occurred in the piece dividing step. In contrast, failures occurred at a rate of

96.7% in Comparison Example 1 and at a rate of 75.2% in Comparison Example 2. In Comparison Example 1 and Comparison Example 2, because the glass and the ceramics were directly processed by the dicing blade, the amount of grinding was reduced as compared to Examples 1 and 2 in which the dicing processing was performed on the glass epoxy substrate 30A. In addition, there was a possibility that the processing surfaces might be chipped or cracked. The failure occurrence rates presented in Table 1 include the situation in which chipping or cracking occurred at the time of the dicing processing and the situation in which the core substrate had a fissure due to stress caused by a difference in linear expansion coefficients between the wiring layers included in the first surface layer structure and the second surface layer structure and the core substrate (the inorganic substrates 10 and 10-2 and the organic substrate 10-1).

[Table 1]

	Example 1	Example 2	Comparison Example 1	Comparison Example 2	Comparison Example 3
Failure Occurrence Rate	0.0%	0.0%	0.0%	96.7%	75.2%

n=200

[0071]

Next, Table 2 presents warping amounts of the multilayer wiring boards to which a thermal history was applied in the state in which the semiconductor element 100 was installed on the multilayer wiring boards in the examples of the present embodiments and the comparison examples. As for the thermal history applied in the state in which the semiconductor element 100 was installed, heat was applied from room temperature (RT) to 260°C, the temperature was decreased back to RT, and warping of the multilayer wiring boards was evaluated at 10°C intervals. The number n of the samples that were evaluated was 10. Average values of warping amounts were calculated.

The warping amounts presented in Table 2 were warping amount observed when the temperature was maintained at 260°C. For multilayer wiring boards, the smaller the warping amount is, the more desirable. As presented in Table 2, the warping amount in Example 1 was 66.4 μm, in Example 2 was 89.7 μm, in Comparison Example 1 was 213.1 μm, and in Comparison Example 3 was 71.5 μm. Because Comparison Example 2 had a high failure occurrence rate in the piece dividing step, it was not possible to make an evaluation. Although Comparison Example 3 exhibited a good result of 71.5 μm, because the failure occurrence rate in the piece dividing step was high, industrial practicality is low. As compared to Comparison Example 1, the warping amounts of the multilayer wiring boards 1 in Example 1 and Example 2 were smaller and were no greater than 100 μm. It can be determined that Example 1 and Example 2 had excellent structures. The warping amounts were measured by implementing a shadow moire method by using TherMoire manufactured by AcroMetrix.

[Table 2]

	Example 1	Example 2	Comparison Example 1	Comparison Example 2	Comparison Example 3
Warping Amount	66.4	89.7	213.1	-	71.5

n=10

[0072]

Next, Table 3 presents reliability evaluation results from a temperature cycle test performed on the examples of the present embodiments and the comparison examples. In the temperature cycle test, one cycle (which hereinafter may be written as "1 cycle") denotes increasing the temperature from the state at -55°C to RT and then to 125°C and again changed to RT and then to -55°C. Each of the temperature levels was maintained for 30 minutes. After a predetermined number of cycles, the exterior appearance was examined for chipping, cracks, and the like, and also, a predetermined electric characteristic examination was performed. In addition, before undergoing the temperature cycle test, reflow at 260°C had been performed three times. The exterior appearance examination and the electric characteristic examination were also performed before undergoing the temperature cycle test ("After Being Divided Into Pieces" in the table) and after the reflow ("Multiple Reflow" in the table). The number n of evaluated samples was 20. When 90 percent of the samples passed both the exterior appearance examination and the electric characteristic examination, the test result is indicated as "Passed" and is otherwise indicated as "Failed". As presented in Table 3, Example 1, Example 2, and Comparison Example 1 passed the test even after 2000 cycles, and thus reliability thereof was guaranteed. In contrast, Comparison Example 2 and Comparison Example 3 did not pass the examinations both before the temperature cycle test and after the temperature cycle test, and reliability thereof was not guaranteed.

[Table 3]

	Example 1	Example 2	Comparison Example 1	Comparison Example 2	Comparison Example 3
After Being Divided Into Pieces	Passed	Passed	Passed	Failed	Passed
Multiple Reflow	Passed	Passed	Passed	Failed	Passed
50 cycles	Passed	Passed	Passed	Failed	Passed
100 cycles	Passed	Passed	Passed	Failed	Passed
200 cycles	Passed	Passed	Passed	Failed	Failed
300 cycles	Passed	Passed	Passed	Failed	Failed
500 cycles	Passed	Passed	Passed	Failed	Failed
700 cycles	Passed	Passed	Passed	Failed	Failed
1000 cycles	Passed	Passed	Passed	Failed	Failed
1500 cycles	Passed	Passed	Passed	Failed	Failed
2000 cycles	Passed	Passed	Passed	Failed	Failed

n=20

[0073]

<Functions and Advantageous Effects>

According to the embodiments of the present invention described above, it is possible to prevent warping and to achieve high reliability. Consequently, it is possible to provide the multilayer wiring board 1 of which it is possible to prevent warping and which has high reliability.

[0074]

<Industrial Applicability>

According to the present invention, it is possible to provide the multilayer wiring board 1 of which it is possible to prevent warping and which has high reliability. Consequently, because it is possible to install a plurality of semiconductor elements, it is possible to make a contribution to enhancing performances of semiconductor apparatuses such as a GPU or a CUP, for example. Further, the present disclosure may be applied to a multilayer wiring board for a photoelectric conversion package used in optical data communication or for optical disaggregated computing. Thus, it is possible to make a contribution to the data communication society and realization of Society 5.0.

[0075]

The scope of the present invention is not limited to the exemplary embodiments presented in the drawings and the description and includes various modification examples. For instance, the above embodiments were explained in detail to facilitate comprehension of the present invention. Thus, the present invention is not necessarily limited to a configuration including all the described elements.

Further, one or more of the elements in a certain embodiment may be replaced with one or more of the elements from another embodiment. In addition, it is also possible to add one or more elements from one embodiment to the elements in another embodiment. Furthermore, one or more of the elements in each of the embodiments may have an additional element, or may be deleted or substituted.

[0076]

The following presents certain aspects describing the present invention; however, the present invention is not limited to these aspects.

(Aspect 1)

A multilayer wiring board including:

an inorganic substrate which has a first surface, a second surface opposite the first surface, and a lateral face connecting a peripheral edge portion of the first surface to a peripheral edge portion of the second surface, and which has formed therein at least one through hole penetrating from the first surface to the second surface;

a protection resin portion disposed in the through hole of the inorganic substrate and disposed so as to cover the lateral face of the inorganic substrate; and

a through electrode which includes a conductor portion extending inside the through hole and establishes an electric connection between the first surface and the second surface.

(Aspect 2)

The multilayer wiring board according to aspect 1, wherein

in the through hole, the conductor portion is covered by the protection resin portion.

(Aspect 3)

The multilayer wiring board according to aspect 1 or 2, wherein

in the through hole, a thickness of the protection resin portion disposed between the inorganic substrate and the conductor portion is at least 10 μm.

(Aspect 4)

The multilayer wiring board according to any one of aspects 1 to 3, further including:

a first surface layer structure formed on the first surface of the inorganic substrate; and

a second surface layer structure formed on the second surface of the inorganic substrate, wherein

each of the first surface layer structure and the second surface layer structure has two or more wiring layers,

a first surface first layer included in the first surface layer structure and formed on the inorganic substrate and a second surface first layer included in the second surface layer structure and formed on the inorganic substrate have no metal wiring, and

one or more wiring layers included in the first surface layer structure and excluding the first surface first layer and one or more wiring layers included in the second surface layer structure and excluding the second surface first layer have metal wirings formed therein.

(Aspect 5)

The multilayer wiring board according to any one of aspects 1 to 4, wherein

the protection resin portion is configured by using the same resin material as a resin material used for the wiring layers included in the first surface layer structure and the second surface layer structure,

the resin material contains a filler mixed in to satisfy a range of 40 wt% to 80 wt% inclusive and having an average particle diameter in a range of 0.3 μm to 1.0 μm inclusive, and

the resin material further contains a build-up resin or glass cloth.

(Aspect 6)

The multilayer wiring board according to any one of aspects 1 to 5, wherein

the protection resin portion disposed on the lateral face of the inorganic substrate has a thickness of at least 50 μm.

(Aspect 7)

The multilayer wiring board according to any one of aspects 1 to 6, wherein

an outer periphery portion of the multilayer wiring board is covered by the protection resin portion and an outer periphery protection portion configured by separating a part of a glass epoxy substrate.

(Aspect 8)

The multilayer wiring board according to any one of aspects 1 to 7, wherein

a capacitor is disposed on the inorganic substrate.

(Aspect 9)

The multilayer wiring board according to any one of aspects 1 to 8, wherein

the inorganic substrate is configured from glass or a ceramic material.

(Aspect 10)

A semiconductor apparatus wherein

at least one semiconductor element is installed, via an interposer substrate, on the multilayer wiring board according to any one of aspects 1 to 9.

(Aspect 11)

A method for manufacturing a multilayer wiring board, the method including:

a first step of dividing a base substrate into pieces and forming inorganic substrates each of which has a first surface, a second surface opposite the first surface, and a lateral face connecting a peripheral edge portion of the first surface to a peripheral edge portion of the second surface, the inorganic substrates each having formed therein at least one through hole penetrating from the first surface to the second surface;

a second step of arranging the inorganic substrates on a glass epoxy substrate resulting from a window opening process, disposing a resin material on the first surface, the second surface, and the lateral face and in the through hole of the inorganic substrate, forming a first surface first layer on the first surface, and forming a second surface first layer on the second surface;

a third step of using a laser inside the through hole and forming a sub through hole being a through hole formed in the resin material;

a fourth step of disposing a conductor portion in the sub through hole, the first surface first layer, and the second surface first layer;

a fifth step of forming, on the first surface side, at least two wiring layers in addition to the first surface first layer and forming, on the second surface side, at least two wiring layers in addition to the second surface first layer; and

a sixth step of obtaining divided pieces by performing dicing processing using blade dicing between the inorganic substrates arranged on the glass epoxy substrate.

(Aspect 12)

The method for manufacturing a multilayer wiring board according to aspect 11, wherein

in the second step, an interval between the inorganic substrates arranged on the glass epoxy substrate is at least 50 μm or larger.

(Aspect 13)

The method for manufacturing a multilayer wiring board according to aspect 11 or 12, wherein

in the fourth step, a seed layer is formed by performing an electroless copper plating process, and the conductor portion is formed by performing an electrolytic plating process.

(Aspect 14)

The method for manufacturing a multilayer wiring board according to any one of aspects 11 to 13, wherein

in the first step and the second step, a capacitor is disposed on the inorganic substrate.

(Aspect 15)

The method for manufacturing a multilayer wiring board according to any one of aspects 11 to 14, wherein

the inorganic substrates are configured from glass or a ceramic material.

(Aspect 16)

The method for manufacturing a multilayer wiring board according to any one of aspects 11 to 15, wherein

in the fourth step, the conductor portion is not formed in a location where the dicing processing is performed.

Reference Signs List

[0077]

1, 1-1, 1-2, 1a: multilayer wiring board; 10, 10-2: inorganic substrate; 10-1: organic substrate; 10A: base substrate; 11: through hole; 12: sub through hole; 15: through electrode; 21: first surface layer structure; 22: second surface layer structure; 25: protection resin portion; 30: outer periphery protection portion; 30A: glass epoxy substrate; 40: solder resist layer; 50: solder bump; 60: capacitor; 100: semiconductor element; 200: semiconductor apparatus; TC: centerline of through hole 11; SS: tangent line of through hole 11 and lateral face