CLAIMS

1. A process for preparing a support substrate equipped with a charge-trapping layer, the process comprising the introduction of a single-crystal silicon base substrate having a resistivity of greater than 500 ohm.cm into a chamber of deposition equipment and, without removing the base substrate from the chamber and while flushing the chamber with a carrier gas, performing the following successive steps:

- forming a dielectric layer on an exposed face of the base substrate by introducing a reactive gas into the chamber over a first time period;
- forming a polycrystalline silicon charge-trapping layer directly on the dielectric layer by introducing a precursor gas containing silicon into the chamber over a second time period, subsequent to the first time period;

the process being characterized in that the time for which the dielectric layer is exposed only to the carrier gas, between the first time period and the second time period, is less than 30 seconds and in that the step of forming the charge-trapping layer is performed at a temperature strictly between 1010°C and 1200°C.

2. The process according to the preceding claim, in which the carrier gas comprises or consists of hydrogen.

3. The process according to either of the preceding claims, in which the precursor gas containing silicon is chosen from the list including silane, disilane, trichlorosilane, dicholorosilane and silicon tetrachloride.

4. The process according to one of the preceding claims, in which the dielectric layer is made of silicon oxide and the reactive gas comprises between 0.1% and 10% oxygen in a neutral gas such as argon.

5. The process according to one of the preceding claims, in which the step of forming the dielectric layer is performed at a temperature of between 1010°C and 1150°C.

6. The process according to one of the preceding claims, in which the dielectric layer has a thickness of greater than 0.5 nm.

7. The process according to one of the preceding claims, in which the step of forming the charge-trapping layer is performed at a temperature above 1050°C or 1100°C.

8. The process according to one of the preceding claims, in which the charge-trapping layer and the dielectric layer are formed at respective temperatures that are identical to within 50°C.

9. The process according to one of the preceding claims, in which the time for which the dielectric layer is exposed only to the carrier gas is less than 20 seconds or 15 seconds.

10. The process according to one of the preceding claims, in which the charge-trapping layer has a thickness of between 0.1 and 10 microns.