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(54) ELECTRONIC CIRCUIT

- (71) We, HITACHI, LTD., of 5-1, 1-chome, Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—
- The present invention relates to an electronic circuit including at least one insulated gate field effect transistor (hereinafter referred to as MISFET).
- In the case where an insulated gate field effect transistor is used as an amplifier element in an amplifier circuit for constructing an electronic circuit, a capacitive element externally provided at the input side of the amplifier circuit according to the circuit design of the electronic circuit, or a parasitic capacitance necessarily formed thereat tends to form a large discharging time constant circuit for voltages applied thereto, since the insulated gate field effect transistor generally has a high input impedance. On the basis of this fact, we have found that in such a circuit the bias voltage of the amplifier circuit is transiently maintained at the previous state against an abrupt variation in power voltage of the power source such as a dry battery due to the storage effect of the capacitor provided at the input side of the amplifier circuit, resulting in an incorrect output signal of the electronic circuit during a transient period. For example, in the case where the amplifier circuit is used in an oscillation circuit for an electronic watch, such a problem will now be explained in greater detail.
- A typical type of conventional complementary oscillation circuit for an electronic watch comprises a complementary MIS amplifier circuit in which a bias resistor is connected between the input and the output of a complementary inverter circuit including a N channel MISFET and a P channel MISFET. A positive feedback circuit including a quartz oscillator and two capacitors is connected between the input and the output of the amplifier circuit. One of the two capacitors is provided at the input side of the amplifier circuit and the other capacitor is provided at the output side of the amplifier circuit. An oscillation output of the oscillation circuit is coupled to a frequency divider circuit through a waveform shaping circuit. The frequency divider circuit and a gate circuit form a clock pulse signal which in turn is applied to a driving circuit to drive a pulse motor. A battery is commonly provided for the amplifier circuit, the waveform shaping circuit and the motor driving circuit.
- In the above described circuitry, a large driving current flows through the pulse motor so that the battery is exhausted or the power voltage of the battery is greatly decreased at low temperatures because of its high internal resistance.
- In response to an abrupt decrease in the power voltage, the amplifier circuit is not provided with a desirable bias voltage corresponding to the decreased power voltage, since the bias voltage of the amplifier circuit is maintained at the previous state because of a storage effect of the capacitor which is provided at the input side of the amplifier circuit. As a result, a correct oscillation output cannot be obtained.
- Such a problem of undesirable bias point caused due to the variation in power voltage also takes place commonly in MISFET amplifier circuits in case that parasitic capacitances such as gate capacitance or electrostatic capacitance between electric leads are necessarily formed at the input side of the amplifier circuit.
- An object of the present invention, therefore, is to allow a desirable shift of bias point in response to the variation in power voltage in an amplifier circuit constructed by a MISFET or MISFET's.
- Another object of the present invention is the stabilization of oscillation output

against the variation in power voltage in an oscillation circuit using such a MISFET amplifier circuit.

According to one aspect of the present invention there is provided an electronic circuit comprising an amplifier circuit including:

at least one insulated gate field effect transistor as an amplifying element having its gate connected to an input terminal of the amplifier and its drain connected to an output terminal of the amplifier;

a power voltage terminal;

an earth terminal;

a bias resistor provided between said input and output terminals; and

first and second capacitive elements series-connected between said power voltage terminal and said earth terminal, a divided voltage of a power voltage determined by said first and second capacitive elements being selected to be equal to a bias voltage supplied through said bias resistor, said divided voltage being applied to said input terminal, whereby the bias voltage will follow abrupt changes in the said power voltage.

According to a second aspect of the present invention there is provided an electronic circuit comprising an oscillation circuit including:

an amplifier circuit having at least one insulated gate field effect transistor as an amplifying element, having its gate connected to an input terminal of the amplifier and its drain connected to an output terminal of the amplifier, and a bias resistor provided between said input and output terminals;

positive feedback means for coupling an output signal of said amplifier circuit to the input side thereof, said positive feedback means having an inductive element and first and second capacitive elements provided at the input and output sides of said amplifier circuit respectively; and

a third capacitive element for dividing a power voltage in co-operation with said first capacitive element provided at the input side of said amplifier circuit, a divided voltage of said power voltage determined by a ratio between the capacitances of said first and third capacitive elements being selected to be equal to a bias voltage supplied through said bias resistor, whereby the bias voltage will follow abrupt changes in the said power voltage.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, in which:—

Figure 1 is a circuit diagram for explaining a conventional complementary MIS circuit for a watch;

Figure 2 is a graph showing an input

versus output transfer characteristic for explaining a way of determining a bias voltage;

Figure 3 is a circuit diagram showing an embodiment of complementary MIS oscillation circuit according to the present invention;

Figure 4 is a circuit diagram showing an embodiment in which the oscillation circuit of Figure 3 is applied to a complementary MIS circuit for a watch;

Figure 5 is a circuit diagram showing a circuit embodiment of complementary MIS amplifier circuit according to the present invention;

Figure 6 is a circuit diagram showing a second embodiment of an MIS amplifier circuit according to the present invention; and

Figure 7 is a graph showing an input versus output transfer characteristic for explaining a way of determining a bias voltage in the amplifier circuit of Figure 6.

Prior to describing the present invention, reference will first be made to a conventional complementary MIS circuit for a watch, a typical example of which is shown in Figure 1.

In Figure 1, an oscillation circuit 1 constituting a main part of the complementary MIS circuit for a watch comprises a complementary MIS amplifier circuit in which a bias resistor R_F is connected between the input and output of a complementary inverter circuit including a N channel MISFET Q_{N1} and a P channel MISFET Q_{P1} . Between the input and output of the amplifier circuit is provided a positive feedback circuit which includes a quartz oscillator QO and capacitors C_D and C_G . A resistor R_D is provided at the output side of the amplifier circuit for limiting an output current to make the power loss small and absorbing the variation in output current due to various factors such as the variation in power voltage.

An oscillation output of the above-constructed oscillation circuit 1 is coupled to a first input of a frequency divider circuit 3 through a complementary inverter circuit 2 which serves as a waveform shaping circuit and includes a N channel MISFET Q_{N2} and a P channel MISFET Q_{P2} . The waveform-shaped output from the inverter circuit 2 also is inverted through an inverter 1N and then applied to a second input of the frequency divider circuit 3. In co-operation of the frequency divider circuit 3 and a gate circuit 4, signal pulses are generated from two outputs of the gate circuit 4 alternately or one after the other for every second. The pulse signal drives a pulse motor M through a driving circuit 5 which includes a complementary inverter circuit constructed by a N channel MISFET Q_{N3} and a P

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channel MISFET Q_{P3} and a driving circuit 5' which includes a complementary inverter circuit constructed by a N channel MISFET Q_{N4} and a P channel MISFET Q_{P4} .

5 In the above-described MIS circuit, a large current flows through the pulse motor M when the motor is driven. As a result, a battery E is exhausted or the power voltage of the battery E is greatly decreased at low
10 temperatures because of its high internal resistance r .

The decrease in power voltage results in the following problems in the oscillation circuit 1. In the amplifier circuit
15 constituting the oscillation circuit 1, a bias point A of the amplifier circuit lies on an input versus output transfer curve I of the amplifier circuit and is defined at a point at which input and output voltages are equal
20 to each other, as shown in Figure 2. This is due to the fact that the input and output of the amplifier circuit come to the same D.C. potential. In this condition, when the power voltage $-V_{DD}$ abruptly decreases to $-V'_{DD}$ in
25 value, the input versus output characteristic of the amplifier circuit changes in accordance with the variation in power voltage, as represented by a curve I' . However, a bias voltage by the bias resistor
30 R_F is maintained at the previous state or a point A because of a storage effect of the capacitor C_G which is provided at the input side of the amplifier circuit. Therefore, the bias voltage is high in absolute value with
35 respect to a new threshold level of the amplifier circuit, so that the N channel MISFET Q_{N1} falls near to its cut-off state. Thus, the output level approaches earth potential with result that a correct or
40 normal oscillation output is unobtainable. Of course the bias voltage is changed to a normal bias point A' on the new input versus output characteristic curve I' after a predetermined time interval determined by
45 the bias resistor R_F .

It should be appreciated that the above-described abnormal oscillation output upon the variation in power voltage, for example,
50 when the pulse motor is driven, provides a possibility that time lag may occur in the MIS circuit for the watch.

The problem of an undesirable bias point due to the variation in power voltage also takes place commonly in MISFET
55 amplifier circuits generally constructed by semiconductor integrated circuits, in the case where parasitic capacitances such as gate capacitance or electrostatic capacitance between electric leads are necessarily formed at the input side of the
60 amplifier circuit.

The above problems can be overcome by the present invention. Preferred embodiments of the present invention will

be now explained with respect to Figures 3 to 7.

In Figure 3 showing a circuit diagram of an embodiment of complementary MIS oscillation circuit to which the present invention is applied, the oscillation circuit
70 constitutes a complementary MIS amplifier circuit in which a bias resistor R_F is connected between the input and output terminals of an inverter circuit including a N channel MISFET Q_N and a P channel
75 MISFET Q_P . A positive feedback circuit including a quartz oscillator QO and capacitors C_D and C_G' is connected between the input terminal of the amplifier circuit and one end of a resistor R_D the
80 other end of which is connected to the output terminal OUT of the amplifier circuit. The quartz oscillator is used as an inductive element to form an oscillation circuit. An inductor may be employed
85 instead of the quartz oscillator. In such a complementary MIS oscillation circuit, a capacitor C_G'' having substantially the same capacitance as the capacitor C_G' is connected between a power source
90 terminal $-V_{DD}$ and the input terminal. The condition of $C_G''=C_G'$ is established in order to make a divided voltage of the power voltage determined by the capacitors C_G'' and C_G' equal to an input bias voltage
95 which is determined by the bias resistor R_F and substantially becomes $-V_{DD}/2$. For a correct oscillation condition, it should be appreciated that each of the capacitances of the capacitors C_G'' and C_G' is established
100 to be equal to a half of the capacitance at the input side of the oscillation circuit 1 of Figure 1, i.e. the capacitor C_G .

In the oscillation circuit with the above-described construction according to the
105 present invention, the capacitors provided at the input side of the amplifier circuit form a series circuit between the power source terminal and earth so that these capacitors exhibit no storage effect with
110 respect to the variation in power voltage and therefore follow this variation. Thus, the bias voltage is not subjected to the influence of the input side capacitors, thereby preventing the occurrence of
115 abnormal oscillation output.

Figure 4 shows an embodiment of complementary MIS circuit for a watch to which the oscillation circuit of Figure 3 is applied. In Figures 1, 3 and 4, similar circuit
120 components have similar reference numerals or symbols. A complementary MIS circuit for a watch is subjected to the variation in power voltage upon the driving of a pulse motor, as has been explained with
125 respect to Figure 1. However, the oscillation output of the oscillation circuit 1 of Figure 4 is not influenced by the variation in power voltage so that a stable

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oscillation output can be provided to drive the pulse motor M. As a result, a problem such as time lag is eliminated.

5 Figure 5 shows an embodiment of complementary MIS amplifier circuit to which the present invention is applied. In the amplifier circuit, capacitors C_{G1} and C_{G2} having substantially the same capacitance are provided at the power source and earth sides respectively. The capacitor C_{G2} at the earth side may be a parasitic capacitance. In this amplifier circuit, the bias voltage follows the variation in input versus output transfer characteristic resulting from the variation in power voltage, for the same reason as has been described earlier. As a result, the A.C. amplification output is stable.

20 Figure 6 shows an embodiment of another MIS amplifier circuit to which the present invention is applied. This MIS amplifier circuit comprises an inverter circuit including a P channel MISFET and a load resistor R_L . A resistor R_F is connected between the input terminal IN and output terminal OUT of the inverter circuit. The input versus output transfer characteristic of this MIS amplifier circuit is shown in Figure 7. As apparent from the figure, the characteristic curve 1 is different from the characteristic curves of a complementary MIS amplifier circuit and the bias voltage V_G determined by the bias resistor R_F is not equal to $-V_{DD}/2$. The bias voltage V_G lies on the characteristic curve 1 and is defined as being at a point at which the input voltage is equal to the output voltage. Therefore, a divided voltage of a power voltage determined by a ratio between the capacitances of the capacitors C_{G1} and C_{G2} is selected to be equal to the bias voltage V_G .

As has been described, the present invention is widely applicable to complementary MIS oscillation circuits as well as amplifier circuits in which at least one MISFET is used as an amplifying element and a bias resistor is provided between input and output sides.

50 WHAT WE CLAIM IS:—

1. An electronic circuit comprising an amplifier circuit including:
at least one insulated gate field effect transistor as an amplifying element having its gate connected to an input terminal of the amplifier and its drain connected to an output terminal of the amplifier;

a power voltage terminal;
an earth terminal;
a bias resistor provided between said input and output terminals; and
first and second capacitive elements series-connected between said power voltage terminal and said earth terminal, a divided voltage of a power voltage determined by said first and second capacitive elements being selected to be equal to a bias voltage supplied through said bias resistor, said divided voltage being applied to said input terminal, whereby the bias voltage will follow abrupt changes in the said power voltage.

2. An electronic circuit comprising an oscillation circuit including:

an amplifier circuit having at least one insulated gate field effect transistor as an amplifying element, having its gate connected to an input terminal of the amplifier and its drain connected to an output terminal of the amplifier, and a bias resistor provided between said input and output terminals;

positive feedback means for coupling an output signal of said amplifier circuit to the input side thereof, said positive feedback means having an inductive element and first and second capacitive elements provided at the input and output sides of said amplifier circuit respectively; and

a third capacitive element for dividing a power voltage in co-operation with said first capacitive element provided at the input side of said amplifier circuit, a divided voltage of said power voltage determined by a ratio between the capacitances of said first and third capacitive elements being selected to be equal to a bias voltage supplied through said bias resistor, whereby the bias voltage will follow abrupt changes in the said power voltage.

3. An electronic circuit according to Claim 2, wherein the capacitance of said third capacitive element is defined in a manner that the total capacitance of said first and third capacitive elements is equal to a predetermined capacitance of a capacitive element to be provided at said input side of said amplifier circuit to obtain a predetermined oscillating frequency in said oscillation circuit.

4. An electronic circuit according to Claim 2, wherein the capacitance of said third capacitive element is defined so as to obtain a predetermined oscillating

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oscillation output can be provided to drive the pulse motor M. As a result, a problem such as time lag is eliminated.

Figure 5 shows an embodiment of complementary MIS amplifier circuit to which the present invention is applied. In the amplifier circuit, capacitors C_{G1} and C_{G2} having substantially the same capacitance are provided at the power source and earth sides respectively. The capacitor C_{G2} at the earth side may be a parasitic capacitance. In this amplifier circuit, the bias voltage follows the variation in input versus output transfer characteristic resulting from the variation in power voltage, for the same reason as has been described earlier. As a result, the A.C. amplification output is stable.

Figure 6 shows an embodiment of another MIS amplifier circuit to which the present invention is applied. This MIS amplifier circuit comprises an inverter circuit including a P channel MISFET and a load resistor R_L . A resistor R_F is connected between the input terminal IN and output terminal OUT of the inverter circuit. The input versus output transfer characteristic of this MIS amplifier circuit is shown in Figure 7. As apparent from the figure, the characteristic curve I is different from the characteristic curves of a complementary MIS amplifier circuit and the bias voltage V_G determined by the bias resistor R_F is not equal to $-V_{DD}/2$. The bias voltage V_G lies on the characteristic curve I and is defined as being at a point at which the input voltage is equal to the output voltage. Therefore, a divided voltage of a power voltage determined by a ratio between the capacitances of the capacitors C_{G1} and C_{G2} is selected to be equal to the bias voltage V_G .

As has been described, the present invention is widely applicable to complementary MIS oscillation circuits as well as amplifier circuits in which at least one MISFET is used as an amplifying element and a bias resistor is provided between input and output sides.

WHAT WE CLAIM IS:—

1. An electronic circuit comprising an amplifier circuit including:
at least one insulated gate field effect transistor as an amplifying element having its gate connected to an input terminal of the amplifier and its drain connected to an output terminal of the amplifier;

a power voltage terminal;

an earth terminal;

a bias resistor provided between said input and output terminals; and

first and second capacitive elements series-connected between said power voltage terminal and said earth terminal, a divided voltage of a power voltage determined by said first and second capacitive elements being selected to be equal to a bias voltage supplied through said bias resistor, said divided voltage being applied to said input terminal, whereby the bias voltage will follow abrupt changes in the said power voltage.

2. An electronic circuit comprising an oscillation circuit including:

an amplifier circuit having at least one insulated gate field effect transistor as an amplifying element, having its gate connected to an input terminal of the amplifier and its drain connected to an output terminal of the amplifier, and a bias resistor provided between said input and output terminals;

positive feedback means for coupling an output signal of said amplifier circuit to the input side thereof, said positive feedback means having an inductive element and first and second capacitive elements provided at the input and output sides of said amplifier circuit respectively; and

a third capacitive element for dividing a power voltage in co-operation with said first capacitive element provided at the input side of said amplifier circuit, a divided voltage of said power voltage determined by a ratio between the capacitances of said first and third capacitive elements being selected to be equal to a bias voltage supplied through said bias resistor, whereby the bias voltage will follow abrupt changes in the said power voltage.

3. An electronic circuit according to Claim 2, wherein the capacitance of said third capacitive element is defined in a manner that the total capacitance of said first and third capacitive elements is equal to a predetermined capacitance of a capacitive element to be provided at said input side of said amplifier circuit to obtain a predetermined oscillating frequency in said oscillation circuit.

4. An electronic circuit according to Claim 2, wherein the capacitance of said third capacitive element is defined so as to obtain a predetermined oscillating

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frequency in said oscillation circuit in co-operation with said first capacitive element.

- 5 An electronic circuit constructed substantially as herein described, with reference to Figure 3, or Figure 5, or Figure 6 of the accompanying drawings.

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