CLAIMS

1. A method of forming a semiconductor structure, the method comprising:

forming a first recessed region in a semiconductor structure, the first recessed region defining a first opening with a first positive tapering profile, as at least part of the first positive tapering profile, widening the first opening in a direction towards a top source/drain region of the semiconductor structure at a first tapering angle;

forming a top source/drain contact within the first opening, the top source/drain contact surrounding a surface of the top source/drain region; and

forming a protective liner in direct contact with a bottom portion of the top source/drain region at an interface between the bottom portion of the top source/drain region, a top spacer adjacent to the top source/drain region and a second dielectric material between two consecutive top source/drain regions.

2. The method of claim 1, further comprising:

forming a second recessed region comprising a second opening with a first negative tapering profile, the first negative tapering profile comprising a second tapering angle narrowing in a direction towards a bottom source/drain region of the semiconductor structure; and

forming a bottom source/drain contact within the second recessed region.

3. The method of claim 1, further comprising:

forming a third recessed region comprising a third opening with a second negative tapering profile, the second negative tapering profile comprising a third tapering angle narrowing in a direction towards a high-k metal gate stack; and

forming a gate contact within the third recessed region.

4. The method of claim 1, wherein forming the protective liner in direct contact with the bottom portion of the top source/drain region further comprises:

recessing a first interlevel dielectric layer to expose a top portion of the top source/drain region and top portions of the top spacer adjacent to the top source/drain region;

selectively removing the exposed top portions of the top spacer; and

conformally depositing the protective liner above and in direct contact with the top source/drain region.

5. The method of claim 4, wherein recessing the first interlevel dielectric layer is performed using a high selectivity blanket atomic layer etching.

6. The method of claim 1, further comprising:

depositing a sacrificial material above the protective liner;

depositing an organic planarization layer above the sacrificial material; and

recessing the organic planarization layer, the sacrificial material, the protective liner and a top portion of a

first interlevel dielectric layer, wherein the recessing creates a plurality of recesses with different tapering profiles for contact formation.

7. The method of claim 1, wherein the protective liner comprises titanium nitride.

8. A semiconductor structure comprising:

a first region comprising a first positive tapering profile, the first positive tapering profile comprising a first tapering angle widening in a direction towards a top source/drain region of the semiconductor structure;

a top source/drain contact within the first region, the top source/drain contact surrounding a surface of the top source/drain region; and

a protective liner in direct contact with a bottom portion of the top source/drain region at an interface between the bottom portion of the top source/drain region, a top spacer adjacent to the top source/drain region and a second dielectric material located between two consecutive top source/drain regions.

9. The semiconductor structure of claim 8, further comprising:

a second region comprising a first negative tapering profile, the first negative tapering profile comprising a second tapering angle narrowing in a direction towards a bottom source/drain region of the semiconductor structure; and

a bottom source/drain contact within the second region.

10. The semiconductor structure of claim 8, further comprising:

a third region comprising a second negative tapering profile, the second negative tapering profile comprising a third tapering angle narrowing in a direction towards a high-k metal gate stack; and

a gate contact within the third region.

11. The semiconductor structure of claim 8, wherein the protective liner comprises titanium nitride.