A MOSFET WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR AND MINIMUM OVERLAP CAPACITANCE

ABSTRACT

Methods of fabricating metal oxide semiconductor field effect transistor (MOSFET) devices having a high dielectric constant (k greater than 7) gate insulator (26), low overlap capacitance (0.35 fF/μm or below) and a channel length (sub-lithographic, e.g., 0.1 μm or less) that is shorter than the lithography-defined gate lengths are provided. The methods include a damascene processing step and a chemical oxide removal (COR) step. The COR step produces a large taper on a pad oxide layer (14) which, when combined with a high-k gate insulator (26), results in low overlap capacitance, sort channel lengths and better device performance as compared to MOSFET devices that are formed using conventional Complimentary Metal Oxide Semiconductor (CMOS) technologies.

Fig. 1E