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PATENT SPECIFICATION

DRAWINGS ATTACHED

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Int. Cl.: —H 01 I 1/14

COMPLETE SPECIFICATION

Semiconductor Devices, Integrated Circuits and Methods for Making Same

5 We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Express-
10 way, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be per-
15 formed, to be particularly described in and by the following statement:—

This invention relates to semiconductor de-
vices, including integrated circuits and to
20 methods for making same. More particularly it relates to integrated circuit devices which
25 use the ambient fabrication atmosphere as an isolation medium between elements of the circuit

In a high frequency integrated circuit it
is desirable to electrically isolate various com-
20 ponents of the circuit by some means which produces a lower capacitive coupling be-
25 tween them than that afforded by the conven- tional PN junction isolation. PN junction
isolation is achieved by the use of the high
30 resistance, reverse-bias characteristics of such a junction, said junction being physically
located between the elements to be isolated. There are two common ways of building a
35 PN junction isolation region, namely, that of using a diffused collector region and that
of using an epitaxial collector region. Be-
cause the reverse biased PN junction can
40 only be used up to a voltage which is deter- mined by the impurity concentrations at the
collector-isolation junction, both of these
methods produce devices which are voltage
limited in operation. In order to make a
transistor having a low collector saturation
resistance (Rcs), it is necessary to have a
high surface impurity concentration. This
high impurity concentration causes the con-
comitant PN isolation junction breakdown

voltage to be low. Thus the conventional PN
junction isolation makes it quite difficult to
fabricate a device having both high voltage
breakdown and low Rcs characteristics. 45

A second disadvantage of PN junction iso-
lation is the capacitive coupling which, exist-
ing between isolated regions and the sub-
strate, seriously impairs the ability of the de-
vice to operate at the higher frequencies. 50

There is also a problem in controlling the
PNPN action of the active PN junction,
such as in a transistor or diode, coupled with
the isolation PN junction. This problem can
55 be lessened somewhat by introducing a second
epitaxial layer which is, for example, highly
N-doped for the case of P-type substrate.
This solution is nonetheless plagued with the
same problem of attempting to fabricate a
60 low Rcs, high collector-base breakdown vol-
tage device.

As integrated circuit technology advances,
additional active and passive elements are be-
ing crowded into monolithic semiconductor
65 networks, increasing the number of elements
thereon, and placing them into progressively
smaller spaces. The necessary reduction in
the size of the elements presents a serious
70 problem when attempting to make internal
connections between the elements and exter-
nal connections thereto. A technique to make
these connections has been previously de-
veloped for making a solid package wherein
75 the bonding of jumper wires is rendered un-
necessary by constructing a multilayer lead
device with interconnections in thin layers
and insulated from the other layers by an
insulating material. In this manner, larger
80 contact areas are provided for making ex-
ternal connections to the devices of the net-
work.

Beam lead techniques using thick leads
for mechanical support have been developed

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Price 5s. 0d.

which utilize air insulation between the components. However, such techniques do not lend themselves to the aforescribed multilayer lead system because of the thickness of the leads.

5 The present invention provides a method for fabricating an integrated electrical network which uses the ambient fabrication atmosphere (air, for example) as the insulation medium separating the elements of the network and which has an improved mechanical structure.

10 According to the present invention an integrated electrical network includes a plurality of electrically interconnected, discrete, spaced semiconductor bodies each having one surface attached to the same plane surface of an insulating support member. Each semiconductor body defines a semiconductor circuit component and includes at least one region of predetermined conductivity-type extending to the said one surface of the body, which region is ohmically attached to a metallic contact sandwiched between the said one surface of the body and the support member. Each metallic contact is electrically insulated from the remainder of the said one surface of the body and an ohmic attachment between an electrical lead and at least one of the contacts is made at the surface of the contact adjacent the semiconductor body. The circuit components can include active and/or passive components formed by regions of suitable conductivity-type formed in the bodies and extending to the said one surface thereof.

35 The components can be electrically interconnected to provide desired circuit functions. Interconnections may be achieved by having one or more of the metallic contacts directly attached to at least two of the semiconductor bodies and/or by the electrical leads. The electrical leads can be attached directly to the metallic contacts or attachment can be effected by a further body of semiconductor material having one surface attached both to the support member and to the metallic contact, the electrical lead being ohmically attached to an opposite surface of the further body.

50 Such an integrated electrical network uses the ambient atmosphere, e.g. air, as the isolation medium between the elements of the network; the construction is compatible with multilayer interconnection lead techniques and provides a sound mechanical structure.

55 The invention is also applicable to discrete semiconductor devices, for example transistors. Transistors are often manufactured in such manner as to place the collector surface of the device in contact with a header member and in a planar diffused device the emitter and base regions are exposed to view from the surface opposite that of the collector surface. This type of fabrication results in the relatively small emitter and

base regions being embedded in a collector region which is relatively thick and has a large area. Because the area of the collector is large, there is a large stray capacitance between the collector and the can (cap or lid) of the device, such capacitance being usually undesirable in high frequency applications. Such a structure also places a limitation on how small a semiconductor device can be built, since the collector region is always larger than that portion of the collector which is used in the transistor action. These limitations are also true in relation to semiconductor devices other than transistors, e.g. capacitors, diodes, and field-effect transistors. The present invention provides a semiconductor device comprising a body of semiconductor material including a region of predetermined conductivity-type extending to one surface of the body and a metallic contact overlying the said one surface of the body; the said region is ohmically attached to one surface of the metallic contact and an electrical lead is ohmically attached to the same surface of the contact, the contact otherwise being electrically insulated from the semiconductor body. An electrically insulating support is disposed on the opposite surface of the contact and is attached to the semiconductor body. The electrical lead can be attached directly to the metallic contact or the attachment can be effected by a further body of semiconductor material having one surface attached both to the support member and to the contact, the electrical lead then being ohmically attached to an opposite surface of the further body.

70 The invention also provides methods of manufacturing or fabricating semiconductor devices or integrated networks. A method of fabricating a semiconductor device, in accordance with the invention, comprises the steps of forming in a body of semiconductor material at least one region of predetermined conductivity-type extending to one surface of the body and covering that surface with a layer of insulating material having an aperture exposing the said region. A metallic contact is deposited to make ohmic connection with the said region through the aperture and to extend over the insulating layer. An insulating support is attached to the body to sandwich the insulating layer and the contact between the semiconductor body and the support and an electrical lead is ohmically attached to the surface of the contact more remote from the support member. In carrying out this method, concurrently with the removal of semiconductor material from the semiconductor body, a portion of the insulating material can be removed to expose the metallic contact for ohmically connecting the electrical lead thereto. Alternatively, the predetermined conductivity-type region can be formed in a body of semiconductor material

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having the same conductivity-type but a higher conductivity, the insulating layer then having at least one further aperture exposing a higher conductivity area of the body. One of the metallic contacts that extends over the insulating layer to make ohmic contact with the higher conductivity portion of the body through this further aperture and to make contact with the said region of predetermined conductivity-type. Removal of part of the semiconductor body then leaves the said higher conductivity portion in the form of an island and an electrical lead is connected to the higher conductivity island on a surface thereof remote from the support member.

By way of example, the invention will be described in greater detail with reference to the accompanying drawings in which:—

Figure 1 illustrates a sectional view of a conventional semiconductor device having two transistors diffused therein;

Figure 2 illustrates an inverted sectional view of the device of Figure 1 partially fabricated according to the invention;

Figure 3 illustrates two semiconductor devices fabricated according to the invention;

Figure 4(a) is a conventional diagram of a circuit capable of being fabricated as an integrated circuit device according to the invention;

Figure 4(b) illustrates a plan view of a diffused transistor which can be used in the circuit of Figure 4(a);

Figure 4(c) illustrates a plan view of a diffused resistor which can be used in the circuit of Figure 4(a);

Figure 5 illustrates an integrated circuit device embodying the circuit of Figure 4(a);

Figure 6 illustrates a sectional view of a semiconductor wafer having a vapor-etched and redeposited semiconductor region therein;

Figure 7 illustrates a sectional view of the wafer of Figure 6 having diffused base and emitter regions in the redeposited region;

Figure 8 illustrates a sectional view of the device of Figure 6 mounted upon insulating substrate and inverted;

Figure 9 illustrates a sectional view of the mounted device of Figure 8 having etched out regions therein according to the invention;

Figure 10 illustrates a pictorial view of the device of Figure 9;

Figure 11 illustrates a schematic representation of a simple circuit easily adaptable to integrated circuit fabrication processes according to the invention; and

Figure 12 illustrates a pictorial view of an integrated circuit fabricated according to the invention embodying the circuit of Figure 11.

For a more detailed description, with specific reference to Figure 1, there is shown a semiconductor wafer 1 comprised of lightly doped N type epitaxial silicon an N+ sili-

con substrate by way of example, into which a pair of NPN transistors 2 and 8 have been diffused by conventional planar diffusions utilizing standard photoresist and silicon oxide masking techniques. Transistor 2 is comprised of a collector 3, a diffused base 4 and a diffused emitter 5, while transistor 8 is comprised of a collector 9, a base 10, and emitter 11. A variation from the double-diffused epitaxial collector devices illustrated includes the use of intrinsic or P type instead of N or N+ epitaxial, along with triple diffusion to make NPN devices. Intrinsic or P type substrate material is used in this latter technique to provide an insulation medium between components by the junctions or the intrinsic material but such a medium is unnecessary in this invention due to the etching step which provides isolation by removing the material between the components. When N or N+ silicon is used for the wafer 1, the wafer is then the collector and only a base and an emitter diffusion will be necessary. Subsequent to the base and emitter diffusions, metallized base 7 and emitter 29 contacts are applied to transistor 2, and metallized base 30 and emitter 31 contacts are applied to transistor 8, the contacts being applied by evaporation, sputtering or the like. The silicon oxide mask 6 provides a conventional means of selectively depositing the metallized contacts onto the emitter and base regions of the two transistors.

It will be appreciated that while the device of Figure 1 has been illustrated as comprising two transistors diffused into a semiconductor wafer, this has been done for the sake of simplicity in pointing out the salient features of the invention as further illustrated in Figures 2, 3, 4(a—c) and 5. While the preferred embodiment comprises a semiconductor wafer of silicon, in which NPN transistors are formed by diffusion, it is obvious that the wafer and transistors are merely illustrative and are in no sense meant to be construed as a limitation upon the invention. Likewise, as is obvious, in order to build a single semiconductor device such as a transistor, only one such transistor would be diffused into the wafer. Thus the wafer could be N or P type silicon, germanium, or any other available semiconductor material and the transistors could be any number (not limited to two) and any combination of NPN and PNP devices. There could also be resistors (as shown in Figure 4(a—c) and capacitors (not shown) in the circuit, all or any of which are to be construed as being within the scope of the invention as defined in the appended claims.

With reference to Figure 2, the device of Figure 1 is inverted and mounted on a ceramic substrate 12, utilizing an insulating adhesive material (not illustrated) such as cement, glass or epoxy to cause one surface of the device to be adhered to the substrate.

Alternatively, the insulating material 12 could be deposited onto the silicon wafer, such as by deposition of a thick layer of silica. The opposite or top surface is then lapped or etched evenly down to a thickness of perhaps 1 mil removing part of the N+ material to simplify the subsequent selective etching. Then gold or gold over molybdenum is evaporated onto the top surface and selectively removed except over what will later be mesa tops, leaving gold contacts 27 and 28. The top surface is then selectively masked by photoresist methods to leave the developed photoresist areas 13 and 14 as masks against the subsequent etching operation. Of course, the masking process step could be performed prior to mounting the device upon the substrate. A selective etchant, such as CP8 by way of example, described in "Transistor Technology," Vol. 2, edited by F. J. Biondi, at page 598, is applied to the masked surface to remove the semiconductor material 15, 16 and 17, and portions of the oxide layer 6 (shown as 18, 19 and 20) to thus lay bare portions of the metallized contact regions 7, 29, 30 and 31.

As shown in Figure 3, the portions of the silicon wafer which were not removed by the etch are now mesa-shaped, with collector contacts 27 and 28 on top. Collector leads 22 and 25 are then respectively attached to these contacts, as by ball bonding. Likewise, the emitter and base leads 23 and 21 on the one transistor 2 and 24 and 26 on the other transistor 8, are ball bonded, to thereby result in a device having two transistors with all necessary leads, a strong mechanical structure, and air-isolation between the transistors.

Figures 4(b) and 4(c), respectively, illustrate an underside view of transistor 42 and resistor 38, both of which are further illustrated in Figure 4(a) and Figure 5. Such an underside view is to clarify the bottom side of the pyramid-appearing structure pictorially illustrated in Figure 5. In Figure 4(b), transistor 42 is comprised of a collector region 48 formed in the intrinsic region 47, a base region 49 and an emitter region 53. To these regions are secured metallized contacts, illustrated as collector contact 52, base contact 50 and emitter contact 51. The small square 54 represents a region removed from the silicon oxide (not shown) through which the metallized contact makes an electrical connection to the semiconductor region. In Figure 4(c), resistor 38 is comprised of a region 46 of semiconductor material, either P or N type, formed in the intrinsic material 44. Metallized contacts 36 and 37 are secured to opposite ends of the region 46 through the holes 45 in the silicon oxide (not shown).

As illustrated in Figure 5, a simple circuit, such as shown in Figure 4(a), comprised of two transistors and two resistors, is produced in a semiconductor wafer in a similar manner

as was done in Figure 1 with the transistors, except that the resistors 38 and 41 normally require only one diffusion step and have no rectifying junctions. Of course, a different conductivity type than that of the resistors could be diffused around each or both of them, much as is done in the conventional PN junction isolation resistor diffusion processes, but such is not necessary in the present embodiment of the invention. Figure 4(a) schematically shows such a circuit, admittedly simple, made so in order to illustrate an operative circuit which utilizes the invention. Figure 5 shows the resistors 38 and 41, with their respective metallized contacts. It likewise illustrates the transistors 42 and 43, along with the interconnections necessary to complete the circuit of Figure 4(a). All of the external leads shown (33, 32, 35 and 34) make ohmic contact to the metallized contacts of the circuit elements, as do the interconnecting metallized regions, all of which may be done by any conventional technique, such as by ball bonding. Substrate 12, of some material such as is described in reference to the substrate 12 of Figure 2, can then be mounted on a suitable header (not shown) to result in a packaged device.

A further aspect of the invention to be described with reference to Figs. 6-10 utilizes one or more "islands" of high conductivity semiconductor material between the metallized contacts which are in intimate relationship with the active semiconductor regions of a given device and the metallic pads to which lead wires may be attached.

In Figure 6, there is shown a semiconductor wafer 101, for example, highly doped N type (commonly referred to as N+) silicon, having an oxide layer 102. By conventional selective masking and etching processes a portion of the layer 102 is removed and a region of the wafer 101 is then vapor etched to leave a cavity, not illustrated. Subsequent to the vapor etching step the cavity is filled with a less highly doped N type silicon material 103 by a conventional redeposition process.

Figure 7 illustrates how a transistor is formed in the collector region 103, having a conventional diffused base region 104 and a conventional emitter region 105, both of the diffused regions being the result of conventional photomasking and diffusion processes well-known in the semiconductor industry. Metallized contacts 106 and 107 are then applied by conventional evaporation processes to the emitter region 105 and the base region 104, respectively. The contact region 107 also extends through the oxide layer 102 to form a contact 108 with the N+ region 101, while the contact region 106 extends through the oxide layer 102 to form a contact 109 with the N+ region 101.

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vice of Figure 7 has been illustrated as comprising one transistor diffused into a semiconductor wafer, this has been done for the sake of simplicity in pointing out the salient features of the invention as further illustrated in Figure 11 and 12. While the preferred embodiment comprises a semiconductor wafer of silicon, into which a silicon NPN transistor is diffused, it is obvious that the wafer and transistor are merely illustrative and are in no sense meant to be construed as a limitation upon the invention. Thus the wafer could be N or P type silicon, germanium or any other available semiconductor material and the transistors could be any number (not limited to one) and any combination of NPN and PNP devices all interconnected as a circuit. There could also be resistors (as shown in Figure 11 and 12) and capacitors (not shown) in the circuit, all or any of which are to be construed as being within the scope of the invention as defined in the appended claims.

With reference to Figure 8, the device of Figure 7 is inverted and mounted to a ceramic substrate 111, utilizing an insulating adhesive material 110 such as cement, glass or epoxy, to cause one surface of the device to adhere to the substrate. Alternatively, the insulating material 111 could be deposited onto the silicon wafer, such as by deposition of a thick layer of quartz. The opposite or top, surface 101 is then lapped or etched away down to a thickness of perhaps 1 mil, removing part 101' of the N+ material to simplify the subsequent selective etching. Gold or gold over molybdenum is then evaporated onto the top surface and selectively removed except over what will later be mesa tops, leaving gold contacts 115, 116 and 117. The opposite or top surface is then selectively masked by photoresist methods against the subsequent etching operation. Of course, the masking process step could be performed prior to mounting the device upon the substrate. A selective etchant, such as CP8 by way of example, described in "Transistor Technology," Vol. 2, edited by F. J. Biondi, at page 598, is applied to the masked surface to remove the semiconductor material 101 between the "islands" 112, 113 and 114, as illustrated in Figure 9.

As shown in Figures 9 and 10, the "islands" of the silicon wafer 101 which were not removed by the etch are now mesa-shaped, with metallized contacts 115, 116 and 117 on top. External leads 118, 119 and 120 are then respectively attached to these contacts, as by ball bonding, thereby to produce a device having a transistor with all necessary leads, a strong mechanical structure, air-isolation between elements of the transistor, and a reduced collector area with its resulting lower stray capacitance.

As illustrated in Figure 12, a simple cir-

cuit, such as shown in Figure 11, comprising two transistors 123 and 124 and two resistors 121 and 122, is produced in a semiconductor wafer in a similar manner as described for the one transistor shown in Figure 9, except that the resistors 121 and 122 normally require only one diffusion step and have no rectifying junctions. Of course, a different conductivity type than that of the resistors could be diffused around each or both of them, as is done in the conventional PN junction isolation resistor diffusion processes. But such is not necessary in the present embodiment of the invention. Figure 11 schematically shows such a circuit, admittedly simple, made so in order to illustrate an operative circuit which utilizes the invention. Figure 12 shows the resistors 121 and 122, with their respective metallized contacts. It likewise illustrates the transistors 123 and 124, along with the interconnections necessary to complete the circuit of Figure 11. It should be appreciated that, as with a single transistor, the transistors of this circuit have a reduced collector region and a lesser capacitance. All of the external leads 129, 130, 131 and 132 make ohmic contact to the metallized contacts of the circuit elements, as do the interconnecting metallized regions, all of which may be done by any conventional technique, such as by ball bonding. Substrate 133 of some material such as is described in reference to the substrate 111 of Figure 9, can then be mounted on a suitable header (not shown) to result in a packaged device.

The circuit devices of Figs. 5 and 12 have been illustrated as embodying the invention but the actual circuits shown in Figs. 4a and 12 are merely shown and described to illustrate a specific example of a large number of circuits which could be embodied in an integrated circuit device fabricated according to the invention.

Although the invention has been described in a simplified form with respect to a small wafer that involves only the isolation of a few elements, it will be appreciated that the invention is equally applicable to more complicated configurations wherein a larger multiplicity of elements are to be isolated within a single unit.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a body of semiconductor material including a region of predetermined conductivity type extending to one surface of the body, a metallic contact overlying the said one surface of the semiconductor body, the said region being ohmically attached to one surface of the contact and an electrical lead being ohmically attached to the same surface of the contact, the contact otherwise being electrically insulated from the semiconductor body, and an electrically insulating support disposed on the



vice of Figure 7 has been illustrated as comprising one transistor diffused into a semiconductor wafer, this has been done for the sake of simplicity in pointing out the salient features of the invention as further illustrated in Figure 11 and 12. While the preferred embodiment comprises a semiconductor wafer of silicon, into which a silicon NPN transistor is diffused, it is obvious that the wafer and transistor are merely illustrative and are in no sense meant to be construed as a limitation upon the invention. Thus the wafer could be N or P type silicon, germanium or any other available semiconductor material and the transistors could be any number (not limited to one) and any combination of NPN and PNP devices all interconnected as a circuit. There could also be resistors (as shown in Figure 11 and 12) and capacitors (not shown) in the circuit, all or any of which are to be construed as being within the scope of the invention as defined in the appended claims.

With reference to Figure 8, the device of Figure 7 is inverted and mounted to a ceramic substrate 111, utilizing an insulating adhesive material 110 such as cement, glass or epoxy, to cause one surface of the device to adhere to the substrate. Alternatively, the insulating material 111 could be deposited onto the silicon wafer, such as by deposition of a thick layer of quartz. The opposite or top, surface 101 is then lapped or etched away down to a thickness of perhaps 1 mil, removing part 101' of the N+ material to simplify the subsequent selective etching. Gold or gold over molybdenum is then evaporated onto the top surface and selectively removed except over what will later be mesa tops, leaving gold contacts 115, 116 and 117. The opposite or top surface is then selectively masked by photoresist methods against the subsequent etching operation. Of course, the masking process step could be performed prior to mounting the device upon the substrate. A selective etchant, such as CP8 by way of example, described in "Transistor Technology," Vol. 2, edited by F. J. Biondi, at page 598, is applied to the masked surface to remove the semiconductor material 101 between the "islands" 112, 113 and 114, as illustrated in Figure 9.

As shown in Figures 9 and 10, the "islands" of the silicon wafer 101 which were not removed by the etch are now mesa-shaped, with metallized contacts 115, 116 and 117 on top. External leads 118, 119 and 120 are then respectively attached to these contacts, as by ball bonding, thereby to produce a device having a transistor with all necessary leads, a strong mechanical structure, air-isolation between elements of the transistor, and a reduced collector area with its resulting lower stray capacitance.

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The circuit devices of Figs. 5 and 12 have been illustrated as embodying the invention but the actual circuits shown in Figs. 4a and 12 are merely shown and described to illustrate a specific example of a large number of circuits which could be embodied in an integrated circuit device fabricated according to the invention.

Although the invention has been described in a simplified form with respect to a small wafer that involves only the isolation of a few elements, it will be appreciated that the invention is equally applicable to more complicated configurations wherein a larger multiplicity of elements are to be isolated within a single unit.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a body of semiconductor material including a region of predetermined conductivity type extending to one surface of the body, a metallic contact overlying the said one surface of the semiconductor body, the said region being ohmically attached to one surface of the contact and an electrical lead being ohmically attached to the same surface of the contact, the contact otherwise being electrically insulated from the semiconductor body, and an electrically insulating support disposed on the



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opposite surface of the contact and attached to the semiconductor body.

2. A device according to Claim 1, in which the body includes a plurality of regions each of predetermined conductivity type and extending to the same one surface of the body, a plurality of metallic contacts overlying the said one surface, one of the said regions and an electrical lead being ohmically attached to one of the contacts at spaced locations on the same surface of the contact, another one of the said regions and another electrical lead being ohmically attached to another one of the contacts at spaced locations on the same surface of that contact, the contacts otherwise being electrically insulated from the semiconductor body, and the insulating support being disposed adjacent the surfaces of the said contacts opposite to the surfaces to which the regions and the electrical leads are attached.

3. A device according to Claim 1, in which the semiconductor body comprises a base region, an emitter region in the base region and a collector region surrounding the base region, the base, emitter and collector regions each extending to the same surface of the body and defining emitter-base, and collector-base pn junctions extending to that surface of the semiconductor body, and a further region of the same conductivity as and of higher conductivity than the collector region, the further region extending to the opposite surface of the semiconductor body, metallic contacts overlying the said one surface of the body, the base region and an electrical lead being ohmically attached at spaced locations to the same surface of one contact, the emitter region and an electrical lead being ohmically attached at spaced locations to the same surface of another contact, the contacts otherwise being electrically insulated from the semiconductor body and in which insulating support is disposed adjacent the opposite surfaces of the metallic contacts, and an ohmic collector connection attached to the further region of the semiconductor body at the said opposite surface of the semiconductor body.

4. An integrated electrical network having a plurality of electrically interconnected circuit elements including discrete, spaced semiconductor bodies each having one surface attached to the same plane surface of an insulating support member, each semiconductor body defining a semiconductor component and including at least one region of predetermined conductivity type extending to the said one surface thereof and ohmically attached to a metallic contact sandwiched between the said one surface of the body and the support member, each metallic contact being electrically insulated from the remainder of the said one surface of the body, and an ohmic attachment between an electrical lead and at least

one of the contacts at the surface of the said contact adjacent the semiconductor body.

5. A network according to Claim 4, in which the said one surface of at least one of the metallic contacts is ohmically attached to two of the semiconductor bodies.

6. A device according to any one of Claims 1—3 or a network according to Claim 4, in which the said attachment between an electrical lead and a contact is effected by a further body of semiconductor material serving merely as a conductor and having one surface attached both to the support member and to the contact, the electrical lead being ohmically attached to an opposite surface of the further body.

7. An integrated network according to Claim 4, in which the bodies comprise highly conductive semiconductor material, the said one regions being of lesser conductivity and each having a semiconductor component formed therein, at least some of the metallic contacts also being ohmically attached to respective ones of further bodies of semiconductor material serving merely as conductors on surfaces thereof attached to the support member, and electrical leads ohmically attached to the opposite surfaces of the further bodies.

8. A network according to any one of Claims 4—7, in which at least one of the electrical components is a transistor.

9. A network according to Claim 7, in which at least one of the lesser conductivity regions contains further regions of predetermined conductivity types which all extend to the said one surface to define a transistor in the semiconductor body containing these regions.

10. A method of fabricating a semiconductor device, comprising the steps of forming in a body of semiconductor material at least one region of predetermined conductivity type extending to one surface of the body and covering that surface with a layer of insulating material having an aperture exposing the said region, depositing a metallic contact to make ohmic contact with the said region through the aperture and to extend over the insulating layer, attaching an insulating support to the body to sandwich the insulating layer and the contact between the semiconductor body and the support, and ohmically attaching an electrical lead to the surface of the contact more remote from the support member.

11. A method according to Claim 10, including the steps of forming in the body of semiconductor material a first region of one conductivity type containing a second region of opposite conductivity type, and a third region of opposite conductivity type surrounding the first region, all three regions and the pn junctions between them extending to the

said one insulating of the first acts being with the through the insulating moving underlying yond the leads to locations surfaces support member further el the body the said

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65 5 said one surface of the body, in which the insulating layer has apertures exposing areas of the first and second regions, metallic contacts being deposited to make ohmic contact with the respective first and second regions through the apertures and to extend over the insulating layers beyond the pn junctions, removing parts of the semiconductor body underlying parts of the contacts extending beyond the pn junctions, attaching electrical leads to the respective metallic contacts at locations beyond the pn junctions and at the surfaces thereof more remote from the support member, and ohmically connecting a further electrical lead to the third region of the body at a surface of the body opposite the said one surface.

80 10 12. A method according to Claim 10 or Claim 11, in which concurrently with the removal of semiconductor material from the semiconductor body, a portion of the insulating material is removed to expose the metallic contact for ohmically connecting the electrical lead thereto.

85 25 13. A method according to Claim 11, in which the first, second and third regions are formed in a body of semiconductor material having the same conductivity type but higher conductivity than the third region and the insulating layer has at least one further aperture exposing a higher conductivity area of the body, in which one of the metallic contacts extends over the insulating layer to make ohmic contact with the higher conductivity portion of the body through the further aperture and to make contact with one of the first and second regions, and in which the said removal of part of the semiconductor body leaves the said higher conductivity portion as an island, and in which one of the first mentioned electrical leads is connected to the said higher conductivity island on a surface thereof remote from the support member.

100 40 105 45 14. A method of fabricating an integrated electrical network including the steps of,

110 50 a) forming a plurality of regions of semiconductor material in a body of semiconductor material of like conductivity type as and of higher conductivity than the regions, the said regions extending to the same surface of the body, and forming a semiconductor device in at least one of the said regions adjacent to the said one surface,

115 55 b) depositing first metallic ohmic contacts on respective zones of the said semiconductor device and of at least one of the other regions through apertures formed in an insulating layer covering the said one surface of the body; the first contacts extending over the insulating layer and being ohmically connected to respective further surface zones of

semiconductor body through further apertures in the insulating layer,

65 c) locating an insulating support adjacent the said one surface of the body and attaching the support to the body.

70 d) masking regions of a surface of the semiconductor body opposite the said one surface, the masked regions being disposed opposite the said regions of semiconductor material and opposite the said further apertures in the insulating layer,

75 e) etching the semiconductor body in the unmasked regions of the said opposite surface thereof to form the body into mesa regions electrically isolated from each other apart from the electrical inner-connections provided by the deposited contacts,

80 f) depositing further metallic contacts on a surface of each mesa region opposite the substrate and attaching electrical leads to the further metallic contacts.

85 15. A method according to Claim 14, in which prior to the masking and etching step, part of the said opposite surface of the body is removed to reduce the thickness of the higher conductivity portion.

90 16. A method according to Claim 14, in which the said regions of semiconductor material are formed in the said one surface of the semiconductor body by vapor etching and semiconductor material redeposition.

95 17. A method according to Claim 16, including the steps of applying diffusion masking material to the said one surface of the body and forming the or each semiconductor device by planar diffusion through the mask into a said region of the semiconductor material, the diffusion masking material also providing the said apertured insulating layer.

100 18. A method according to any one of Claims 14—17, in which the said semiconductor device is a transistor and the other one, or at least one of the other ones of the said regions provides a passive semiconductor device, the semiconductor devices being interconnected in a desired manner by at least some of the said electrical leads.

105 19. A method of fabricating semiconductor devices, substantially as described herein to and as illustrated by Figs. 1—3 of the accompanying drawings.

110 20. A method according to Claim 19, substantially as further described herein with reference to and as illustrated by Figs. 4 and 5 of the accompanying drawings.

115 21. A method of forming a semiconductor device, substantially as described herein with reference to and illustrated by Figs. 6—10 of the accompanying drawings.

120 22. A method according to Claim 21, substantially as further described herein with reference to and as illustrated by Figs. 10—12 of the accompanying drawings.



23. The product of a method according to any one of Claims 11—22.

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