SUMMARY

[0012] The invention provides a microelectronic structure that includes a through substrate via, and a method for fabricating the microelectronic structure that includes the through substrate via. In particular, the microelectronic structure includes a through substrate via that includes: (1) an annular conductor layer located within an aperture through a substrate but not filling the aperture within the substrate, such as a semiconductor substrate, where the annular conductor layer may optionally have an enclosed end; and (2) a plug layer (i.e., typically, but not necessarily a dielectric plug layer) surrounded by the annular conductor layer and completely filling the aperture within the substrate. A method for fabricating the microelectronic structure includes forming a blind aperture within a microelectronic substrate, such as a semiconductor substrate. Amongst other optional layers, a conformal conductor layer is located and formed into the blind aperture while not filling the blind aperture, and a dielectric plug layer is located and formed over the conformal conductor layer and completely filling the blind aperture. Excess portions of the dielectric plug layer and the conformal conductor layer are planarized and a bottom portion of the substrate is also removed to expose at least the conformal conductor layer.

[0013] An annular through substrate via in accordance with the invention provides value insofar as such an annular through substrate via is more readily and uniformly fabricated since such an annular through substrate via may be fabricated using a wider blind aperture than a blind aperture of an analogous via that comprises a non-annular via.

[0014] A particular microelectronic structure in accordance with the invention includes a substrate that includes an aperture that penetrates through the substrate. This particular microelectronic structure also includes an annular conductor layer located at a periphery of the aperture and not filling the aperture. This particular microelectronic structure also includes a plug layer located surrounded by the annular conductor layer and filling the aperture.

[0015] Another particular microelectronic structure in accordance with the invention includes a semiconductor substrate including an aperture that penetrates through the semiconductor substrate. This particular microelectronic structure also includes an

annular liner layer located upon the semiconductor substrate at a periphery of the aperture and not filling the aperture. This particular microelectronic structure also includes an annular conductor layer located upon the annular liner layer and not filling the aperture. This particular microelectronic structure also includes an annular stop layer located upon the annular conductor layer and not filling the aperture. This particular microelectronic structure also includes a plug layer located upon the annular stop layer and filling the aperture.

[0016] A particular method for fabricating a microelectronic structure in accordance with the invention includes forming a blind aperture within a substrate. This particular method also includes successive layering and subsequently planarizing within the blind aperture a conformal conductor layer that does not completely fill the blind aperture and a plug layer that does completely fill the aperture. This particular method also includes planarizing a backside of the substrate to expose at least the conformal conductor layer.

[0017] Another particular method for fabricating a microelectronic structure in accordance with the invention includes forming a blind aperture within a semiconductor substrate. This particular method also includes successive layering and subsequently planarizing within the blind aperture a conformal dielectric liner layer that does not completely fill the aperture, a conformal conductor layer that does not completely fill the blind aperture, a conformal stop layer that does not completely fill the aperture and a plug layer that does completely fill the aperture. This particular method also includes planarizing a backside of the substrate to expose at least the conformal conductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The objects, features and advantages of the invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

[0019] FIG. 1 to FIG. 13 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a microelectronic structure in accordance with a particular embodiment of the invention.

structure of FIG. 12 may be effected using methods including but not limited to purely mechanical planarizing methods and chemical mechanical polish planarizing methods. As is illustrated within the schematic cross-sectional diagram of FIG. 12, the microelectronic structure is planarized to provide that the conductor layer 20'' still has an enclosed bottom, although such a feature of the microelectronic structure whose schematic cross-sectional diagram is illustrated in FIG. 12 is not a limitation of the embodiment or of the invention. Rather, within the context of the embodiment, each of the conformal conductor liner layer 18', the conductor layer 20' and the etch stop layer 22' that are illustrated in FIG. 11 may be planarized to leave exposed portions of a resulting conductor liner layer, a resulting conductor layer, a resulting stop layer and a resulting plug layer, in accordance with the phantom line that corresponds with reference numeral 27.

[0050] FIG. 13 shows a third conductor layer 28 located and formed upon a bottom surface of the microelectronic structure whose schematic cross-sectional diagram is illustrated in FIG. 12. The third conductor layer 28 is otherwise generally analogous or equivalent with the second conductor layer 26 that is illustrated in FIG. 9 within the context of conductor materials and methods of fabrication, but rather located and formed upon a bottom surface of the of the microelectronic structure that is illustrated in FIG. 12 rather than the top surface of the microelectronic structure that is illustrated in FIG. 12. Typically, the third conductor layer 28 comprises a conductor material of a thickness that meets the prescribed and required performance metrics for resistance within the microelectronic structure whose schematic cross-sectional diagram is illustrated in FIG. 13.

[0051] FIG. 13 shows a schematic cross-sectional diagram of a microelectronic structure in accordance with a particular embodiment of the invention. The microelectronic structure includes a substrate 10'' that includes an aperture that is formed completely through the substrate 10''. Successively nested within the aperture is: (1) a conductor liner layer 18'' at a periphery of the aperture and not filling the aperture; (2) a conductor layer 20'' located upon the conductor liner layer 18'' and also not filling the aperture; (3) a stop layer 22' located upon the conductor layer 20'' and also not filling the aperture; and (4) a plug layer 24''' located upon the etch stop layer 22' and filling the aperture.

SUMMARY

[0012] The invention is defined in the independent claims. Some optional features of the invention are defined in the dependent claims.

[0012a] There is provided in one example, a microelectronic structure that includes a through substrate via, and a method for fabricating the microelectronic structure that includes the through substrate via. In particular, the microelectronic structure includes a through substrate via that includes: (1) an annular conductor layer located within an aperture through a substrate but not filling the aperture within the substrate, such as a semiconductor substrate, where the annular conductor layer may optionally have an enclosed end; and (2) a plug layer (i.e., typically, but not necessarily a dielectric plug layer) surrounded by the annular conductor layer and completely filling the aperture within the substrate. A method for fabricating the microelectronic structure includes forming a blind aperture within a microelectronic substrate, such as a semiconductor substrate. Amongst other optional layers, a conformal conductor layer is located and formed into the blind aperture while not filling the blind aperture, and a dielectric plug layer is located and formed over the conformal conductor layer and completely filling the blind aperture. Excess portions of the dielectric plug layer and the conformal conductor layer are planarized and a bottom portion of the substrate is also removed to expose at least the conformal conductor layer.

[0013] An exemplary annular through substrate via provides value insofar as such an annular through substrate via is more readily and uniformly fabricated since such an annular through substrate via may be fabricated using a wider blind aperture than a blind aperture of an analogous via that comprises a non-annular via.

[0014] A particular exemplary microelectronic structure includes a substrate that includes an aperture that penetrates through the substrate. This particular microelectronic structure also includes an annular conductor layer located at a periphery of the aperture and not filling the aperture. This particular microelectronic structure also includes a plug layer located surrounded by the annular conductor layer and filling the aperture.

[0015] Another particular exemplary microelectronic structure includes a semiconductor substrate including an aperture that penetrates through the semiconductor substrate. This particular microelectronic structure also includes an

annular liner layer located upon the semiconductor substrate at a periphery of the aperture and not filling the aperture. This particular microelectronic structure also includes an annular conductor layer located upon the annular liner layer and not filling the aperture. This particular microelectronic structure also includes an annular stop layer located upon the annular conductor layer and not filling the aperture. This particular microelectronic structure also includes a plug layer located upon the annular stop layer and filling the aperture.

[0016] A particular exemplary method for fabricating a microelectronic structure includes forming a blind aperture within a substrate. This particular method also includes successive layering and subsequently planarizing within the blind aperture a conformal conductor layer that does not completely fill the blind aperture and a plug layer that does completely fill the aperture. This particular method also includes planarizing a backside of the substrate to expose at least the conformal conductor layer.

[0017] Another particular exemplary method for fabricating a microelectronic structure includes forming a blind aperture within a semiconductor substrate. This particular method also includes successive layering and subsequently planarizing within the blind aperture a conformal dielectric liner layer that does not completely fill the aperture, a conformal conductor layer that does not completely fill the blind aperture, a conformal stop layer that does not completely fill the aperture and a plug layer that does completely fill the aperture. This particular method also includes planarizing a backside of the substrate to expose at least the conformal conductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The objects, features and advantages of the invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

[0019] FIG. 1 to FIG. 13 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a microelectronic structure.

structure of FIG. 12 may be effected using methods including but not limited to purely mechanical planarizing methods and chemical mechanical polish planarizing methods. As is illustrated within the schematic cross-sectional diagram of FIG. 12, the microelectronic structure is planarized to provide that the conductor layer 20" still has an enclosed bottom, although such a feature of the microelectronic structure whose schematic cross-sectional diagram is illustrated in FIG. 12 is not a limitation of the embodiment or of the invention. Rather, within the context of the embodiment, each of the conformal conductor liner layer 18', the conductor layer 20' and the etch stop layer 22' that are illustrated in FIG. 11 may be planarized to leave exposed portions of a resulting conductor liner layer, a resulting conductor layer, a resulting stop layer and a resulting plug layer, in accordance with the phantom line that corresponds with reference numeral 27.

[0050] FIG. 13 shows a third conductor layer 28 located and formed upon a bottom surface of the microelectronic structure whose schematic cross-sectional diagram is illustrated in FIG. 12. The third conductor layer 28 is otherwise generally analogous or equivalent with the second conductor layer 26 that is illustrated in FIG. 9 within the context of conductor materials and methods of fabrication, but rather located and formed upon a bottom surface of the of the microelectronic structure that is illustrated in FIG. 12 rather than the top surface of the microelectronic structure that is illustrated in FIG. 12. Typically, the third conductor layer 28 comprises a conductor material of a thickness that meets the prescribed and required performance metrics for resistance within the microelectronic structure whose schematic cross-sectional diagram is illustrated in FIG. 13.

[0051] FIG. 13 shows a schematic cross-sectional diagram of an exemplary microelectronic structure .The microelectronic structure includes a substrate 10" that includes an aperture that is formed completely through the substrate 10". Successively nested within the aperture is: (1) a conductor liner layer 18" at a periphery of the aperture and not filling the aperture; (2) a conductor layer 20" located upon the conductor liner layer 18" and also not filling the aperture; (3) a stop layer 22' located upon the conductor layer 20" and also not filling the aperture; and (4) a plug layer 24"' located upon the etch stop layer 22' and filling the aperture.