CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a lower structure;

a stack structure on the lower structure and having an opening;

a vertical structure in the opening;

a contact structure on the vertical structure; and

a conductive line on the contact structure,

wherein the stack structure includes a plurality of gate layers and a plurality of interlayer insulating layers,

wherein the vertical structure includes an insulating core region, a channel semiconductor layer, a plurality of data storage patterns, a first dielectric layer, and a second dielectric layer,

wherein the insulating core region extends in a vertical direction, the vertical direction being perpendicular to an upper surface of the lower structure,

wherein the channel semiconductor layer covers a side surface and a lower surface of the insulating core region,

wherein the plurality of data storage patterns are between the channel semiconductor layer and the plurality of gate layers, in a horizontal direction parallel to the upper surface of the lower structure, and are spaced apart from each other in the vertical direction,

wherein at least one of an upper surface and a lower surface in each of the plurality of data storage patterns is a concave shape,

wherein at least a portion of the first dielectric layer is disposed between the

plurality of data storage patterns and the plurality of gate layers,

wherein at least a portion of the second dielectric layer is disposed between the plurality of data storage patterns and the channel semiconductor layer, and

wherein the insulating core region includes a plurality of first convex portions having increased widths in regions facing the plurality of gate layers.

2. The semiconductor device according to claim 1, wherein the insulating core region further includes a plurality of second convex portions having increased widths in regions facing the plurality of interlayer insulating layers, and concave portions having decreased widths between the plurality of first convex portions and the plurality of second convex portions.

3. The semiconductor device according to claim 1 or claim 2,

wherein each of the plurality of data storage patterns includes a first side surface facing a corresponding one of the plurality of gate layers, and a second side surface facing the channel semiconductor layer,

wherein each of the plurality of data storage patterns includes a first portion adjacent to the first side surface, a second portion adjacent to the second side surface, and a minimum vertical thickness portion between the first portion and the second portion, and

wherein a thickness of the minimum vertical thickness portion is less than a maximum vertical thickness of the first portion and a maximum vertical thickness of the second portion.

4. The semiconductor device according to claim 3, wherein a distance

between the minimum vertical thickness portion and the first side surface is less than a distance between the minimum vertical thickness portion and the second side surface.

5. The semiconductor device according to claim 3, wherein a distance between the minimum vertical thickness portion and the first side surface is greater than a distance between the minimum vertical thickness portion and the second side surface.

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6. The semiconductor device according to claim 1 or claim 2,

wherein each of the plurality of data storage patterns includes a first side surface facing a corresponding one of the plurality of gate layers, and a second side surface facing the channel semiconductor layer,

wherein at least a portion of the plurality of data storage patterns further include a void between the first side surface and the second side surface, and

wherein a distance between the void and the first side surface is greater than a distance between the void and the second side surface.

7. The semiconductor device according to claim 1 or claim 2,

wherein each of the plurality of data storage patterns includes a first side surface facing a corresponding one of the plurality of gate layers, and a second side surface facing the channel semiconductor layer,

wherein at least a portion of the plurality of data storage patterns further include a void between the first side surface and the second side surface, and

wherein a distance between the void and the first side surface is less than a distance between the void and the second side surface.

8. The semiconductor device according to claim 1 or claim 2,

wherein each of the plurality of data storage patterns includes a first side surface facing a corresponding one of the plurality of gate layers, and a second side surface facing the channel semiconductor layer, and

wherein at least a portion of the second side surface is a concave shape.

9. The semiconductor device according to any one of claims 1 to 8, further comprising:

a horizontal connection structure between the lower structure and the stack structure,

wherein the horizontal connection structure includes a lower horizontal connection pattern, and an upper horizontal connection pattern on the lower horizontal connection pattern,

wherein the vertical structure passes through the stack structure, extends in a downward direction to pass through the horizontal connection structure, and extends into the lower structure,

wherein the upper horizontal connection pattern is spaced apart from the channel semiconductor layer of the vertical structure, and

wherein the lower horizontal connection pattern is in contact with the channel semiconductor layer of the vertical structure.

10. The semiconductor device according to claim 9, wherein the insulating core region further includes a lower convex portion facing the lower horizontal connection pattern.

11. The semiconductor device according to any one of claims 1, 3 to 10, wherein the insulating core region further includes concave portions having decreased widths in regions facing the interlayer insulating layers.

12. The semiconductor device according to any one of claims 1, 3 to 10, wherein the insulating core region has constant widths in regions facing the interlayer insulating layers.

13. A semiconductor device comprising:

a lower structure;

a stack structure including an interlayer insulating layer and a gate layer sequentially stacked on the lower structure; and

a vertical structure passing through the stack structure,

wherein the vertical structure includes an insulating core region passing through the interlayer insulating layer and the gate layer, a channel semiconductor layer covering at least a side surface of the insulating core region, a data storage pattern between the channel semiconductor layer and the gate layer, in a horizontal direction parallel to an upper surface of the lower structure, a first dielectric layer at least interposed between the data storage pattern and the gate layer, and a second dielectric layer at least interposed between the data storage pattern and the channel semiconductor layer,

wherein the data storage pattern has a first side surface facing the gate layer and a second side surface facing the channel semiconductor layer,

wherein the second side surface of the data storage pattern has a concave portion, and

wherein at least one of an upper surface and a lower surface of the data storage pattern is a concave shape.

14. The semiconductor device according to claim 13, wherein the second side surface of the data storage pattern has curved shapes on and below the concave portion.

15. The semiconductor device according to claim 13 or claim 14,

wherein the insulating core region includes a first concave portion, a first convex portion having a width greater than the first concave portion and disposed on the first concave portion, and a second concave portion having a width less than the first convex portion and disposed on the first convex portion,

wherein the first convex portion faces the data storage pattern, and

wherein a portion having a minimum horizontal width in the first concave portion and a portion having a minimum horizontal width in the second concave portion face the gate layer.

16. The semiconductor device according to claim 15, wherein a distance between the portion having the minimum horizontal width in the first concave portion and the portion having the minimum horizontal width in the second concave portion is less than a thickness of the gate layer in a vertical direction, and greater than a maximum thickness of the data storage pattern in the vertical direction.

17. The semiconductor device according to claim 15 or claim 16,

wherein the insulating core region further includes a second convex portion

having a width greater than that of the first concave portion and disposed below the first concave portion, and

wherein the second convex portion faces the interlayer insulating layer.

18. The semiconductor device according to claim 17, wherein a distance between a portion having a maximum horizontal width in the second convex portion and the portion having the minimum horizontal width in the first concave portion is greater than a distance between the portion having the minimum horizontal width in the first concave portion and a portion having a maximum horizontal width in the first convex portion.

19. A semiconductor device comprising:

a lower structure;

a stack structure including an interlayer insulating layer and a gate layer sequentially stacked on the lower structure; and

a vertical structure passing through the stack structure,

wherein the vertical structure includes an insulating core region passing through the interlayer insulating layer and the gate layer, a channel semiconductor layer covering at least a side surface of the insulating core region, a data storage pattern between the channel semiconductor layer and the gate layer, in a horizontal direction parallel to an upper surface of the lower structure, a first dielectric layer at least interposed between the data storage pattern and the gate layer, and a second dielectric layer at least interposed between the data storage pattern and the channel semiconductor layer,

wherein the insulating core region has at least two inflection points in a portion

facing the gate layer, and

wherein at least one of an upper surface and a lower surface of the data storage pattern is a concave shape.