

DESCRIPTION

TITLE: PROCESS FOR MANUFACTURING A COMPOSITE STRUCTURE
COMPRISING A THIN LAYER OF MONOCRYSTALLINE SiC ON A CARRIER
SUBSTRATE MADE OF SiC

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor materials for microelectronic components. The invention relates in particular to a process for manufacturing a composite structure comprising a thin layer of monocrystalline silicon carbide on a carrier substrate made of silicon carbide.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

Interest in silicon carbide (SiC) has increased considerably over the last few years because this semiconductor material is able to increase the capacity to handle energy. SiC is increasingly widely used for manufacturing innovative power devices to meet the needs of rising fields in electronics, notably such as electric vehicles.

Power devices and integrated power supply systems based on monocrystalline silicon carbide are able to manage a much higher power density than their traditional silicon homologues, and do so with smaller active-zone dimensions. To further limit the dimensions of power devices on SiC, it is advantageous to manufacture vertical instead of lateral components. For this, vertical electrical conduction, between an electrode arranged on the front face of the SiC structure and an electrode arranged on the rear face, must be allowed by said structure.

However, monocrystalline SiC substrates intended for the microelectronics industry are still expensive and difficult to supply at a large size. It is therefore advantageous to make use of thin-layer transfer solutions to produce composite structures which typically comprise a thin layer of monocrystalline SiC on a less expensive carrier substrate. One well-known thin-layer transfer solution is the Smart Cut™ process, based on implanting light ions and assembling by direct bonding. Such a process makes it possible, for example, to manufacture a composite structure comprising a thin layer of monocrystalline SiC (c-SiC), taken from a c-SiC donor substrate, in direct contact with a carrier substrate made of polycrystalline SiC (p-SiC), and allowing vertical electrical conduction. However, it remains difficult to achieve high-quality direct bonding by molecular adhesion between two substrates made of c-SiC and p-SiC, since managing the surface state and roughness of these substrates is complex.

Various methods derived from this process are also known from the prior art. For example, F. Mu et al. (ECS Transactions, 86 (5) 3-21, 2018) implement direct bonding after activating the surfaces to be assembled by bombardment with argon (SAB: "surface activation bonding"): such a treatment prior to bonding generates a very high density of side bonds, which promote the formation of covalent bonds at the assembly interface, and hence a high bonding energy. However, this method has the drawback of generating an amorphous layer at the surface of the monocrystalline SiC donor substrate, which negatively affects vertical electrical conduction between the thin layer of c-SiC and the carrier substrate made of p-SiC.

Solutions have been proposed to solve this problem, in particular in EP3168862, involving the implantation of dopant species into said amorphous layer in order to restore its electrical properties. The main drawback of this approach is its complexity and hence its cost.

Also known is US8436363, which describes a process for manufacturing a composite structure comprising a thin layer of c-SiC arranged on a metal carrier substrate, the coefficient of thermal expansion of which is matched to that of the thin layer. This manufacturing process comprises the following steps:

- forming a buried brittle plane in a c-SiC donor substrate, delimiting a thin layer between said buried brittle plane and a front surface of the donor substrate;

- depositing a layer of metal, for example of tungsten or molybdenum, on the front surface of the donor substrate to form the carrier substrate with sufficient thickness to act as a stiffener;

- separating along the buried brittle plane to form, on the one hand, the composite structure comprising the metal carrier substrate and the thin layer of c-SiC and, on the other hand, the rest of the c-SiC donor substrate.

Such a manufacturing process is, however, not compatible when the material forming the carrier substrate is p-SiC requiring deposition at temperatures above 1200°C (usual temperatures for the manufacture of p-SiC). Specifically, at these high temperatures, the growth kinetics of the cavities present in the buried brittle plane are faster than the growth kinetics of the p-SiC layer and the thickness required for a stiffening effect is not reached before blistering starts to occur, which is related to the deformation of the layer vertically in line with the cavities.

Irrespective of the layer transfer technique used, the additional problem arises of providing a composite structure comprising a thin c-SiC layer of very high quality, and in particular free of extended defects (or having a very low density thereof), which are liable to affect the performance qualities

and the reliability of power devices intended to be produced on said thin layer.

SUBJECT OF THE INVENTION

The present invention relates to an alternative solution to those of the prior art, and is directed towards completely or partly overcoming the abovementioned drawbacks. The invention relates in particular to a process for manufacturing a composite structure comprising a high-quality thin layer of c-SiC on a carrier substrate made of SiC.

BRIEF DESCRIPTION OF THE INVENTION

The invention relates to a process for manufacturing a composite structure comprising a thin layer of monocrystalline silicon carbide arranged on a carrier substrate made of silicon carbide. The process comprises:

- a) a step of providing an initial substrate made of monocrystalline silicon carbide,
- b) a step of epitaxial growth of a monocrystalline silicon carbide donor layer on the initial substrate, to form a donor substrate, the donor layer having a density of crystal defects less than that of the initial substrate,
- c) a step of ion implantation of light species into the donor layer, to form a buried brittle plane delimiting the thin layer between said buried brittle plane and a free surface of said donor layer,
- d) a step of direct liquid injection-chemical vapour deposition, at a temperature below 1000°C, to form a carrier layer directly on the free surface of the donor layer, said carrier layer being formed by an at least partially amorphous SiC matrix,

- e) a step of separating along the buried brittle plane to form, on the one hand, an intermediate composite structure comprising the thin layer on the carrier layer and, on the other hand, the rest of the donor substrate,
- f) a step of heat treatment at a temperature of between 1000°C and 1800°C, applied to the intermediate composite structure, to crystallize the carrier layer and to form the polycrystalline carrier substrate,
- g) a step of mechanical and/or chemical treatment(s) of the composite structure, the treatment(s) being applied to a free face of the carrier substrate, the rear face of the composite structure, and/or to a free face of the thin layer, the front face of the composite structure.

According to other advantageous and non-limiting features of the invention, taken alone or in any technically feasible combination:

- the deposition step d) is performed at a temperature of between 100°C and 700°C, or even preferentially between 200°C and 600°C;
- the deposition step d) is performed at a pressure of between 1 Torr and 500 Torr;
- the precursors used during the deposition step d) are chosen from polysilylethylene and disilabutane;
- on conclusion of the deposition step d), the carrier layer has a thickness of greater than or equal to 10 microns, or even a thickness of greater than or equal to 50 microns, or even a thickness of greater than or equal to 100 microns, or even a thickness of greater than or equal to 200 microns;
- chemical etching, mechanical grinding and/or mechanochemical polishing is (are) applied to a free face of the carrier layer, between step d) and step e);

- step a) comprises the formation, on the initial substrate, of a monocrystalline conversion layer, to convert basal plane dislocation defects of the initial substrate into threading edge dislocation defects;
- the epitaxial growth step b) is performed at a temperature above 1200°C, preferentially between 1500°C and 1650°C;
- the separation step e) is performed at a temperature above the deposition temperature of step d);
- the separation step e) takes place during the deposition step d), preferentially at the end of step d);
- the separation step e) and the crystallization step f) take place during the same heat treatment;
- step g) comprises simultaneous mechanochemical polishing of a front face and of a rear face of the composite structure;
- the process comprises a step of reconditioning the rest of the donor substrate for the purpose of reuse as initial substrate or as donor substrate.

BRIEF DESCRIPTION OF THE FIGURES

Other features and advantages of the invention will become apparent from the following detailed description of the invention, which is given with reference to the appended figures, in which:

[Fig. 1] Figure 1 shows a composite structure produced according to a production process in accordance with the invention;

[Fig. 2a]

[Fig. 2b]

[Fig. 2c]

[Fig. 2d]

[Fig. 2e]

[Fig. 2f]

[Fig. 2g] Figures 2a to 2g show steps of a manufacturing process in accordance with the invention;

[Fig. 3a]

[Fig. 3b] Figures 3a and 3b show steps of a manufacturing process in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

In the description, the same reference numerals in the figures might be used for elements of the same type. The figures are schematic representations which, for the sake of legibility, are not to scale. In particular, the thicknesses of the layers along the z-axis are not to scale with respect to the lateral dimensions along the x- and y-axes; and the relative thicknesses of the layers with respect to one another are not necessarily respected in the figures.

The present invention relates to a process for manufacturing a composite structure 1 comprising a thin layer 10 of monocrystalline silicon carbide arranged on a carrier substrate 20 made of silicon carbide (Figure 1). The carrier substrate 20 is advantageously polycrystalline ("p-SiC" will be used to refer to polycrystalline SiC).

The process first comprises a step a) of providing an initial substrate 11 made of monocrystalline silicon carbide (Figure 2a). Throughout the rest of the description, "c-SiC" will be used to refer to monocrystalline silicon carbide.

The initial substrate 11 is preferentially in the form of a wafer with a diameter of 100 mm, 150 mm or 200 mm, or even 300 mm or even 450 mm, and a thickness typically between 300 and 800 microns. It has a front face 11a and a rear face 11b. The surface roughness of the front face 11a is advantageously chosen to be less than 1 nm Ra (average roughness), measured by atomic force microscopy (AFM) in a scan of 20 microns x 20 microns.

The process then comprises a step b) of epitaxial growth of a monocrystalline silicon carbide donor layer 110 on the initial substrate 11, to form a donor substrate 111 (Figure 2b). The epitaxial growth step is performed so that the donor layer 110 has a crystal defect density less than that of the initial substrate 11.

Typically, the initial substrate 11 made of c-SiC is of the 4H or 6H polytype, with an offcut angle less than 4.0° relative to the $\langle 11\text{-}20 \rangle$ crystallographic axis $\pm 0.5^\circ$, and a micropipe density of less than or equal to $5/\text{cm}^2$, or even less than $1/\text{cm}^2$. For example, when N- (nitrogen-)doped, it preferentially has a resistivity of between 0.015 ohm.cm and 0.030 ohm.cm. An initial substrate 11 having a low density of basal plane dislocation (BPD) defects, typically less than or equal to $3000/\text{cm}^2$, may be chosen. c-SiC substrates having BPD densities of the order of $1500/\text{cm}^2$ are reasonably available, which facilitates their supply.

It is desirable for the donor layer 110, from which the c-SiC thin layer 10 of the composite structure 1 will be formed on conclusion of the process of the present invention, to have a crystal quality greater than that of the initial substrate 11, to meet the specifications required for the vertical components intended to be produced on said thin layer 10. Various types of extended defects are present in a c-SiC layer or substrate. These extended defects may affect the performance and reliability of

the components. In particular, defects of BPD type are fatal for bipolar components: specifically, a Shockley stacking fault (or SSF) is extended from the dislocation when the energy for recombination of an electron-hole pair is available. The expansion of an SSF stacking fault inside the active region of the component brings about an increase in the passing state resistance of the component.

The c-SiC donor layer 110 is thus produced so as to have a BPD defect density of less than or equal to $1/\text{cm}^2$.

For this, the epitaxial growth step b) is performed at a temperature above 1200°C , preferentially between 1500°C and 1650°C . The precursors used are silane (SiH_4), propane (C_3H_8) or ethylene (C_2H_4); the carrier gas may be hydrogen with or without argon.

The low content of BPD defects in the donor layer 110 is obtained by favouring the conversion of the BPD defects present in the initial substrate 11 into threading edge dislocations (TED).

According to a particular embodiment, step a) comprises the formation of a monocrystalline conversion layer 13, preferentially based on c-SiC, to maximize the conversion of the BPD defects of the initial substrate 11 into TED defects (Figure 3a). For this, it is advantageous to choose a low cutting angle close to 4° for the initial c-SiC substrate 11, to increase the *in situ* etching performed before the epitaxial growth, to target large growth rates (typically greater than $5\text{ }\mu\text{m/h}$) and finally to choose growth conditions for the monocrystalline conversion layer 13, with a C/Si ratio in the precursor streams of close to 1.

Step b) then consists in performing the epitaxial growth of the donor layer 110 on said conversion layer 13 (Figure 3b). According to this particular embodiment, it is also possible to obtain a c-SiC donor layer 110 with a BPD defect density of less than or equal to $1/\text{cm}^2$ or even less than $0.1/\text{cm}^2$. Furthermore,

the probability of bipolar degradation (probability of a hole arriving under the BPD/TED conversion point) on conclusion of the process according to the present invention is negligible (< 0.1%), the monocrystalline conversion layer 13 not being intended to be transferred into the composite structure 1. The prior art directed towards reducing bipolar degradations consists in incorporating, between the conversion layer and the active layer, a recombination layer (nitrogen-doped beyond 10^{18} at/cm³). This layer can, at the cost of a thickness of 10 μ m and of a concentration of greater than 5×10^{18} /cm³, reduce the probability of the presence of holes to 0.1% relative to the base structure not including this recombination layer. In the present invention, since the monocrystalline conversion layer 13 is not transferred, the probability of a hole reaching the nucleation point of the bipolar degradation (point of BPD-TED conversion or any BPD point) is at least less than 0.1%, or even very close to 0%.

It is noted that conventional sequences of cleaning or etching of the initial substrate 11, directed towards eliminating all or some of the particulate, metallic or organic contaminants, or a native oxide layer which are potentially present on its front face 11a, may be performed prior to the epitaxial growth step b).

The manufacturing process according to the invention also comprises a step c) of ion implantation of light species into the donor layer 110, to a given depth representative of the desired thickness of the thin layer 10 and in all cases not reaching the initial substrate 11 (and/or the conversion layer 13, when this layer is present). This implantation generates a buried brittle plane 12 in the donor layer 110 which delimits the thin layer 10 between said buried brittle plane 12 and a free surface 11a of said donor layer 110 (Figure 2c).

The implanted light species are preferentially hydrogen, helium or these two species co-implanted. As is well known with reference to the Smart Cut™ process, these light species will form, around the given depth, microcavities distributed in a thin layer parallel to the free surface 11a of the donor layer 110, i.e. parallel to the plane (x,y) in the figures. This thin layer is referred to as the buried brittle plane 12, for the sake of simplicity.

The energy for implanting the light species is chosen so as to reach the given depth in the donor layer 110.

Typically, hydrogen ions will be implanted at an energy between 10 keV et 250 keV, and at a dose between $5 \times 10^{16}/\text{cm}^2$ and $1 \times 10^{17}/\text{cm}^2$, to delimit a thin layer 10 having a thickness of about 100 to 1500 nm.

It should be noted that a protective layer could be deposited on the free face of the donor layer 110 prior to the ion implantation step. This protective layer may be composed of a material such as silicon oxide or silicon nitride, for example.

The process according to the invention then comprises a step d) of direct liquid injection-chemical vapour deposition (DLI-CVD), at a temperature below 1000°C and preferentially below 900°C , to form a carrier layer 20' directly on the free surface of the donor layer 110 (Figure 2d). The deposition step d) may be performed at a temperature of between 100°C and 800°C , between 100°C and 700°C , or even advantageously between 200°C and 600°C . The pressure in the deposition chamber is preferentially defined between 1 Torr and 500 Torr.

The DLI-CVD deposition technique affords good yields between the materials (precursors) supplied and the deposition thicknesses achieved, without the need to use chlorinated precursors, which limits the costs and the environmental constraints.

Preferentially, the DLI-CVD deposition involves a disilabutane precursor or a polysilylethylene precursor, said precursor being pure or diluted. Other precursors such as methyltrichlorosilane, ethylenetrichlorosilane, dichloromethylvinylsilane, tetraethylsilane, tetramethylsilane, diethylmethylsilane, bistrimethylsilylmethane or hexamethyldisilane may optionally be used.

Such a technique is described in the thesis by Guillaume Boisselier (2013, "Dépôt chimique en phase vapeur de carbures de chrome, de silicium et d'hafnium assisté par injection liquide pulsée [Pulsed liquid injection-chemical vapour deposition of chromium, silicon and hafnium carbides]"), for applications in the deposition of ceramic coatings onto parts, to protect them during very high temperature treatments, for example of steel or alloy metal parts.

The Applicant has developed a DLI-CVD deposition step d) for an entirely different application, namely the formation of a carrier layer 20' on a c-SiC donor layer 110, to obtain, on conclusion of the manufacturing process, a composite structure 1 intended for the microelectronics field.

The deposited carrier layer 20' forms an SiC matrix comprising amorphous SiC, and reaction byproducts derived from the precursors used during the deposition and formed from carbon chains. In addition, the SiC matrix may optionally comprise crystalline SiC grains.

The DLI-CVD technique can afford a deposition rate of greater than or equal to 10 microns/hour, or even greater than 50 microns/hour, or else even greater than 100 microns/hour. Given the mean deposition temperature, the deposition rate does not need to be high (beyond obvious economic reasons), since the

heat-activated growth of the cavities of the buried brittle plane 12 remains slow within these temperature ranges, making it easily possible to achieve a thickness of carrier layer 20' that is capable of ensuring a stiffening effect with respect to the buried brittle plane 12.

On conclusion of step d), the carrier layer 20' has a thickness of greater than or equal to 10 microns, 50 microns, 100 microns or even greater than or equal to 200 microns. The stack 211 resulting from step d) comprises the carrier layer 20' arranged on the donor layer 110, which is itself arranged on the initial substrate 11.

The process according to the present invention then comprises a step e) of separation along the buried fragile plane 12, to form, on the one hand, the intermediate composite structure 1' and, on the other hand, the rest 111' of the donor substrate (Figure 2e).

According to an advantageous embodiment, the separation step e) is performed by applying a heat treatment to the stack 211, at a separation temperature above the deposition temperature of step d). Specifically, the microcavities present in the buried brittle plane 12 follow growth kinetics until the initiation of a fracture wave which will propagate across the entire extent of the buried brittle plane 12 and result in separation between the intermediate composite structure 1' and the rest of the initial substrate 111'. In practice, the temperature may be between 950°C and 1200°C and preferentially between 1000°C and 1200°C, as a function of the implantation conditions of step c).

According to an alternative embodiment, the separation step e) is performed by applying a mechanical stress to the stack 211, optionally preceded by a heat treatment to embrittle the buried brittle plane 12. The stress may be exerted, for example, by

inserting a tool (e.g.: razor blade) close to the buried brittle plane 12. By way of example, the separation stress may be of the order of a few GPa, preferentially greater than 2 GPa.

According to yet another embodiment, step e) of separation along the buried brittle plane 12 is performed during or directly at the end of the DLI-CVD deposition step d), in particular when the deposition temperatures are in the range 900°C-1000°C.

The manufacturing process according to the present invention then comprises a step f) of heat treatment at a temperature of between 1000°C and 1800°C, applied to the intermediate composite structure 1', to crystallize the carrier layer 20' and to form the polycrystalline carrier substrate 20.

The annealing atmosphere may notably comprise gases such as argon, nitrogen, hydrogen, helium or a mixture of these gases. Such annealing has the effect of eliminating the hydrogen from the carrier layer 20' and bringing about crystallization of the SiC matrix in the form of polycrystalline SiC.

A conventional furnace for treating a plurality of structures simultaneously (batch annealing) may be used to perform the crystallization heat treatment. The typical duration of the treatment is then between a few minutes and a few hours.

It may optionally be envisaged to perform the crystallization heat treatment *in situ*, in the DLI deposition chamber, for a typical duration of the order of a few minutes.

Advantageously, the temperature increase and decrease ramps will be limited, for example less than 20°/minute, less than 5°/minute or even less than 1°/minute, to limit the appearance of cracks or structural defects in the crystalline layer.

After step f), a composite structure 1 is obtained comprising a thin layer 10 of monocrystalline silicon carbide arranged on a carrier substrate 20 made of polycrystalline silicon carbide.

The deposition parameters (step d) and crystallization annealing parameters (step f) are determined so that said carrier substrate 20 has:

- good electrical conductivity, i.e. less than or equal to 0.03 ohm.cm, or even less than or equal to 0.01 ohm.cm,
- high thermal conductivity, i.e. greater than or equal to 150 W.m⁻¹.K⁻¹, or even greater than or equal to 200 W.m⁻¹.K⁻¹,
- and a coefficient of thermal expansion close to that of the thin layer 10, i.e. typically between 3.8^{E-6}/K and 4.2^{E-6}/K at room temperature.

To obtain these properties, the following structural characteristics are preferentially targeted for the carrier substrate 20: polycrystalline structure, grains of 3C SiC type, [111] oriented, with a mean size of 1 to 50 µm in the main plane of the substrate, N-type doping for a final resistivity of less than or equal to 0.03 ohm.cm, or even less than or equal to 0.01 ohm.cm.

Furthermore, a non-insulating interface between the donor layer 110 and the carrier substrate 20 is preferentially targeted. A specific resistance of the interface typically less than 1 mohm.cm² is typically expected. To ensure the electrical conductivity of the interface, removal of the native oxide present on the free face of the donor layer 110 is performed by HF (hydrofluoric acid) deoxidation, via a wet or dry route, prior to the deposition step d). Alternatively, overdoping at least of the first deposited nanometres of the carrier layer 20' may be performed by introducing dopant species during the DLI-CVD deposition step d). It should be noted that, in general, dopant species may be introduced (in various dosages) during the

deposition step d) according to the level of doping and the electrical conductivity targeted for the carrier substrate 20, which conductivity will be effective on conclusion of the crystallization annealing of step f).

Advantageously also, prior to the deoxidation and/or to the formation of the carrier layer 20', cleaning sequences are applied to the donor substrate 111 to remove all or some of the particulate, metallic or organic contaminants potentially present on its free faces.

As is known per se, on conclusion of the separation step e), the free face 10a of the thin layer 10 of the composite structure 1 has a surface roughness of between 5 and 100 nm RMS (measured with an atomic force microscope (AFM), on scans of 20 microns × 20 microns).

A step g) of mechanical and/or chemical treatment(s) of the composite structure 1 is thus envisaged to smooth the free surface 10a of the thin layer 10 and/or to correct the thickness uniformity of the composite structure 1 (Figure 2f).

Step g) may comprise mechanochemical polishing (MCP) of the free face 10a of the thin layer 10, typically with removal of material of the order of 50 nm to 1000 nm, so as to obtain a final roughness of less than 0.5 nm RMS (on an AFM field of 20×20 μm), or even less than 0.3 nm. Step g) may also comprise a chemical or plasma treatment (cleaning or etching), for example cleaning of SC1/SC2 type (Standard Clean 1, Standard Clean 2) and/or HF (hydrofluoric acid), and/or an N₂, Ar, CF₄, etc. plasma, to further improve the quality of the free face 10a of the thin layer 10.

It is important to note that the crystallization of the carrier layer 20' often causes cracks or structural defects in the

crystalline layer (which forms the carrier substrate 20), which has an impact on its mechanical and electrical quality.

Thus, step g) may comprise mechanochemical polishing (MCP) and/or a chemical treatment (etching or cleaning) and/or a mechanical treatment (rectification) of the rear face 20b of the carrier substrate 20, so as to eliminate all or some of the cracks and structural defects, to improve the thickness uniformity of said carrier substrate 20 and also its roughness on the rear face 20b. The thickness removed at the rear face may be between about 100 microns and a few microns.

A roughness of less than 0.5 nm RMS (measured with an atomic force microscope (AFM) on fields of 20 microns $\times$ 20 microns) is desired to produce vertical components, for which at least one metal electrode will be present on the rear face 20b of the composite substrate 1.

Polishing or rectification of the edges of the composite structure 1 may also be performed during this step g) to make the shape of its circular contour and the cutting edge waste compatible with the requirements of microelectronic manufacturing processes.

It should be noted that the treatments applied to the rear face 20b of the carrier substrate 20 may optionally be applied to the free face of the carrier layer 20', just before the separation step e), i.e. before the front face 10a of the composite structure 1 is laid bare, so as to limit its contamination, notably in the course of polluting or restrictive treatments such as chemical etching or mechanical grinding (rectification).

According to an advantageous embodiment, the mechanochemical treatment step g) comprises simultaneous polishing (MCP) of a front face 10a and of a rear face 20b of the composite structure

1, to make said structure 1 smooth and to improve its thickness uniformity. The polishing parameters may differ between the front face and the rear face, the smoothing of a c-SiC surface and of a p-SiC surface usually requiring different consumables. The mechanical component of the polishing is favoured in particular for the rear face 20b when the carrier substrate 20 is made of p-SiC, to limit the preferential attack of the grain joints by the chemical component of the polishing. By way of example, the polishing parameters, such as the spin speed (polishing head and plate), the pressure, the concentration and physical properties of the abrasives (i.e. diamond nanoparticle diameter between about 10 nm and 1 μm), may be modified to accentuate the mechanical component.

Optionally, a step g') of heat treatment at a temperature of between 1000°C and 1800°C, for about one hour and up to a few hours, is performed after step g). The object of this step is to stabilize the composite structure 1, by ensuring structural or surface defects, still present in and/or on the thin layer 10, and, where appropriate, by making the crystalline configuration of the carrier substrate 20 evolve substantially, so that the structure 1 is compatible with the subsequent high-temperature heat treatments required for the manufacture of components on the thin layer 10.

The process according to the invention may comprise a second step h) of epitaxial growth of an additional layer 10' of monocrystalline silicon carbide on the thin layer 10 of the composite structure 1 (Figure 2g). Such a step is applied when a relatively large thickness of working layer 100 is required for the manufacture of components, typically from about 5 to 50 microns.

It may be chosen to limit the temperatures applied during this step h), so as to restrict the stresses induced in the working layer 100 (corresponding to the combination of the thin layer 10 and the additional layer 10') because of the composite structure 1.

Finally, the manufacturing process may comprise a step of reconditioning the rest 111' of the donor substrate for the purpose of reuse as initial substrate 1 or as donor substrate 111. Such a reconditioning step is based on one or more treatments of the face 110'a (Figure 2e), by surface or edge mechanochemical polishing, and/or by mechanical rectification, and/or by wet or dry chemical etching.

Preferentially, the thickness of the donor layer 110 formed in step b) is defined so that the rest 111' of the donor substrate 111 can be reused at least twice as donor substrate 111.

Preferentially, when the conversion layer 13 is present, care will be taken to keep said layer intact, i.e. to always keep a portion of donor layer 10 on the rest 111' of the donor substrate. Thus, when the portion of donor layer 10 is insufficient for the production of a composite structure 1, only the step of epitaxial growth of the donor layer 10 is necessary and not the prior step of growth of the conversion layer 13.

Example:

According to a non-limiting implementation example, the initial substrate 11 provided in step a) of the manufacturing process is a wafer made of c-SiC of 4H polytype, with an orientation of 4.0° relative to the $\langle 11-20 \rangle$ axis $\pm 0.5^\circ$, with a diameter of 150 mm and a thickness of 350 μm .

A conventional RCA cleaning sequence (Standard Clean 1 + Standard Clean 2) followed by Caro's acid (mixture of sulfuric acid and

hydrogen peroxide) and then HF (hydrofluoric acid) is performed on the initial substrate 11 prior to step b) of epitaxial growth of the c-SiC donor layer 110.

The growth is performed in an epitaxy chamber, at a temperature of 1650°C, with precursors such as silane (SiH₄) and propane (C₃H₈) or ethylene (C₂H₄), generating the c-SiC donor layer 110 with a thickness of 30 microns (growth rate: 10 microns/h). The donor layer has a BPD defect density of the order of 1/cm².

Hydrogen ions are implanted at an energy of 150 keV and a dose of 6E16 H+/cm² through the free surface of the donor layer 110. A buried brittle plane 12 is thus created at a depth of about 800 nm in the initial substrate 11.

A cleaning sequence of RCA + Caro's acid is performed on the donor substrate 111 so as to remove potential contaminants from the free face of the donor layer 110.

DLI-CVD deposition is performed on the donor layer 110, at a temperature of 800°C, with the disilabutane (DSB) precursor, at a pressure of 50 Torr, for 60 minutes, so as to reach a thickness of at least 150 microns for the carrier layer 20'. Under these conditions, the carrier layer 20' is deposited in the form of an amorphous SiC matrix, comprising reaction byproducts derived from the deposition precursors.

Annealing at 1000°C is then applied to the stack 211 for 50 minutes, and separation is performed on the buried fragile plane 12 during said annealing. On conclusion of this separation step e), the intermediate composite structure 1' formed of the thin layer 10 and of the carrier layer 20' is separated from the rest 111' of the donor substrate.

A crystallization heat treatment at 1200°C for 1 hour under an argon atmosphere is then applied to said intermediate composite

structure 1', to form the poly-SiC carrier substrate 20 of the composite structure 1.

Alternatively, the separation and the crystallization may be performed during the same heat treatment, for example at 1200°C under a neutral atmosphere.

Mechanical rectification of the rear face of the carrier substrate 20, removing about 15 to 30 microns, makes it possible to eliminate cracks and structural defects generated by the crystallization of the SiC matrix.

One or more mechanochemical polishing operations are then performed to restore the surface roughness of the thin layer 10 and of the rear face of the carrier substrate 20, followed by conventional cleaning sequences.

Needless to say, the invention is not limited to the described embodiments and examples, and implementation variants thereof may be envisaged without departing from the scope of the invention as defined by the claims.

CLAIMS

1. Process for manufacturing a composite structure comprising a thin layer of monocrystalline silicon carbide arranged on a carrier substrate made of silicon carbide, the process comprising:
 - a) a step of providing an initial substrate made of monocrystalline silicon carbide,
 - b) a step of epitaxial growth of a monocrystalline silicon carbide donor layer on the initial substrate, to form a donor substrate, the donor layer having a density of crystal defects less than that of the initial substrate,
 - c) a step of ion implantation of light species into the donor layer, to form a buried brittle plane delimiting the thin layer between said buried brittle plane and a free surface of said donor layer,
 - d) a step of direct liquid injection-chemical vapour deposition, at a temperature below 1000°C, to form a carrier layer directly on the free surface of the donor layer, said carrier layer being formed by an at least partially amorphous SiC matrix,
 - e) a step of separating along the buried brittle plane to form, on the one hand, an intermediate composite structure comprising the thin layer on the carrier layer and, on the other hand, the rest of the donor substrate,
 - f) a step of heat treatment at a temperature of between 1000°C and 1800°C, applied to the intermediate composite structure, to crystallize the carrier layer and to form the polycrystalline carrier substrate,
 - g) a step of mechanical and/or chemical treatment(s) of the composite structure, the treatment(s) being applied to a free face of the carrier substrate, the rear face of the composite structure, and/or to a free face of the thin layer, the front face of the composite structure.

2. Manufacturing process according to the preceding claim, in which the deposition step d) is performed at a temperature of between 100°C and 700°C, or even preferentially between 200°C and 600°C.
3. Manufacturing process according to either of the preceding claims, in which the deposition step d) is performed at a pressure of between 1 Torr and 500 Torr.
4. Manufacturing process according to any one of the preceding claims, in which the precursors used during the deposition step d) are chosen from polysilylethylene and disilabutane.
5. Manufacturing process according to any one of the preceding claims, in which, on conclusion of the deposition step d), the carrier layer has a thickness of greater than or equal to 10 microns, or even a thickness of greater than or equal to 50 microns, or even a thickness of greater than or equal to 100 microns, or even a thickness of greater than or equal to 200 microns.
6. Manufacturing process according to any one of the preceding claims, in which chemical etching, mechanical grinding and/or mechanochemical polishing is (are) applied to a free face of the carrier layer, between step d) and step e).
7. Manufacturing process according to any one of the preceding claims, in which step a) comprises the formation, on the initial substrate, of a monocrystalline conversion layer, to convert basal plane dislocation defects of the initial substrate into threading edge dislocation defects.

8. Manufacturing process according to any one of the preceding claims, in which the epitaxial growth step b) is performed at a temperature above 1200°C, preferentially between 1500°C and 1650°C.
9. Manufacturing process according to any one of the preceding claims, in which the separation step e) is performed at a temperature above the deposition temperature of step d).
10. Manufacturing process according to any one of Claims 1 to 8, in which the separation step e) takes place during the deposition step d), preferentially at the end of step d).
11. Manufacturing process according to any one of Claims 1 to 9, in which the separation step e) and the crystallization step f) are performed during the same heat treatment.
12. Manufacturing process according to any one of the preceding claims, in which step g) comprises simultaneous mechanochemical polishing of a front face and of a rear face of the composite structure.
13. Manufacturing process according to any one of the preceding claims, comprising a step of reconditioning the rest of the donor substrate for the purpose of reuse as initial substrate or as donor substrate.