Description

The invention relates to a method of storing words of *n* bits on and reproducing them from an optically readable record carrier, having the features of the preamble of claim 1.

The invention also relates to a record carrier for use in the method.

The invention also relates to a first apparatus for carrying out the method, comprising the features of the preamble of claim 14.

Moreover, the invention relates to a second apparatus for carrying out the method.

Such a method, record carrier and apparatus are known from Philips Technical Review, Vol. 40, 1982, No. 6, the complete issue, which issue is herewith incorporated by reference. Such apparatuses and record carriers are commercially available under the designation Compact Disk Digital Audio System and are used for reproducing audio information which is recorded on the optically readable record carrier in digitally coded form.

In the same way as audio cassettes such a record carrier may be used for the storage of other data, in particular computer data, such as computer programs and computer games. However, the risk of an erroneous n-bit word is too great for this purpose. In the case of digital audio said errors are largely masked by said interpolation, which is effective in the case of digital audio because adjacent words represent correlated signal values and the substitute signal value obtained through interpolation will generally be compatible with the original signal value. However, if as in the case of said computer data, the words are uncorrelated, the interpolation will result in a word which has no relation with the original word. Thus, for such a use interpolation is unlikely to improve the error probability.

It is the object of the invention to provide a method of the type mentioned in the opening paragraph which enables a simple storage and reproduction with a reduced error probability. The invention is embodied in the method, the record carrier and in the two apparatuses. The method in accordance with the invention is characterized by the features of the characterising part of claim 1.

The invention is based on the recognition that in this way using a standard compact-disk digital audio player including the interpolation circuit it is yet possible to store and reproduce data in a reliable manner because by repeating said groups at least three times and subsequently sampling them at the correct instant erroneous interpolation cannot be generated by interpolating at the sampling instant.

The record carrier for use in the inventive method is characterized by the features of the characterising part of claim 8.

The first apparatus of the type mentioned in the introductory part for carrying out the method in accordance with the invention is characterized by the features of the characterising part of claim 14.

The second apparatus for carrying out the method in accordance with the invention is characterized by the features of the characterising part of claim 17.

This second apparatus has the advantage that the first apparatus is obtained by connecting the second apparatus to the output of an existing player for audio-signal reproduction.

The method and the record carrier is further characterized in that the m most significant bits of the words of n bits directly constitute the data word of m bits.

In this way the data words can be recovered very simply from the output signal of the sampling circuit by means of an A/D converter.

In order to obtain clock information in a simple manner the method and the record carrier in accordance with the invention may further be characterized in that one bit of those n bits which are less significant than the m most significant bits represents the clock signal.

In this respect it is advantageous that the period of the clock signal corresponds to the duration of k words of n bits.

As a result of this step the frequency of this clock information is situated in a zero point of the data-information spectrum because the clock frequency is then 2x the repetition frequency of the data words.

This version of the method and the record carrier is further characterized in that k is an even number and the clock frequency is obtained in that the bit intended for the clock signal alternately assumes one of two logic levels every k/2 words of n bits.

Thus, a clock signal of a symmetrical shape, which is simple to be processed electronically, is obtained in the analog signal.

Specifically, a preferred version of the method and the record carrier in accordance with the invention is characterized in that $n = 16$ and $m = 10$, the clock signal is represented by the 13th bit, and the 11th and 12th bit have a fixed logic value, and that after sampling the signal is subjected to an analog-to-digital conversion.

For the recovery of the digital data words the first apparatus may further be characterized in that an analog-to-digital converter is arranged after the sampling circuit.

For the recovery of a clock signal the first apparatus may further be characterized in that the apparatus further comprises a filter which is tuned to the clock frequency and which is connected to the output of the digital-to-analog converter, and a phase-locked loop for deriving a clock frequency for controlling the sampling circuit from the analog signal, and the second apparatus may further be characterized in that the apparatus further comprises a filter which is tuned to the clock frequency and which is connected to the analog input, and a phase-locked loop for deriving a clock frequency for controlling the sampling circuit from the analog signal.

The invention will now be described in more detail, by way of example, with reference to the

accompanying drawings, in which

Figure 1 shows an apparatus for carrying out the method in accordance with the invention,

Figure 2 shows some diagrams to illustrate the operation of the interpolation circuit in said apparatus,

Figure 3 shows some diagrams to explain the operation of said apparatus.

Figure 1 shows an apparatus for carrying out the method in accordance with the invention. It comprises an optical read apparatus 1 which reads a disk-shaped record carrier 3, driven by a drive means 4, by means of a laser beam 2. The signal read is applied to a decoder circuit 5, in which the signal is modulated, arranged and subjected to an error correction process in conformity with the standard compact-disk digital audio system. On the outputs 16-bit digital audio signals appear for the left-hand channel (output 6) and for the right-hand channel (output 8), a reliability flag for the digital samples in the left-hand signal (output 7), a reliability flag for the digital samples in the right-hand channel (output 9) and a clock signal (output 10) representing the sampling frequency (44.1 kHz). These signals are applied to an interpolation circuit 11 which generates a new sample when the reliability flag indicates that this sample is unreliable. Moreover, the circuit 11 may be designed so that the signal is suppressed temporarily when too many unreliable samples appear, which depending on the version, may already be the case in the event of two consecutive erroneous samples. The output signal of the interpolation circuit 11, together with the sampling frequency, is applied to a D/A converter 12, which produces an analog signal on outputs 13 (left-hand channel) and 14 (right-hand channel), which converter also comprises a low-pass filter. So far the apparatus corresponds to a standard compact-disk digital audio player.

Figure 2 illustrates the operation of the interpolation circuit 11 when, in accordance with the invention, each sample is repeated at least three times. Figure 2a shows these samples S_1, S_2 and S_3 with corresponding analog signal values A_3 followed by three samples S_4, S_5 and S_6 with the analog signal values A_1. When the reliability flag indicates that sample S_3 is unreliable a sample S_{30} is generated with a corresponding analog signal value $A_2 = \frac{1}{2}(A_1 + A_3)$ between the analog signal values of the samples S_2 and S_4. If as indicated in Figure 2b the sample S_2 is unreliable, the interpolation circuit substitutes it by the sample S_{20} of a corresponding signal value between the signal values of the samples S_1 and S_3 and consequently identical to the sample S_2. When a sample is repeated three times the central sample is always correct in the case of interpolation of one erroneous sample, regardless of which sample is obtained by interpolation.

Figures 2c and 2d represent a situation in which the samples are repeated four times. Four identical samples S_1 to S_4 are shown, followed by four identical samples S_5 to S_8 of corresponding signal values A_3 and A_1, respectively. In Figure 2c it is assumed that the sample S_4 is incorrect. The interpolation circuit then generates a sample S_{40} of the analog signal value A_2. In the situation of Figure 2d it is assumed that the sample S_3 is not correct. The interpolation circuit then generates as identical sample S_{30}. Both the sample S_2 and S_3 remain correct regardless of the place of an incorrect sample.

In general it is therefore correct to state that when each sample is repeated at least three times the corresponding analog signal values within each block of repeated samples are correct in the range which is situated within the limits of each block at least at a time interval equal to the repetition period of the samples provided that the number of consecutive erroneous samples is not greater than two, although these situations may also turn out to be correct in the case of a corresponding extension of the blocks and the interpolation period. For example, two consecutive incorrect samples upon insertion of the samples by interpolation do not present problems when each sample is repeated five times or more.

The invention is based on the insights outlined in the foregoing. The apparatus shown in Figure 1 therefore comprises a sampling circuit 15 for sampling the analog output signals on outputs 13 and 14 (in principle it is also possible to use only one of the two channels) at the correct instants. For this purpose a clock signal is derived from the analog signal on output 14, for example by means of a phase-locked loop 16. The output signal on the output of the sampling circuit 15 is converted into a digital code by means of an analog-to-digital converter 17, which code appears on output 18 (left-hand channel) and 19 (right-hand channel) together with the clock signal on output 20.

Figure 3 illustrates the operation by means of example where 2-bit data words are stored *via* 4-bit samples which are repeated three times. Figure 3a shows three consecutive data words 11, 01 and 10. They may be represented by a selection of one out of four analog signal values A_0, A_1, A_2 and A_3. In the case of a selection in accordance with a binary series the values A_0, A_1, A_2 and A_3 respectively correspond to the data words 00, 01, 10 and 11 and may therefore be recorded directly on the record carrier as two bits of samples S. When each sample is repeated three times the pattern shown in Figure 3b is obtained. After read-out and digital-to-analog conversion the pattern, in conformity with the invention, should be sampled at the location of the samples S_2, S_5, S_8. For this purpose a clock signal as shown in Figure 3c may be provided, which signal comprises one bit which assumes the logic value 1 at the location of the samples S_2, S_5, S_8. This bit may be added to the samples S at some distance (for example, one bit) as a less-significant bit, so that four-bit samples are obtained. After read-out and demodulation this yields the signal shown in Figure 3d on the output of the demodulator 5. It is now assumed that the samples S_3 and S_8 are incorrect. The interpolation circuit 11 then inserts a sample

of the corresponding analogue signal value A_2 instead of A_1 for the sample S_3, whilst of the sample S_8 the clock modulation disappears. Thus, a signal as shown in Figure 3e appears on the output of the interpolation circuit 11, which signal is converted into a signal as shown in Figure 3f (when the filtration is ignored) by the D/A converter 12, which signal has the incorrect value A_2 at the location of sample S_3 and from which the clock modulation is missing at the location of the sample S_8. By means of the filter and phase-locked loop circuit 16 the clock signal is derived (Figure 3g), said phase-locked loop inserting the missing clock pulse at the location of the sample S_8 without any problems. After sampling the signal shown in Figure 3h is obtained on the output of this sampling circuit 15, which signal is converted into the logic signal shown in Figure 3i by the A/D converter 17, the A/D converter in the present example being a two-bit converter because the two least-significant bits need not be converted. Thus, the erroneous samples S_2 and S_8 do not disturb the reproduction of the logic signal shown in Figure 3a.

In the present example a repetition of three times is used. In a practical example, in which 10-bit data words are accommodated in 16-bit samples as most significant bits, the clock modulation being applied to the 13th bit (note that the clock modulation must be added to only one of the two stereo channels when the information in the two channels allows this), a repetition of four times is chosen because then a symmetrical clock may be used with a change of the logic level after every 2nd bit, *i.e.* in the example shown in Figure 3c between the samples S_2 and S_3, S_4 and S_5, S_6 and S_7, etc., which simplifies the logic. It is to be noted that a repetition of four or more times is advantageous in comparison with three times repetition because in the case of three times repetition sampling must be effected exactly at the central bit group, which imposes stringent requirements on the stability of the clock signal. The choice of a clock with a frequency which is twice as high as the repetition frequency of the data words (Figure 3i) moreover has the advantage that this clock then appears in a zero point of the frequency spectrum of the data words.

In the manner described in the foregoing a standard compact-disk digital audio player may be adapted for the transfer of data signals, in particular non-intercorrelated data words, without modifying the player, in which case the error probability would be too high if no additional steps were taken. Because in general said player is already in use for audio purposes, it may be advantageous to design an adaptor comprising the sampling circuit 15, the phase-locked loop 16 and the analog-to-digital converter 17.

Obviously, it is possible to achieve an additional error correction in the coding of the data words themselves by means of parity bits and the like.

In the apparatus 5 the samples are provided with a reliability flag. In principle, it would therefore be possible to select always a reliable sample from the groups of three or more samples without the use of the inventive principle. However, then it is necessary to equip the player with an output such that the interpolation circuit 11 has no undesired effects, but this has the disadvantage that for this purpose standard compact-disk digital audio players have to be modified. By way of illustration Figure 1 shows such a modification. For this purpose the outputs 6 to 9 of the decoder device 5 are connected to a selection device 21 in which from each group one reliable sample is selected, which directly in digital form is applied to an output 22 (left-hand channel) and 23 (right-hand channel) respectively. All 16 bits of each sample may then be utilized for the data word. For the purpose of synchronization the sampling frequency on the output 10 of the demodulation circuit is divided by the number of samples per data word by means of a divider stage 22, steps being taken to ensure the correct phase relationship. This clock frequency is also applied to an output 25. The player thus modified is suitable for use with record carriers in which all 16 bits are employed for data storage.

The complete apparatus shown in Figure 1 may be advantageous because it is suitable for both systems and, if desired, for audio reproduction.

In principle, it is also possible to store and reproduce one-bit data words. The A/D converter 17 is then a one-bit converter or discriminator.

Claims

1. A method of storing words of n bits on and reproducing them from an optically readable record carrier, which words each represent an analog signal value, in which words are recovered from a signal obtained by reading said record carrier during reproduction, after which said words are subjected to an interpolation process, in which a word to be substituted for an unreliable word is generated from the words situated on both sides of the unreliable word by interpolation of said words and subsequently to a digital-to-analog conversion for converting said words into the corresponding analog signals characterized in that each n-bit word is stored k times on the record carrier in such a way that after said digital-to-analog conversion a group of k consecutive analog signals is yielded, each of these signals representing the n-bit word, in that each group of k signals is sampled at an instant situated at least one n-bit word time interval from both the beginning and the end of said group and in that the sampled signal is converted into an m-bit data word, whereby $k \geq 3$ and $1 \leq m \leq n$.

2. A method as claimed in Claim 1, characterised in that $m < n$ and that the m most-significant bits of the words of n bits directly constitute the data word of m bits.

3. A method as claimed in Claim 2, characterized in that one bit of those n bits, which are less significant than the m most significant bits is used for the representation of a clock signal.

of the corresponding analogue signal value A_2 instead of A_1 for the sample S_3, whilst of the sample S_8 the clock modulation disappears. Thus, a signal as shown in Figure 3e appears on the output of the interpolation circuit 11, which signal is converted into a signal as shown in Figure 3f (when the filtration is ignored) by the D/A converter 12, which signal has the incorrect value A_2 at the location of sample S_3 and from which the clock modulation is missing at the location of the sample S_8. By means of the filter and phase-locked loop circuit 16 the clock signal is derived (Figure 3g), said phase-locked loop inserting the missing clock pulse at the location of the sample S_8 without any problems. After sampling the signal shown in Figure 3h is obtained on the output of this sampling circuit 15, which signal is converted into the logic signal shown in Figure 3i by the A/D converter 17, the A/D converter in the present example being a two-bit converter because the two least-significant bits need not be converted. Thus, the erroneous samples S_2 and S_8 do not disturb the reproduction of the logic signal shown in Figure 3a.

In the present example a repetition of three times is used. In a practical example, in which 10-bit data words are accommodated in 16-bit samples as most significant bits, the clock modulation being applied to the 13th bit (note that the clock modulation must be added to only one of the two stereo channels when the information in the two channels allows this), a repetition of four times is chosen because then a symmetrical clock may be used with a change of the logic level after every 2nd bit, *i.e.* in the example shown in Figure 3c between the samples S_2 and S_3, S_4 and S_5, S_6 and S_7, etc., which simplifies the logic. It is to be noted that a repetition of four or more times is advantageous in comparison with three times repetition because in the case of three times repetition sampling must be effected exactly at the central bit group, which imposes stringent requirements on the stability of the clock signal. The choice of a clock with a frequency which is twice as high as the repetition frequency of the data words (Figure 3i) moreover has the advantage that this clock then appears in a zero point of the frequency spectrum of the data words.

In the manner described in the foregoing a standard compact-disk digital audio player may be adapted for the transfer of data signals, in particular non-intercorrelated data words, without modifying the player, in which case the error probability would be too high if no additional steps were taken. Because in general said player is already in use for audio purposes, it may be advantageous to design an adaptor comprising the sampling circuit 15, the phase-locked loop 16 and the analog-to-digital converter 17.

Obviously, it is possible to achieve an additional error correction in the coding of the data words themselves by means of parity bits and the like.

In the apparatus 5 the samples are provided with a reliability flag. In principle, it would therefore be possible to select always a reliable sample from the groups of three or more samples without the use of the inventive principle. However, then it is necessary to equip the player with an output such that the interpolation circuit 11 has no undesired effects, but this has the disadvantage that for this purpose standard compact-disk digital audio players have to be modified. By way of illustration Figure 1 shows such a modification. For this purpose the outputs 6 to 9 of the decoder device 5 are connected to a selection device 21 in which from each group one reliable sample is selected, which directly in digital form is applied to an output 22 (left-hand channel) and 23 (right-hand channel) respectively. All 16 bits of each sample may then be utilized for the data word. For the purpose of synchronization the sampling frequency on the output 10 of the demodulation circuit is divided by the number of samples per data word by means of a divider stage 22, steps being taken to ensure the correct phase relationship. This clock frequency is also applied to an output 25. The player thus modified is suitable for use with record carriers in which all 16 bits are employed for data storage.

The complete apparatus shown in Figure 1 may be advantageous because it is suitable for both systems and, if desired, for audio reproduction.

In principle, it is also possible to store and reproduce one-bit data words. The A/D converter 17 is then a one-bit converter or discriminator.

Claims

1. A method of storing words of n bits on and reproducing them from an optically readable record carrier, which words each represent an analog signal value, in which words are recovered from a signal obtained by reading said record carrier during reproduction, after which said words are subjected to an interpolation process, in which a word to be substituted for an unreliable word is generated from the words situated on both sides of the unreliable word by interpolation of said words and subsequently to a digital-to-analog conversion for converting said words into the corresponding analog signals characterized in that each n-bit word is stored k times on the record carrier in such a way that after said digital-to-analog conversion a group of k consecutive analog signals is yielded, each of these signals representing the n-bit word, in that each group of k signals is sampled at an instant situated at least one n-bit word time interval from both the beginning and the end of said group and in that the sampled signal is converted into an m-bit data word, whereby $k \geq 3$ and $1 \leq m \leq n$.

2. A method as claimed in Claim 1, characterised in that $m < n$ and that the m most-significant bits of the words of n bits directly constitute the data word of m bits.

3. A method as claimed in Claim 2, characterized in that one bit of those n bits, which are less significant than the m most significant bits is used for the representation of a clock signal.

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4. A method as claimed in Claim 3, characterized in that the period of the clock signal corresponds to the duration of k words of n bits.

5. A method as claimed in Claim 4, characterized in that k is an even number and the clock frequency is obtained in that the bit intended for the clock signal alternately assumes one of two logic levels every k/2 words of n bits.

6. A method as claimed in Claim 3, 4 or 5, characterized in that n = 16 and m = 10, the clock signal is represented by the 13th bit, and the 11th and 12th bit have a fixed logic value.

7. A method as claimed in any one of Claims 1 to 6, characterized in that after sampling the signal is subjectd to an analog-to-digital conversion.

8. A record carrier for use in the method as claimed in any of the Claims 1 to 7, characterized in that each of the n-bit words is stored k times on the record carrier in such a way that after said digital-to-analog conversion a group of k consecutive analog signals is yielded, each of these signals representing the n-bit word.

9. A record carrier as claimed in Claim 8, characterized in that the m most-significant bits of the words of n bits directly constitute the data word of m bits.

10. A record carrier as claimed in Claim 9, characterized in that one bit of those n bits which are less significant than the m most significant bits represents a clock signal.

11. A record carrier as claimed in Claim 10, characterized in that the period of the clock signal corresponds to the duration of k words of n bits.

12. A record carrier as claimed in Claim 11, characterized in that k is an even number and the clock signal is obtained in that the bit intended for the clock signal alternately assumes one of two logic values evry k/2 words of n bits.

13. A record carrier as claimed in Claim 10, 11 or 12, characterized in that n = 16 and m = 10, the clock signal is represented by the 13th bit and the 11th and 12th bit have a fixed logic value.

14. An apparatus for carrying out the method as claimed in any one of the Claims 1 to 7, comprising a read apparatus (1), a decoding circuit (5) for recovering words of n bits which each represent an analog signal value from the signal read, an interpolation circuit (11) for generating a substitute word for an unreliable word by interpolation of the words situated on both sides of said unreliable word, and a digital-to-analog converter (12) for converting said words into the corresponding analog signals, characterized by a sampling circuit (15) for sampling each group of k signals at an instant which is situated at least one n-bit word time interval from both the beginning and the end of said group.

15. An apparatus as claimed in Claim 14, characterized in that an analog-to-digital converter (17) is arranged after the sampling circuit (15).

16. An apparatus as claimed in Claim 14 or 15, characterized in that the apparatus further comprises a filter which is tuned to the clock frequency and which is connected to the output of the digital-to-analog converter, and a phase-locked loop (16) for deriving a clock frequency for controlling the sampling circuit (15) from the analog signal.

17. An apparatus for carrying out the method as claimed in any one of the Claims 1 to 7, characterized in that the apparatus is provided with an input for receiving the output signal from a standard compact-disk digital audio player, a sampling circuit (15) for sampling each group of k signals at an instant which is situated at least one n-bit word time interval from both the beginning and the end of said group, an analog-to-digital converter (17) whose input is connected to the output of the sampling circuit (15), and an output for a digital signal, which output is connected to the output of the analog-to-digital converter (17).

18. An apparatus as claimed in Claim 17, characterized in that the apparatus further comprises a filter which is tuned to the clock frequency and which is connected to the analog input, and a phase-locked loop (16) for deriving a clock frequency for controlling the sampling circuit (15) from the analog signal.

Patentansprüche

1. Verfahren zum Aufzeichnen von Worten von n Bits auf und zum Wiedergeben dieser Worte von einem optisch lesbaren Aufzeichnungsträger, wobei diese Worte je einen analogen Signalwert darstellen und aus einem Signal wiedergewonnen werden, das durch das Lesen des Aufzeichnungsträgers bei der Wiedergabe erhalten wird, wonach die Worte einem Interpolationsvorgang unterworfen werden, wobei ein gegen ein unzuverlässiges Wort zu ersetzendes Wort aus den an beiden Seiten des unzuverlässigen Worts befindlichen Worten durch Interpolation dieser Wörter und durch nachfolgende Digital/Analog-Wandlung zum Umsetzen dieser Wörter in die entsprechenden analogen Signale abgeleitet wird, dadurch gekennzeichnet, dass jedes n Bit-Wort k-mal auf dem Aufzeichnungsträger aufgezeichnet wird, derart dass nach der genannten digitalen/analogen Wandlung eine Gruppe von k aufeinanderfolgenden analogen Signale gewonnen wird, wobei jedes dieser Signale das n-Bit-Wort darstellt, dass jede Gruppe von k Signalen zu einem Zeitpunkt wenigstens ein n-Bit-Wortzeitintervall sowohl vom Anfang als auch vom Ende der Gruppe abgetastet wird und dass das abgetastete Signal in ein m-Bit-Datenwort umgewandelt wird, wobei $k \geq 3$ und $1 \leq m \leq n$ sind.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, dass $m < n$ ist, und dass die m Bits mit grösster Wertigkeit in den Worten von b Bits das Datenwort von m Bits direckt darstellen.

3. Verfahren nach Anspruch 2, dadurch gekennzeichnet, dass ein Bit dieser n Bits mit geringerer Wertigkeit als die m Bits mit grösster Wertigkeit für die Darstellung eines Taktsignals verwendet wird.

4. Verfahren nach Anspruch 3, dadurch gekenn-

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zeichnet, dass die Periode des Taktsignals der Dauer von k Worten von n Bits entspricht.

5. Verfahren nach Anspruch 4, dadurch gekennzeichnet, dass k eine gerade Zahl und die Taktfrequenz dadurch erhalten wird, dass das Bit für das Taktsignal abwechselnd nach jeweils k/2 Worten von je n Bits einen von zwei logischen Pegeln annimmt.

6. Verfahren nach Anspruch 3, 4, oder 5, dadurch gekennzeichnet, dass n = 16 und m = 10 sind, das Taktsignal durch das 13. Bit dargestellt wird und die 11. and 12. Bits einen festen logischen Wert haben.

7. Verfahren nach einem oder mehreren der Ansprüche 1 bis 6, dadurch gekennzeichnet, dass nach dem Abtasten das Signal einer Analog/Digital-Wandlung unterworfen wird.

8. Aufzeichnungsträger zur Verwendung beim Verfahren nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, dass jedes der n-Bit-Worte k-mal auf dem Aufzeichnungsträger derart aufgezeichnet wird, dass nach der Digital-Analog-Wandlung eine Gruppe von k aufeinanderfolgenden analogen Signalen gewonnen wird, wobei jedes dieser Signale das n-Bit-Wort darstellt.

9. Aufzeichnungsträger nach Anspruch 8, dadurch gekennzeichnet, dass die m Bits mit grösster Wertigkeit in den Worten von n Bits das Datenwort von m Bits direkt darstellen.

10. Aufzeichnungsträger nach Anspruch 9, dadurch gekennzeichnet, dass ein Bit dieser n Bits mit geringerer Wertigkeit als die m Bits mit grösster Wertigkeit ein Taktsignal darstellt.

11. Aufzeichnungsträger nach Anspruch 10, dadurch gekennzeichnet, dass die Periode des Taktsignals die Dauer von k Worten von n Bits entspricht.

12. Aufzeichnungsträger nach Anspruch 11, dadurch gekennzeichnet, dass k eine gerade Zahl ist und das Taktsignal derart erhalten wird, dass das für das Taktsignal vorgesehene Bit abwechselnd nach jeweils k/2 Worten von n Bits einen von zwei logischen Werten annimmt.

13. Aufzeichnungsträger nach Anspruch 10, 11 oder 12, dadurch gekennzeichnet, dass n = 16 und m = 10 sind, das Taktsignal durch das 13. Bit dargestellt wird und die 11. und 12. Bits einen festen logischen Wert haben.

14. Gerät zur Durchführung des Verfahrens nach einem oder mehreren der Ansprüche 1 bis 7, mit einen Lesegerät (1), einem Decoder (5) zur Wiedergewinnung von Worten von n Bits, die je einen analogen Signalwert aus dem gelesenen Signal darstellen, einem Interpolationskreis (11) zum Erzeugen eines Ersatzworts für ein unzuverlässiges Wort durch Interpolation der an beiden Seiten des unzuverlässigen Worts befindlichen Worte und einem Digital-Analog-Wandler (12) zum Umsetzen der Worte in die entsprechenden analogen Signale, dadurch gekennzeichnet, dass ein Abtastkreis (15) zum Abtasten jeder Gruppe von k Signalen zu einem Zeitpunkt wenigstens ein n-Bit-Wortzeitintervall sowohl vom Anfang als auch vom Ende der Gruppe vorgesehen ist.

15. Gerät nach Anspruch 14, dadurch gekennzeichnet, dass ein Analog/Digital-Wandler (17) dem Abtastkreis (15) nachgeschaltet ist.

16. Gerät nach Anspruch 14 oder 15, dadurch gekennzeichnet, dass das Gerät weiter ein auf die Taktfrequenz abgestimmtes Filter, das an den Ausgang des Digital/Analog-Wandlers angeschlossen ist, und eine Phasenverriegelungsschleife (16) zum Ableiten einer Taktfrequenz aus dem analogen Signal zur Steuerung des Abtastkreises (15) enthält.

17. Gerät zur Durchführung des Verfahrens nach einem oder mehreren der Ansprüche 1 bis 7, dadurch gekennzeichnet, dass das Gerät mit einem Eingang zum Empfangen des Ausgangssignals aus einem Standard-Compact-Disk-Digital-Audio-Spielers, mit einem Abtastkreis (15) zum Abtasten jeder Gruppe von k Signalen zu einem Zeitpunkt wenigstens ein n-Bit-Wortzeitintervall sowohl vom Anfang als auch vom Ende der genannten Gruppe, mit einem Analog/Digital-Wandler (17), dessen Eingang an den Ausgang des Abtastkreises (15) angeschlossen ist, und mit einem Ausgang für ein digitales Signal versehen ist, dessen Ausgang an den Ausgang des Analog/Digital-Wandlers (17) angeschlossen ist.

18. Gerät nach Anspruch 17, dadurch gekennzeichnet, dass das Gerät weiter ein auf die Taktfrequenz abgestimmtes Filter, das an den analogen Eingang angeschlossen ist, und eine Phasenverriegelungschleife (16) zum Ableiten einer Taktfrequenz aus dem analogen Signal zur Steuerung des Abtastkreises (15) enthält.

Revendications

1. Procédé pour le stockage de mots de *n* bits dans, et leur reproduction à partir d'un support d'enregistrement lisible par voie optique, mots qui représentent chacune une valeur de signal analogique, lesdits mots étant récupérés à partir d'un signal obtenu par lecture dudit support d'enregistrement pendant la reproduction, après quoi lesdits mots sont soumis à une procédé d'interpolation, selon lequel un mot à substituer à mot non fiable est engendré à partir des mots situés des deux côtés du mot non fiable par interpolation desdits mots et ensuite une conversion numérique analogique, afin de convertir lesdits mots en signaux analogiques correspondants, caractérisé en ce que chaque mot de n bits est stocké k fois dans le support d'enregistrement de façon à obtenir, après ladite conversion numérique-analogique, un groupe de k signaux analogiques successifs, chacun de ces signaux représentant le mot de n bits, de façon que chaque groupe de k signaux est échantillonné à un instant éloigné d'un intervalle de temps d'au moins un mot à n bits tant du début que de la fin de chaque groupe et que chaque signal échantillonné est converti en un mot de données à m bits avec $k \geq 3$ et $1 \leq m \leq n$.

2. Procédé selon la revendication 1, caractérisé en ce que $m < n$ et en ce que les m bits les plus signifiants des mots de n bits constituent de façon directe le mot de données de m bits.

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3. Procédé selon la revendication 2, caractérisé en ce qu'un bit des n bits, qui sont moins signifiants que les m bits les plus signifiants, est utilisé pour la représentation d'un signal d'horloge.

4. Procédé selon la revendication 3, caractérisé en ce que la periode du signal d'horloge correspond à la durée de k mots de n bits.

5. Procédé selon la revendication 4, caractérisé en ce que k est un nombre pair et a fréquence d'horloge est obtenue du fait le bit destiné au signal d'horloge prend alternativement l'un de neux niveaux logiques, tout les k/2 mots de n bits.

6. Procédé selon la revendication 3, 4, ou 5, caractérisé en ce que n = 16, m = 10, le signal d'horloge est représenté par le 13ième bit, et le 11ième et le 12ième bit présentent une valeur logique fixe.

7. Procédé selon l'une des revendications 1 à 6, caractérisé en ce qu'après l'échantillonnage, le signal est soumis à une conversion analogique-numérique.

8. Support d'enregistrement à utiliser dans le procédé selon l'une des revendications 1 à 7, caractérisé en ce que chacun des mots à n bits est stocké k fois dans le support d'enregistrement de façon à obtenir, après ladite conversion numérique-analogique, un groupe de k signaux analogiques successif, chacun de ses signaux représentant le mot à n bits.

9. Support d'enregistrement selon la revendication 8, caractérisé en ce que les m bits les plus signifiants des mots de n bits constituent de façon directe le mots de données de m bits.

10. Support d'enregistrement selon la revendication 9, caractérisé en ce que un bit des n bits, qui sont moins signifiants que les m bits les plus signifiants représente un signal d'horloge.

11. Support d'enregistrement selon la revendication 10, caractérisé en ce que la période du signal d'horloge correspond à la durée de k mots de n bits.

12. Support d'enregistrement selon la revendication 11, caractérisé en ce que k est un nombre pair et le signal d'horloge est obtenu du fait que le bit destiné au signal d'horloge prend alternativement l'une des deux valeurs logiques, tous les k/2 mots de n bits.

13. Support d'enregistrement selon la revendication 10, 11 ou 12, caractérisé en ce que n = 16 et m = 10, le signal d'horloge étant représenté par le 13ième bit et le 11ième et 12ième bit présentent une valeur logique fixe.

14. Dispositif pour la mise en oeuvre du procédé selon l'une des revendications 1 à 7, comportant un appareil de lecture (1), un circuit de décodage (5) pour la récuperation de mots de n bits, qui présentent chacun une valeur de signal analogique, à partir du signal lu, un circuit d'interpolation (11) pour la formation d'un mot de représentation pour un mot non fiable par interpolation des mots situés des deux côtés dudit mot non fiable, et un convertisseur numérique-analogique (12) pour la conversion desdits mots en les signaux analogiques correspondants, caractérisé par un circuit d'échantillonnage (15) pour l'échantillonnage de chaque groupe de k signaux à un moment qui est éloigné d'un intervalle d'une durée d'un mot à n bits tant du début que de la fin dudit groupe.

15. Dispositif selon la revendication 14, caractérisé en ce qu'un convertisseur analogique-numérique (17) est disposé après le circuit d'échantillonnage (15).

16. Dispositif selon la revendication 14 ou 15, caractérisé en ce que le dispositif comporte en outre un filtre qui est destiné à la fréquence d'horloge et qui est connecté à la sortie d'un convertisseur numérique-analogique et une boucle à blocage de phase 16 pour recupérer la fréquence d'horloge pour la commande du circuit d'échantillonnage (15) à partir du signal analogique.

17. Appareil pour la mise en oeuvre du procédé selon l'une des revendications 1 à 7, caractérisé en ce que le dispositif est muni d'une entrée pour la réception du signal de sortie à partir d'un lecteur audio numérique de disque compact standard, un circuit d'échantillonnage (15) pour l'échantillonnage de chaque groupe de k signaux à un moment qui est éloigné d'au moins un intervalle de temps d'un mot à n bits tant du début que de la fin dudit groupe, un convertisseur analogique-numérique (17), dont l'entrée est connectée à la sortie du circuit d'échantillonnage (15) et une sortie d'un signal numérique, sortie qui est connectée à la sortie du convertisseur analogique-numérique (17).

18. Dispositif selon la revendication 17, caractérisé en ce que le dispositif comporte en outre un filtre, qui est destiné à la fréquence d'horloge et qui est connecté à l'entrée analogique, et une boucle à blocage de phase (16) pour récupérer une fréquence d'horloge pour la commande du circuit d'échantillonnage (15) à partir du signal analogique.

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