"Semiconductor Integrated Circuit Device and a method of manufacture thereof".

The present invention relates to a semiconductor integrated circuit device (which will be shortly referred to "IC"), which includes a unit cell for forming such an input/output circuit portion as is made capable of selecting any of a plurality of different input and output functions by changing a wiring pattern, and to a method of manufacturing the semiconductor integrated circuit device. More particularly, the present invention relates to a logical IC resorting to a master slice approach.

For example, a logical IC for a computer adopts the so-called "master slice approach" as its design because it is necessary to design a few but multiple kinds of ICs within a short period of time. The IC resorting to the master slice approach has an advantage that it can realize a multiplicity of logical functions by changing not the basic design (i.e., the master) but only the wiring pattern. In order to enjoy this

advantage, it is necessary that the functions of respective pins (or leads) can be so arbitrarily selected or changed as to satisfy the various requirements. Specifically, the functions of the respective pins are so required that they can be set in a master slice manner to any one function that is arbitrarily selected from the respective functions of an input, an output and bidirectionally of the input and output.

In order to satisfy this requirement, according to the prior art, there is adopted means for providing one I/$\bar{O}$ cell for each of the bonding pads which are provided for each pin. In this context an I/$\bar{O}$ cell is a cell (i.e., a unit circuit portion) which is so basically designed that it can simultaneously construct circuits requiring the largest number of the elements for the respective input and output circuits. In the case where the above mentioned requirements are to be satisfied by providing such I/$\bar{O}$ cell, this I/$\bar{O}$ cell is so formed that it can set the function of one pad (or pin) at any of the input, the output, and bidirectionally of the input and output so as to fabricate the IC resorting to the master slice approach. As a result, the element for realizing the function other than the selected one is not used, but one I/$\bar{O}$ cell performs nothing but one selected function. In the relationship in the arrangement between the

conventional bonding pad and I/Ō cell according to the prior art, moreover, although the input circuit and the output circuit can naturally be simultaneously constructed of one I/Ō cell independently of each other, both the input and output cannot be extracted separately and independently of each other, but only either of them can be extracted from the single I/Ō cell. With this in mind, we have investigated and revealed that the approach thus far described, i.e., the conventional master slice approach, in which the requirements for setting the functions of the pins is to be satisfied by providing one I/Ō cell for one pad, has failed to increase the multiple functions and kinds without changing the basic design.

Accordingly, it is an object of the present invention to provide an IC, which is intended to cope with the increase in the multiple kinds by increasing the degree of freedom in the design of an IC of the master slice approach so that any of an input, an output, bidirectionally of the input and output, and independent input and output can be arbitrarily selected as the function of one I/Ō cell, and also a method of manufacturing the IC.

Another object of the present invention is to make effective use of the I/Ō cell without any change in the same basic design as that of the prior

art especially in the logic IC fabricated by the matter slice approach.

According to one aspect of the present invention there is provided an integrated circuit device including:

(a) a semiconductor body;

(b) a plurality of unit cells formed on the semiconductor body, each of which includes predetermined circuit elements for providing at least one of two different functions of a first circuit and a second circuit,

the plurality of unit cells including a first set of unit cells of the first circuits, a second set of unit cells of the second circuits and a third set of unit cells, each of which independently has the two functions of the first and second circuits, the third set of unit cells including at least one member; and

(c) a wiring pattern for providing each of the unit cells with a respective predetermined circuit function.

According to a second aspect of the present invention there is provided a method of manufacturing an integrated circuit device, including the steps of:

(a) forming a plurality of units cells, each of which includes a plurality of circuit elements;

(b) connecting at least some of the circuit elements of each of the unit cells in a pattern so as to provide a respective predetermined circuit function; and

(c) forming a bonding pad for each of some of the connected unit cells and two bonding pads for each of the other of the connected unit cells.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, in which the present invention is applied to a logical LSI resorting to a master slice approach, e.g., a logical IC of CMOS (i.e. Complementary Metal Oxide Semiconductor) type and having several thousands of logical gates, and

wherein:-

Figure 1 is a top plan view schematically showing the layout of a preferred form of a CMOS type logical IC;

Figure 2A is a top plan view showing the unit cell for the logical circuit;

Figure 2B is a diagram showing an equivalent circuit of the unit cell;

Figure 3A is a top plan view showing a first preferred form of an I/$\bar{O}$ cell;

Figure 3B is a top plan view in the case where a first layered aluminium wiring is applied to the layout of the I/$\bar{O}$ cell shown in Figure 3A;

Figure 3C is a top plan view in the case where a second layered aluminium wiring is applied to the layout of the I/$\bar{O}$ cell shown in Figure 3B;

Figure 4 is a sectional view showing an essential portion of Figure 3C;

Figure 5A is a diagram showing an equivalent circuit of the I/$\bar{O}$ cell of Figure 3C;

Figure 5B is a circuit diagram showing the equivalent circuit in circuit symbols;

Figures 6A, 6B and 6C are circuit diagrams showing I/$\bar{O}$ cells according to second, third and fourth embodiments, respectively; and

Figure 7 is a sectional view showing an

essential portion of Figure 6A.

Figure 1 schematically shows the layout of a semiconductor chip 1 which constitutes a logical IC. In this chip 1, there are transversely arranged in one hundred and several tens of rows a number of unit cells 2, which constitute the logical circuit, forming rows of unit cells 3, and these unit cell rows 3 are longitudinally arranged in several tens of rows at a predetermined interval. Although several unit cells 2 are specifically illustrated in the drawing, the portions in the other unit cell rows 3 are identical, and the illustration of the unit cells is omitted for the sake of clarity. Although only four rows of the unit cells are shown, the other unit cell rows are also similar, and likewise they have been omitted. The interspaces between any adjacent two of the unit cell rows are used as wiring channels 4, each of which has such a width as can be formed on a surface of a field $SiO_2$ film with several tens of aluminium wires extending in the longitudinal direction. In the peripheral portion of the chip 1, there are arranged a number of $I/\overline{O}$ cells 5 which constitute input and output circuits. The $I/\overline{O}$ cells have a variety of circuit functions e.g. as an input circuit, an output circuit, a clock input circuit, a bidirectional buffer circuit and interconnected by aluminium wiring as will be

described hereinafter. At a position adjacent to each I/$\bar{O}$ cell, there are formed for each cell two bonding pads 6a and 6b which are arranged at a predetermined regular pitch. This provision of two bonding pads for each cell plays an important role for extracting the above referred to various circuit functions.

The procedure for forming the logical IC in accordance with the master slice approach will now be described. First of all, the circuit elements of the unit cells 2 and the I/$\bar{O}$ cells 5, i.e. MIS (i.e. Metal Insulator Semiconductor) type field effect transistors (i.e. MISFETs), resistors, polysilicon gate wires and so on are formed in accordance with the basic design (i.e. the master). The basic design is not changed but retains an identical pattern for all kinds. Next, after the whole surface has been covered with a phosphor silicate glass film (which will be referred to as a "PSG film") as an interlayer insulating film, this interlayer insulating film is formed with respective contact holes. After this step of forming the contact holes, various modifications conforming to desired logical functions are made so as to realize the functions. Next, a first-layered aluminium wiring (which will be referred to as "Al-I") is applied to the upper surface. This Al-I includes the wirings for constructing the logical circuits in the unit

cells 2, the power source ($V_{DD}$ and $V_{SS}$) wirings (which are of all kinds and in an identical pattern) for the unit cells 2, the wirings which constitute the input/output circuits in the I/$\bar{O}$ cells 5, and the wirings extending in the longitudinal direction on the wiring channels 4 in order to connect the unit cells 2. Moreover, the surface underlying the two bonding pads 6a and 6b provided for each I/$\bar{O}$ cell 5 is made of the Al-I. Next, after coverage has been made with a second-layered interlayer insulating film (i.e., a PSG film), respective through holes are formed therein, and a second-layered aluminium wiring (which will be shortly referred to as "Al-II") is applied. This Al-II includes the power source wirings (which are of all kinds and in an identical pattern) for the I/$\bar{O}$ cells 5, the wirings extending on the unit cells 2 in a direction to intersect the wiring channels 4 to connect the plural unit cells 2 in order to constitute the logical circuits, and the pad layers overlaid in an identical pattern on the above referred to Al-I so as to form an upper layer overlying the bonding pads 6a and 6b.

The unit cells 2 are so basically designed that each cell can constitute three-input CMOS type NAND gates at the maximum, and each of them is equipped therefor with three P-channel MISFETs and three N-channel MISFETs.

As one example for constructing a logical circuit by the use of those unit cells, the layout in the case where three input NAND gates are constructed is shown in Figure 2A, and the circuit diagram thereof is shown in Figure 2B. In order to effect the circuit design according to the master slice approach, there are formed six MISFETs for providing the basic design (i.e. the master). Specifically, there are formed a P-type well 7 which is formed in an N-type silicon semiconductor substrate 1', a field $SiO_2$ film 8, polysilicon layers 71 to 78, and $N^+$-type semiconductor regions 81 to 84 and $P^+$-type semiconductor regions 91 to 94 which are formed therein in a self-aligned manner by the ion-implantation or diffusion technique using the field $SiO_2$ film 8 and the polysilicon layer 71 to 76 for gate electrodes as masks thereby to provide source or drain regions. There are further formed an N-type region 95 and a P-type region 85 for biasing the N-type substrate 1' and the P-type well 7. Subsequently, the Al-I is formed on the first interlayer insulating film (although not shown) which is formed all over the surface to cover the pattern of the above referred to basic design (i.e. the master). As a result, there are formed input wirings A, B and C, and an output wiring X for constructing the logical circuit in the unit cell 2, e.g. three-input NAND gates.

Moreover, both the power source wiring $V_{DD}$ for supplying the power source ($V_{DD}$) to the unit cell 2 and an earthed connection GND are formed of the Al-I. Although not shown, the wirings A, B, C and X are connected through the Al-II with the logical gates, which are constructed by other unit cells, respectively. Incidentally, these interconnections can also be made by the Al-I if they can be effected only on the wiring channels 4.

The I/$\bar{O}$ cells 5 are so basically designed that a circuit most requiring the number of elements for each of the input and output circuits can be constructed by one I/$\bar{O}$ cell. In the present example, in order to provide interchangeability with an LSTTL (i.e. Low Power Schottky TTL), the elements constructing a converter for mutually converting the logical level of the CMOS and the level of the LSTTL are built in that I/$\bar{O}$ cell. In the drawings to follow, however, a portion of the I/$\bar{O}$ cell is shown, but the aforementioned level converting circuit portion is omitted.

An example, in which input and output circuits are constructed of the single I/$\bar{O}$ cell independently of each other, will be described with reference to Figures 3A to 5B. In the known construction it is not possible to construct and use independent input and output circuits in this way by means of the single I/$\bar{O}$ cell.

The method of forming the I/$\bar{O}$ cell is illustrated in accordance with the steps in Figures 3A to 3C, of which Figure 3A illustrates the layout at the step of the basic design (i.e. the master). Specifically, there are formed a P-type well 10, the field $SiO_2$ film 8, a polysilicon layer 11 acting as a gate electrode, a polysilicon layer 12 acting as an input protection resistor, and an $N^+$-type semiconductor region 17 and a $P^+$-type semiconductor region 18 which are formed in a self-aligned manner by the ion-implantation or diffusion technique using the polysilicon layer 11 and the field $SiO_2$ film 8 as masks thereby to provide a source or drain region.

The important construction in this embodiment is that the bonding pads formed adjacent to the I/$\bar{O}$ cell 5 are provided in a number corresponding to or more than the number of the functions to be performed by that I/$\bar{O}$ cell, e.g. two.

The major portion of the construction including those bonding pads will be described in the following with reference to Figures 3B, 3C, and 4.

After the cell construction conforming to the basic design has been formed, as illustrated in Figure 3A, respective aluminium wirings 19 are then applied by the Al-I, as illustrated in Figure 3B, so an input protection circuit composed of the

polysilicon resistor 12 and a diode 14, an input circuit composed of a CMOS inverter circuit 15, and a three-state output circuit 16 may have independent functions. The regions hatched in the drawing indicate those aluminium wirings 19, the interconnection with the underlying diffusion region region or polysilicon layer is effected at either the wider wiring portion or such a place of the portion indicated at "X" as is made wide of the "dog bone" type. Simultaneously with the wiring step of that Al-I, there are respectively formed bonding pads 6a-1 and 6b-1 of the Al-I for extracting the input and output from the I/$\bar{O}$ cell 5 independently of each other. Thos pads 6a-1 and 6b-1 have their wirings so designed that they are connected with the input protection resistor 12 and the output circuit 16, respectively, by means of the aluminium wirings 19.

After the coverage of the second interlayer insulating film, an Al-II is then formed, as illustrated in Figure 3C. This Al-II forms the aluminium wiring interconnecting the unit cell 2 and the I/$\bar{O}$ cell 5 described in the above, the power source wiring $V_{DD}$ for supplying the power source ($V_{DD}$) to the I/$\bar{O}$ cell 5, and the earthed connection GND, and further aluminium pads 6a-2 and 2b-2 just above and in the same shape as the aforementioned pads 6a-1 and 6b-1.

The portions indicated at "X" in the drawing designate the portions in which the Al-II is interconnected with the Al-I through holes formed on the Al-I contacting with the diffusion region in Figure 3B. In this case, the contacting portions between the Al-I and the diffusion region or the polysilicon layer are not illustrated.

Thus, there are formed adjacent to the I/$\bar{O}$ cell 5 and in an isolated manner from each other the input bonding pad 6a, which is composed of the aluminium pad 6a-1 of the Al-I and the aluminium pad 6a-2 of the Al-II, and the output bonding pad 6b which is composed of the aluminium pad 6b-1 of the Al-I and the aluminium pad 6b-2 of the Al-II.

This state is clearly illustrated in Figure 4. Figure 4 is a sectional view showing a portion including the output pad 6b, the input pad 6a, the wiring 19, the input protection resistor 12, the wiring 19 and the gate protecting circuit 14. The I/$\bar{O}$ cell includes an N-type silicon substrate 20; a field $SiO_2$ film 21; an $SiO_2$ film 22 on the surface of the polysilicon layer; a first PSG film 23; a second PSG film 24; and a third PSG film 25. Incidentally, the I/$\bar{O}$ cell shown in Figure 4 can be manufactured by the well known technique such as the thermal oxidization, ion-implantation, photoetching,

chemical vapour growth and vacuum evaporation.

The equivalent circuit of the I/$\bar{O}$ cell shown in Figure 3C is shown in Figures 5A and 5B, of which Figure 5A is an equivalent circuit diagram whereas Figure 5B is a circuit diagram shown by means of circuit symbols.

As shown in Figure 5A, the input circuit consists of the input protection circuit which comprises the input protection resistor 12 and the diode 14, and the two-stage CMOS inverter 15. Moreover, the signal fed from the pad 6a is further fed therethrough to IN and is connected through the above referred to LSTTL-CMOS level converter with the logical circuit composed of the unit cell 2. . On the other hand, the output circuit is composed of the CMOS inverter, the NAND gate, the NOR gate and three-state output buffer composed of six MOSs. Moreover, two signals EN and OUT, which are fed from the logical circuit composed of the unit cell 2, are fed through the CMOS-LSTTL level converter to the CMOS inverter and NOR gate, respectively. The signal, which is prepared by those two signals EN and OUT, drives the three-state output buffer, the output of which is fed from the pad 6b. Figure 5B is a block diagram showing the circuit by means of symbols.

Figures 6A, 6B and 8B illustrate the

manufacture of I/$\bar{O}$ cell by a method similar to that of Figure 5B.

In the case of the construction shown in Figures 3C and 4, the input circuit and output circuit of the I/$\bar{O}$ cell 5 can be separately connected with external leads by compression-bonding bonding wires 26 and 27 from the external leads to the respective bonding pads 6a and 6b. In other words, both the input and output functions belonging to the I/$\bar{O}$ cell can be simultaneously selected. This is because the two bonding pads 6a and 6b are provided for the single I/$\bar{O}$ cell and are used separately of each other. This cannot be achieved in a known system which has one I/$\bar{O}$ cell and one pad.

Figures 6A, 6B and 6C show second, third and fourth embodiments respectively. These second, third and fourth embodiments are those, in which at least one of the couples 5b of the I/$\bar{O}$ cells 5 indicated at single-dotted lines in the general layout of the chip shown in Figure 1 and the two corresponding pads 6a and 6b are replaced by the couples of the I/$\bar{O}$ cells and the pads shown in Figures 6A, 6B and 6C, respectively. The basic design (i.e. the master) of the I/$\bar{O}$ cells and the unit cells of those embodiments is similar to that of the first embodiment, and its explanation is omitted here. Moreover, it goes

without saying that the second to fourth embodiments are prepared by the steps similar to those having been described in connection with the first embodiment.

In the second embodiment as shown in Figure 6A, only the input circuit portion is extracted from the I/$\bar{O}$ cell 5. In the third embodiment as shown in Figure 6B, only the output circuit portion is extracted. In the fourth embodiment as shown in Figure 6C, both the input and output circuit portions are extracted as the bidirectional input and output. The circuit portions left unextracted are indicated at broken lines. The Al-I providing the wirings corresponding to the portions indicated at the broken lines is not naturally formed.

The difference shared among those embodiments and from the first embodiment resides in that the bonding pad for the single I/$\bar{O}$ is made as if the two pads having been described in the first embodiment were short-circuited.

By the broken lines appearting in the bonding pads 6 of Figures 6A to 6C, specifically, the pads 6 are so shaped that regions 6a' and 6b' corresponding to the pads which are imaginarily divided into two. The positions and sizes of both of those regions 6a' and 6b' thus divided are respectively identical to those of the pads 6a and 6b of the first embodiment.

The construction of those pads 6 is shown in

Figure 7. Figure 7 illustrates the sectional construction of the embodiment of Figure 6A and is a sectional view showing the portion corresponding to Figure 4. The pad 6 has such a laminated construction as is composed of the Al-I and the Al-II. Moreover, the Al-I is so designed that it is connected during its forming step with the input of the I/$\bar{O}$ cell 5. As a result, the pad 6 thus obtained is connected with the input circuit of the I/$\bar{O}$ cell 5. As is apparent from the comparison with Figure 4, the pad 6 is formed all over the regions 6a' and 6b' which in turn are to be formed with the pads 6a and 6b. Moreover, the bonding wire 26 is compress-bonded to the pad 6 to connect the input circuit of the I/$\bar{O}$ cell and the external leads. An explanation of the sectional constructions of the embodiments of Figures 6B and 6C is omitted because it can be easily judged from Figure 7. If the pad 6 is made wider, as in those embodiments, the bonding process can be greatly facilitated and its reliability improved.

In the embodiments of Figures 6A and 6B, incidentally, it is naturally possible to form only one pad 6a or 6b at the positions of the two regions 6a' and 6b' corresponding to the pads and to inter-connect that pad 6a or 6b and the input or output circuit.

The embodiments thus far described can be

obtained as a free modification of the first embodiment in the case where there arises a condition under which the two pads need not be arranged for each I/$\bar{O}$ cell in accordance with the numbers of the pins and the bonding wires and with the circuit aimed at. Moreover, the kind of the IC obtainable by the same basic design (i.e. the master) is widened more than the prior art.

In the case of this embodiment, the ratio between the portion formed with two pads for one I/$\bar{O}$ cell and the portion formed with one pad can be changed in accordance with several conditions including the number of the pins. In this case, incidentally, if two pads are provided for the I/$\bar{O}$ cell at the centre portion of the chip whereas one pad is provided for the I/$\bar{O}$ cell at the end portion while considering the bonding condition, i.e. that the bonding wire is held perpendicularly to the chip side at the centre portion but is held the more obliquely with respect to the chip side, as it approaches towards the end portion of the side, so that the bonding process becomes the more difficult, the workability and reliability of the bonding process can be improved.

As a modification of the foregoing second to fourth embodiments, for example, even if the Al-I layer is provided separately as the pads 6a and 6b of the first embodiment so that those pads 6a and 6b

are short-circuited to provide the pad 6 by means of the second Al-II layer, it is possible to extract only the input, the output or the bidirectional input and output. In this modification, the pattern of the underlying Al-I need not be changed in the least so that the mask for forming the underlying pad can be produced more easily. The short-circuiting structure thus prepared may be provided at the cell of a portion of the whole I/$\bar{O}$ cell, but its number may be suitably changed in accordance with the several conditions such as the pin number.

Moreover, all the respective pads need not be formed into an identical rectangular shape but may be arranged more generally in the shape of a parallelogram in conformity to the compression-bonding direction of the bonding wire, for example, as they approach the closer to both the ends of the pad rows.

Moreover, in the first embodiment, the number of the pads to be arranged for each I/$\bar{O}$ cell may be equal to or less than the number of the output functions performed by that I/$\bar{O}$ cell, e.g. two or more. In an alternative, more pads, e.g. three pads more than the number of the input and output functions can be provided. In this case, it can be expected that the degree of freedom in selecting the pads is further augmented in accordance with the number of

the input and output functions.

Incidentally, it will be understood that the present invention can be applied to other types of locigal IC as well as the CMOS type logical IC illustrated in the above embodiments.

As will be apparent from the above description, the semiconductor integrated circuit device has the following prominent advantages, as summarized in the following:

(a) Especially in the IC design resorting to the master slice approach, the bonding pads can be arbitrarily selected in accordance with the number (i.e. the number of the functions performed by the $I/\bar{O}$ cell) of the input and output signals to be extracted without any change in the basic design (i.e. the master) so that the degree of freedom in the IC design can be augmented. Since the bonding pads can be so constructed as to satisfy all the respective functions of the $I/\bar{O}$ cell, the bonding pads can also be arbitrarily selected in accordance with the master slice approach.

(b) As a result, the restriction to the number of the signals to be extracted can be substantially reduced without any change in the basic design that the number of the pins can be greatly increased (e.g. twice as many as the pins) than in the known

constructions.

(c) Since the two independent functions as the input and output circuits can be imparted to the I/$\bar{O}$ cell, the efficiency of the I/$\bar{O}$ cell can be substantially increased.

CLAIMS.

1. An integrated circuit device including:

(a) a semiconductor body;

(b) a plurality of unit cells formed on the semiconductor body, each of which includes predetermined circuit elements for providing at least one of two different functions of a first circuit and a second circuit,

the plurality of unit cells including a first set of unit cells of the first circuits, a second set of unit cells of the second circuits and a third set of unit cells, each of which independently has the two functions of the first and second circuits, the third set of unit cells including at least one member; and

(c) a wiring pattern for providing each of the unit cells with a respective predetermined circuit function.

2. An integrated circuit device according to claim 1, wherein the first circuit is an input circuit and the second circuit is an output circuit.

3. An integrated circuit device according to claim 1 or claim 2, wherein each of the third set of unit cells has two bonding pads.

4. An integrated circuit device according to claim 3, wherein each one of the two bonding pads is electrically connected to respective input circuits, and the other of the two bonding pads is electrically connected to respective output circuits.

5. An integrated circuit device according to claim 3 or claim 4, wherein each of the bonding pads is composed of a lower conductor film and upper conductor film overlaid on and in contact with the former.

6. An integrated circuit device according to any one of the preceding claims, wherein each of the plurality of unit cells has a circuit element capable of forming a bidirectional input/output circuit.

7. A method of manufacturing an integrated circuit device, including the steps of:

(a) forming a plurality of units cells, each of which includes a plurality of circuit elements;

(b) connecting at least some of the circuit elements of each of the unit cells in a pattern so as to provide a respective predetermined circuit function; and

(c) forming a bonding pad for each of some of the connected unit cells and two bonding pads for each of the other of the connected unit cells.

8. A method of manufacturing an integrated circuit device according to claim 7, wherein the predetermined circuit function includes an input circuit and an output circuit.

9. A method of manufacturing an integrated circuit device according to claim 7 or claim 8, wherein each of the plurality of unit cells has the circuit element capable of forming a bidirectional input/output circuit.

10. An integrated circuit device constructed substantially as herein described with reference to and as illustrated in the accompanying drawings.

11. A method of manufacturing an integrated circuit device substantially as herein described with reference to the accompanying drawings.