

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
7 February 2002 (07.02.2002)

PCT

(10) International Publication Number
WO 02/11207 A2

(51) International Patent Classification⁷: **H01L 23/498,**
H05K 1/16

Kishore [US/US]; 6407 Berkwickshire Way, San Jose, CA
95120 (US).

(21) International Application Number: **PCT/US01/23721**

(74) **Agent: VIKSNINS, Ann, S.;** Schwegman, Lundberg,
Woessner & Kluth, P.A., P.O. Box 2938, Minneapolis, MN
55402 (US).

(22) International Filing Date: **26 July 2001 (26.07.2001)**

(25) Filing Language: **English**

(81) **Designated States (national):** AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK,
SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA,
ZW.

(26) Publication Language: **English**

(30) **Priority Data:**
09/631,037 **31 July 2000 (31.07.2000)** **US**

(71) **Applicant (for all designated States except US): INTEL**
CORPORATION [US/US]; 2200 Mission College Boule-
vard, Santa Clara, CA 95052 (US).

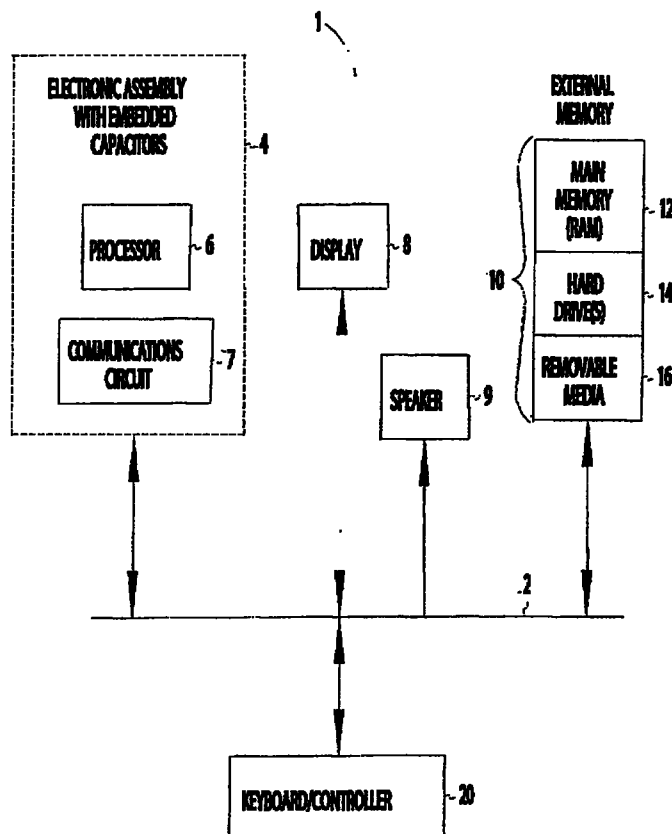
(84) **Designated States (regional):** ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian
patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European
patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE,

(72) **Inventor; and**

(75) **Inventor/Applicant (for US only): CHAKRAVORTY,**

[Continued on next page]

(54) **Title: ELECTRONIC ASSEMBLY COMPRISING SUBSTRATE WITH EMBEDDED CAPACITORS AND METHODS OF MANUFACTURE**



(57) **Abstract:** To reduce switching noise, the power supply terminals of an integrated circuit die can be coupled to the respective terminals of at least one embedded capacitor in a multilayer ceramic substrate. In one embodiment, the capacitor is formed of at least one high permittivity layer. In another embodiment, several high permittivity layers are interleaved with conductive layers. Alternatively, the capacitor can comprise at least one embedded discrete capacitor. Also described are an electronic system, a data processing system, and various methods of manufacture.

WO 02/11207 A2



IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

— *without international search report and to be republished upon receipt of that report*