CLAIMS

1. An apparatus, comprising:

a thyristor coupled to a node and configured to discharge current associated with an over-voltage event at the node, wherein the over-voltage event includes a negative voltage having a magnitude that exceeds a trigger voltage of the thyristor;

a first transistor coupled to the thyristor and configured to adjust the magnitude of the trigger voltage; and

a second transistor coupled to the first transistor, wherein the second transistor is a lateral BJT merged with the first transistor and wherein the first transistor and the second transistor share at least two conductive regions.

2. The apparatus of claim 1, wherein the first transistor is a p-type field effect transistor.

3. The apparatus of claim 2, where in the thyristor comprises a first bi-polar junction transistor (BJT) coupled to a second BJT, wherein the first BJT is coupled to the node and the second BJT is coupled to a reference node.

4. The apparatus of claim 3, wherein a drain of the transistor is coupled to a base of the first BJT that is shared with a collector of the second BJT, and wherein a source of the transistor is coupled to the reference node.

5. The apparatus of claim 1, wherein the first transistor is configured to adjust the magnitude of the trigger voltage to a first voltage while in first state and to a second voltage while in a second state.

6. The apparatus of claim 5, wherein the first state is associated with an operational mode, and wherein the second state is associated with an electrostatic discharge mode.

7. The apparatus of claim 5, wherein the first voltage is greater than the second voltage.

8. The apparatus of claim 1, further comprising a protected circuit coupled to the node in parallel with the thyristor.

9. The apparatus of claim 1, wherein the over-voltage event is an electrostatic discharge (ESD) event.

10. An apparatus, comprising:

a first well doped with a first dopant type;

a first region and a second region within the first well, and the first and second regions doped with a second dopant type;

a second well doped with the second dopant type, the second well within the first well;

a third region within the second well doped with the first dopant type;

a gate;

wherein the first region, the gate, the first well, and the second region together form a transistor, and wherein the first region, the first well, and the second region together form a lateral bi-polar junction transistor, and

wherein the third region, the second well, the first well, and the second region together form a thyristor.

11. The apparatus of claim 10, wherein the third region, the second well, and the first well together form a first bi-polar junction transistor (BJT) of the thyristor, and wherein the second well, the first well, and the second region together form a second BJT of the thyristor.

12. The apparatus of claim 10, wherein the third region is coupled to a node, and wherein the second well is coupled to the first region.

13. The apparatus of claim 12, wherein the first dopant type is an n-type dopant and the second dopant type is a p-type dopant, and wherein the thyristor is configured to discharge a current from the node responsive the node having a negative voltage that is more negative than a trigger voltage.

14. The apparatus of claim 10, wherein the trigger voltage is adjusted based on a state of the transistor, wherein the transistor is in a first state while a voltage of the gate of the transistor has a first value and is in a second state while the voltage of the gate of the transistor has a second value.

15. An apparatus, comprising:

a circuit coupled to a negative input node;

a protection circuit coupled to the negative input node in parallel with the input circuit, the protection circuit including a thyristor, a bipolar junction transistor, and a transistor, the thyristor configured to discharge a current associated with an over-voltage event at the negative input node, wherein the over-voltage event includes a negative voltage at the negative input node that is more negative than a trigger voltage of the thyristor, wherein the transistor is coupled to the thyristor and is

configured to adjust the trigger voltage, and wherein the bipolar junction transistor is coupled in parallel with the transistor.

16. The apparatus of claim 15, wherein the transistor is configured to adjust the trigger voltage based on a voltage at a gate of the transistor.

17. The apparatus of claim 15, wherein, while in a first mode, the transistor is configured to adjust the trigger voltage to a first voltage, and wherein, while in a second mode, the transistor is configured to adjust the trigger voltage to a second voltage.

18. The apparatus of claim 15, wherein the first voltage is more negative than the second voltage.

19. The apparatus of claim 15, wherein the transistor is a p-type field effect transistor, wherein the thyristor is a silicon controlled rectifier sharing a drain of the transistor.

20. A method, comprising:

triggering a thyristor to discharge current from a negative input node to a reference node responsive to a voltage differential between the reference node and the negative input node exceeding a trigger voltage of the thyristor wherein the thyristor is triggered with a transistor coupled to the thyristor and a bipolar junction transistor (BJT) coupled in parallel with the transistor; and

discharging current to the reference node through the triggered thyristor responsive to triggering the thyristor.

21. The method of claim 20, wherein the transistor comprises a p-type transistor, and claim 20 further comprising:

while in an operational mode, adjusting a trigger voltage to a first value using the p-type transistor coupled to the thyristor; and

while in an electrostatic discharge (ESD) mode, adjusting a trigger voltage to a second value using the transistor coupled to the thyristor.

22. The method of claim 21, wherein the thyristor includes a first bi-polar junction transistor and a second BJT, wherein the transistor is coupled to a base of the first BJT and to a collector of the second BJT.

23. The method of claim 21, wherein the first value is more negative than the second value.

24. The method of claim 21, wherein a voltage at a gate of the transistor is a first gate voltage while in the operation mode and the voltage at the gate of the transistor is a second gate voltage while in the ESD mode.

25. The method of claim 21, wherein the BJT is merged with the transistor in an n-well in which the transistor and the BJT are formed.