

Semiconductor Wafer Having A Multilayered Structure And Method For Producing The Same

Technical Field

5 The present invention is directed to a semiconductor wafer having a multilayered structure and a method for producing the same.

Discussion of Closest Prior Art

10 In modern electronics, gallium nitride (GaN) power devices have attracted increased attention due to their superior high-voltage and high-current capacity. In particular, vertical GaN power devices are promising candidates for next generation high-voltage and high-current power switching applications in electric vehicles, smart grids and renewable energy processes.

15 For such device, a relatively thin layer of a heteroepitaxial GaN film is deposited on a silicon wafer, with a buffer layer in between. The deposition of a buffer layer is necessary because of the lattice mismatch and the mismatch between the coefficients of thermal expansion of Si and GaN.

20 Even in the presence of one or more buffer layers, the lattice mismatch results in a relatively high defect density in the GaN layer. Moreover, the different coefficients of thermal expansion can lead to cracks if the GaN layer exceeds a certain thickness. To account for the different coefficient of thermal expansion, sufficient compressive stress must be incorporated into a GaN layer during growth to counteract the tensile stress to which it is subjected during the cooling process. The relatively high defect density and the limited thickness of the GaN layer limits the performance of the power device, for example in terms of its breakdown voltage.

25 There is thus a need for improved GaN structures with new buffer layers that enable the fabrication of GaN drift layers with low defect density and a high thickness of more than 5 μm .

EP 2 727 133 B1 discloses a GaN structure with a buffer layer comprising two translation layers of the composition $B_wAl_xGa_yIn_zN$. Thus, a GaN layer having a thickness of more than 5 μm and a relatively low dislocation density can be obtained.

Yet, the buffer layer is relatively thick and complex and the thickness of the GaN drift layer is limited.

Y. Zhang *et al.* *J. Phys. D: Appl. Phys.* **51** (2018) 273001 describe a buffer layer which enables the preparation of a GaN layer having a dislocation density of $2 \times 10^8 \text{ cm}^{-2}$ and a thickness of less than 6 μm .

A. Dadgar *et al.* *Phys. Stat. Sol. (C)* **0**, No. 6 (2003) describe the reduction of dislocations by a superlattice structure having 15 periods. It is explained that dislocations are bent at the interfaces of the layers of the superlattice, thereby increasing the probability of recombination and annihilation with other dislocations with opposite burgers vector. The mechanism of annihilation of dislocations in such multilayered structures is also discussed by A. E. Romanov and J. S. Speck. *Appl. Phys. Lett.* 83.13 (2003): 2569-2571; by B. Daudin, B. *et al.* *Phys. Rev. B* 56.12 (1997): R7069; and by M. Imura *et al.* *J. Cryst. Growth* 300.1 (2007): 136-140.

Objective and Solution Provided by the Invention

The present invention aims at providing a new GaN structure having a GaN drift layer with an increased thickness, reduced dislocation density and reduced stress in the GaN drift layer.

The above problem is solved by the semiconductor wafer having a multilayered structure according to the first aspect of the present invention.

In a second aspect, the present invention is directed to a method of producing a semiconductor wafer having a multilayered structure. This method is suitable for manufacturing the semiconductor wafer having a multilayered structure according to the first aspect of the present invention.

In particular, the inventors have found that specific process conditions can induce the growth of islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$, with $0.7 \leq x \leq 1.0$ and $0 \leq y \leq 0.5$, followed by a superlattice comprised of layers of these materials. It has been surprisingly found that the presence of islands reduces the dislocations in a

5 comparatively small section of the buffer layer. These islands annihilate dislocations and reduce compressive stress relaxation during GaN growth. Thus, sufficiently high compressive stress is maintained, so that the tensile stress during cooling can be compensated. As a result, GaN drift layers with high thickness and low dislocation density can be obtained in a process that is susceptible for industrial application. In

10 addition, as dislocations, in particular threading dislocations, can be efficiently reduced in a comparatively small section of the buffer layer, the thickness of the buffer layer as a whole can be reduced. This is advantageous as this allows to reduce production costs and enhances heat transport through the buffer layer during operation of the device.

15 The increased compressive stress buildup compensates for the thermal mismatch and enables the growth of thick GaN layers, resulting in crack-free wafers with low residual stress and wafer bow. This outcome is key to achieving thick GaN layers on silicon substrates.

The semiconductor wafer having a multilayered structure according to the first aspect

20 of the present invention has a diameter of not less than 150 mm and not more than 300 mm. The multilayered structure of the wafer comprises in this order

a monocrystalline silicon substrate having a {111} orientation;
at least one AlN nucleation layer;
an $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer;

25 islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$;
a superlattice structure comprising 20 to 120 periods, each period consisting of a layer of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and a layer of $\text{Al}_y\text{Ga}_{1-y}\text{N}$; and
one or more monocrystalline, doped GaN layers having a total thickness of not less than 6 μm ,

wherein at least one of the one or more monocrystalline, doped GaN layers has a threading dislocation density of not more than $5.0 \times 10^8 \text{ cm}^{-2}$, and

wherein $0.3 \leq z \leq 0.7$; $0.7 \leq x \leq 1.0$; and $0 \leq y \leq 0.5$.

In a second aspect of the present invention, a method of producing a semiconductor wafer having a multilayered structure is provided. The method comprises the following steps in this order:

- (i) providing a monocrystalline silicon substrate having a {111} orientation;
- (ii) flowing a gas stream which comprises an aluminum precursor and no nitrogen precursor over the substrate at a temperature of not less than 700 °C and not more than 900 °C so that the total amount of aluminum flown over the substrate is not less than 0.1 μmol and not more than 250 μmol ,
- (iii) depositing a low temperature AlN nucleation layer by flowing a gas stream comprising an aluminum precursor and a nitrogen precursor over the substrate at a temperature of not less than 700 °C and not more than 900 °C,
- (iv) depositing a high temperature AlN nucleation layer by flowing a gas stream comprising an aluminum precursor and a nitrogen precursor over the substrate at a temperature of not less than 950 °C and not more than 1100 °C,
- (v) depositing an $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer with $0.3 \leq z \leq 0.7$ by flowing a gas stream comprising an aluminum precursor, a gallium precursor and a nitrogen precursor over the substrate at a temperature of not less than 950 °C and not more than 1050 °C,
- (vi) depositing alternately $\text{Al}_x\text{Ga}_{1-x}\text{N}$ with $0.7 \leq x \leq 1.0$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$ with $0 \leq y \leq 0.5$ for 20 to 120 cycles by flowing a gas stream comprising an aluminum precursor, a gallium precursor and a nitrogen precursor over the substrate at a temperature of not less than 950°C and not more than 1100°C, wherein the alternation of the deposition is achieved by changing the composition of the gas stream; and
- (vii) depositing one or more monocrystalline, doped GaN layers by flowing a gas stream comprising a gallium precursor, a nitrogen precursor and a dopant precursor over the substrate at a temperature of not less than 900 and not more than 1200°C.

The method according to the second aspect of the present invention does not need ELOG techniques or in-situ masking with silicon nitride and is therefore more economical in terms of process time and costs. The method is therefore more susceptible to industrial application. Furthermore, the method according to the second aspect of the present invention allows to obtain specific shapes and dimensions of the islands formed in step (vi).

The growth of islands and a superlattice structure is an effective way to bend and annihilate dislocations, leading to a drastic reduction in dislocation density in a small section of the buffer, as can be seen in Fig. 8. Thus, it is possible to avoid the use of time-consuming conventional methods such as ELOG and thick buffer structures to achieve similar dislocation densities. The method of the present invention allows the preparation of a superlattice structure, in which sufficient compressive stress is preserved in the crystal lattice. As a result, the positive amount of warp per unit thickness during the GaN growth on top of the superlattice structure is sufficiently high to compensate for the tensile stress generated upon cooling down. A positive warp within the meaning of the present invention indicates that the semiconductor wafer has a convex shape. A negative warp within the meaning of the present invention indicates that the semiconductor wafer has a concave shape.

Also, the lower dislocation densities result in a higher critical breakdown field, such that a lower GaN thickness is required to achieve the same breakdown voltage. This enables sufficiently thick GaN device layers to be grown to produce PIN diodes and transistors for medium-voltage applications (600-1700 V) with either a fully vertical or quasi-vertical configuration.

Brief Description of Figures

Fig. 1 shows a plan-view image of a semiconductor wafer recorded on a scanning electron microscope (SEM) after 5 cycles of depositing alternately $\text{Al}_x\text{Ga}_{1-x}\text{N}$ with $0.7 \leq x \leq 1.0$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$ with $0 \leq y \leq 0.5$ according to steps (i) to (vi) of the method of the present invention.

Fig. 2a shows the reverse current–voltage curves (I-V curves) at different temperatures of a PIN diode with drift layer having a thickness of 3 μm and produced according to the method of the present invention.

5 **Fig. 2b** shows the temperature-dependent breakdown voltage of a PIN diode with a drift layer having a thickness of 3 μm . The PIN diode was formed from a semiconductor wafer produced according to the method of the present invention and is the same PIN diode as studied in Fig. 2a.

Fig. 3 shows the reverse I-V curves of two PIN diodes having a drift layer with a thickness of 3.5 μm and 4.5 μm , respectively. The reverse I-V curves were measured
10 at room temperature. Both samples were prepared from a semiconductor wafer prepared according to the method of to the present invention.

Fig 4a is a schematic drawing of the multilayered structure of a PIN-stack of a semiconductor wafer according to the present invention.
15

Fig. 4b shows a cross-sectional image of a similar PIN-stack as shown in Fig. 4a recorded on a scanning electron microscope.

Fig. 5 shows an image of the surface of a semiconductor wafer according to the
20 present invention in plan-view recorded on an optical microscope.

Fig. 6 is a cross-sectional TEM image of a semiconductor wafer according to the present invention and prepared according to the method of the present invention, showing that dislocations are bent and annihilated by the islands.
25

Fig. 7 shows an SEM image of a buffer layer of a multilayered structure of a semiconductor wafer according to the first aspect of the present invention in cross section, showing a maximum thickness (h) of an island and a value (h/2) corresponding to half of the maximum thickness. h/2 corresponds to the thickness at
30 which an island density of $6 \times 10^7 \text{ cm}^{-2}$ was determined.

Fig. 8 shows a TEM image of the cross section of a buffer layer of a multilayered structure of a semiconductor wafer according to the first aspect of the present invention. The circles highlight the positions where threading dislocations fuse and form a new dislocation or annihilate.

5

Fig. 9 shows the reverse J-V characteristics of the PIN structure of Example 6.

Detailed Description of the Invention

- 10 In the following, the semiconductor wafer having a multilayered structure according to the first aspect of the present invention is disclosed. The multilayered structure of the wafer comprises in this order
- a monocrystalline silicon substrate having a {111} orientation;
 - at least one AlN nucleation layer;
 - 15 an $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer;
 - islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$;
 - a superlattice structure comprising 20 to 120 periods, each period consisting of a layer of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and a layer of $\text{Al}_y\text{Ga}_{1-y}\text{N}$; and
 - one or more monocrystalline, doped GaN layers having a total thickness of not
 - 20 less than 6 μm ,
 - wherein at least one of the one or more monocrystalline, doped GaN layers has a threading dislocation density of not more than $5.0 \times 10^8 \text{ cm}^{-2}$, and
 - wherein $0.3 \leq z \leq 0.7$; $0.7 \leq x \leq 1.0$; and $0 \leq y \leq 0.5$.
- 25 The monocrystalline silicon substrate has a {111} orientation. The substrate is preferably a monocrystalline silicon wafer having a diameter of not less than 150 mm and not more than 300 mm, preferably not less than 150 mm and not more than 210 mm. In a particularly preferred embodiment, the monocrystalline silicon substrate has a diameter of 150 mm or 200 mm. The monocrystalline silicon substrate has
- 30 preferably a thickness of not less than 625 μm and not more than 1500 μm . The monocrystalline silicon substrate is optionally doped and may have a silicon oxide or silicon nitride protection layer on its backside.

The substrate preferably consists of boron-doped monocrystalline silicon. The at least one AlN nucleation layer preferably comprises a low temperature AlN nucleation layer and a high temperature AlN nucleation layer. The total thickness of the at least one AlN nucleation layer is preferably not less than 50 nm and not more than 500 nm.

- 5 Preferably, the high temperature AlN nucleation layer is located on top of the low temperature AlN nucleation layer.

A low temperature AlN nucleation layer within the meaning of the present invention is a layer of the composition AlN deposited by metalorganic chemical vapour deposition (MOCVD) at a temperature of not more than 900°C. The low temperature AlN
10 nucleation layer is formed on top of the monocrystalline silicon substrate. It has preferably a thickness of not less than 1 nm and not more than 50 nm. The purpose of the low temperature AlN nucleation layer is to provide a high density of nucleation sites on the silicon substrate to promote the growth of a continuous high temperature AlN layer, avoiding large pits. The low temperature AlN nucleation layer is formed by
15 flowing a gas stream comprising an aluminum precursor and a nitrogen precursor over the substrate at a temperature of not less than 700 °C and not more than 900 °C.

A high temperature AlN nucleation layer within the meaning of the present invention is a layer of the composition AlN deposited by metalorganic chemical vapour deposition (MOCVD) at a temperature of not less than 950°C. The high temperature AlN
20 nucleation layer is formed on top of the low temperature AlN layer. It has preferably a thickness of not less than 50 nm and not more than 500 nm, more preferably of not less than 100 nm and not more than 300 nm. The high temperature AlN layer is deposited to protect the silicon substrate from meltback-etching that occurs when Ga is in contact with silicon at elevated temperatures. In the initial growth phase, islands
25 form and coalesce. As a result of the high lattice mismatch between AlN and silicon and the subsequent island coalescence, the high temperature AlN nucleation layer has a high density of threading dislocations. The AlN layer grows under tensile stress, which leads to a concave warp of the wafer with increasing AlN thickness. The high temperature AlN nucleation layer is deposited at high temperature by flowing a gas
30 stream comprising an aluminum precursor and a nitrogen precursor over the substrate

with the low temperature AlN layer on top of it at a temperature of not less than 950 °C and not more than 1100 °C.

The $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer is formed on top of the at least one AlN nucleation layer, preferably on top of the high temperature AlN nucleation layer, and has an Al content defined by $0.3 \leq z \leq 0.7$. More preferably, the $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer has a composition defined by $0.4 \leq z \leq 0.6$, most preferably $0.45 \leq z \leq 0.55$. The $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer has preferably a thickness of not less than 10 nm and not more than 400 nm, more preferably not less than 20 nm and not more than 200 nm, and most preferably not more than 100 nm. The effect of the $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer is to smoothen the surface after AlN growth and to annihilate dislocations. Preferably, the $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer is under compressive stress. If the $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer is under compressive stress, a change of the curvature of the wafer is initiated, so that the multilayered structure is less concave as compared to its curvature after deposition of the AlN layers and before the $\text{Al}_z\text{Ga}_{1-z}\text{N}$ deposition. The $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer is deposited by flowing a gas stream comprising an aluminum precursor, a gallium precursor and a nitrogen precursor, and optionally a carrier gas such as hydrogen or nitrogen, over the substrate with the low and the high temperature AlN layers at a temperature of not less than 950 °C and not more than 1050 °C.

On top of the $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer, islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$, with $0.7 \leq x \leq 1.0$ and $0 \leq y \leq 0.5$, preferably $0.80 \leq x \leq 1.00$ and $0.05 \leq y \leq 0.4$, most preferred $0.90 \leq x \leq 1.00$ and $0.10 \leq y \leq 0.20$, are formed.

An island of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ comprises at least one layer of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and an island of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ comprises at least one layer of $\text{Al}_y\text{Ga}_{1-y}\text{N}$. Preferably, the islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ have a layered structure. More preferably, the islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and the islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ consist of alternating layers of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$. In a preferred embodiment, the islands consist of not less than 5 and not more than 20 layers.

The total density of islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ is preferably not less than $1.0 \times 10^7 \text{ cm}^{-2}$ and not more than $1.0 \times 10^{10} \text{ cm}^{-2}$, more preferably, not less than

5.0×10⁷ cm⁻² and not more than 5.0×10⁹ cm⁻². The total density of islands within the meaning of the present invention is determined from plan-view, *i.e.* when viewed from an axial direction. In other words, the island density refers to the density of islands in a plane parallel to the wafer surface and located between Al_zGa_{1-z}N layer and the GaN layers. The island density is preferably determined after not less than 5 cycles, more preferably after not less than 10 and not more than 20 cycles, of depositing alternately Al_xGa_{1-x}N with 0.7≤x≤1.0 and Al_yGa_{1-y}N with 0≤y≤0.5. In other words, it is preferable to determine the island density close to the time of coalescence, before the formation of continuous layers of the super lattice structure is induced.

10 The density of the islands decreases with increasing thickness of the superlattice, due to the coalescence of adjacent islands. Therefore, the island density is most preferably determined, when the thickness of the islands corresponds to half of their maximum thickness. In the present invention, the terms height and maximum thickness are used synonymously with respect to the islands. Fig. 7 shows a scanning electron microscopy (SEM) image of the buffer layer of a multilayered structure of a semiconductor wafer according to the first aspect of the present invention, showing a maximum thickness (h) of an island having and a value (h/2) corresponding to half of the maximum thickness. h/2 corresponds to the thickness at which the island density and island geometry is preferably determined. The density ρ of the islands can be determined by taking an SEM image in cross-section view, so that the SEM image shows a surface perpendicular to (111) orientation of the monocrystalline silicon substrate, counting the number of island n along a lateral line having the length L in the SEM image (as shown in Fig. 7), and determining the density ρ according to the following formula: $\rho = n/L^2$; where n is the number of islands counted along a lateral line with the length L .

The mechanism of island formation will be discussed in more detail below in the context of the method according to the second aspect of the present invention. Fig. 6 is a cross-sectional image of a semiconductor wafer according to the present invention and prepared according to the method of the present invention, showing that dislocations are bent and annihilated by the islands. The image was recorded on a transmission electron microscope.

If the island density is in the above range, the annihilation of dislocations is improved, resulting in a lower dislocation density in the subsequently deposited layers. More particularly, if the island density is lower than $1.0 \times 10^7 \text{ cm}^{-2}$, the distance between neighboring islands is too large for the islands to coalesce. Instead, the layer is closed
5 by vertical growth between the islands. As a result, the areas between the islands have a high dislocation density. In addition, if the island density is lower than $1.0 \times 10^7 \text{ cm}^{-2}$, the thickness at the time of coalescence of adjacent islands is large. Since the islands grow with a low stress, tensile stress induced during cooling is not compensated. If the island density is above $1.0 \times 10^{10} \text{ cm}^{-2}$, the annihilation of
10 dislocations is not effective, either.

Preferably, the islands have a height of not less than 100 nm and not more than 1000 nm. More preferably, the islands have a height (or maximum thickness) of not less than 160 nm and not more than 450 nm. The height or maximum thickness preferably corresponds to the thickness at the point of coalescence. The height is the
15 maximum length of an island in a direction perpendicular to the surface of the wafer, *i.e.* in a direction perpendicular to a plane of the monocrystalline silicon substrate having a {111} orientation. The height refers to the height of the islands at the time of coalescence. If the height of the islands falls within the range of 100 to 1000 nm, the annihilation of dislocations is promoted and thermally induced stress is compensated.
20 In the present invention, the height of the islands is also referred to as thickness of the islands. Preferably, the islands have an aspect ratio of not less than 0.1 and not more than 100, more preferably not less than 0.1 and not more than 10. The aspect ratio is the ratio of width to height of an island. The width is the maximum diameter of an island in a plane parallel to the wafer surface, *i.e.* the maximum width in a plane
25 parallel to the {111} orientation of the monocrystalline silicon substrate. Thus, the maximum width is determined in plan-view of the wafer. The height and diameter of the islands and the island density can be determined by means of scanning electron microscopy (SEM). The height and diameter of the islands and the island density can also be determined by means of transmission electron microscopy (TEM) or atomic
30 force microscope (AFM), wherein the latter requires growth interruption at different stages of the growth of the islands. SEM is a comparatively fast method for analyzing the geometry of the islands, *i.e.* the height and width of the islands. In addition, SEM

allows to analyze a larger area and the cross-section to be analyzed can be easily prepared by mechanically dicing the wafer. Therefore, the total density of islands, their aspect ratio and the height of the islands are preferably determined by means of scanning electron microscopy (SEM).

- 5 The aspect ratio within the meaning of the present invention is preferably a median aspect ratio, which is the median value of the aspect ratios of at least 100 islands. If the aspect ratio is above 100, the height of the islands at the time of coalescence is low. As a result, dislocations will reach the upper surface without interacting with dislocations bent at adjacent islands, resulting in a high dislocation density in the
- 10 doped or non-doped GaN layers of the semiconductor wafer. If the aspect ratio is below 0.1, the height of the islands is relatively high, so that the thermally induced stress is not compensated for during cooling.

- Preferably, the islands have tilted side facets. The tilted side facets cause bending of dislocations and, thus, the annihilation of dislocations is further promoted. More
- 15 particularly, the dislocations, in particular threading dislocations, are bent at the facets of the islands and concentrate at the island boundaries, thereby increasing the probability of annihilation of these dislocations.

- After 5 to 20 periods of depositing alternately $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$, coalescence takes place and, thus, the deposition of continuous layers is initiated on top of the
- 20 islands.

- When the deposition of continuous layers is initiated, a superlattice structure is formed. A superlattice is a periodic structure of layers of two or more materials, wherein the thickness of one period is in the nanometer range. In the present invention, the term superlattice structure refers to a periodic structure of two materials,
- 25 wherein each period has a thickness in the nanometer range and contains two continuous layers. The term continuous layer within the meaning of the present invention refers to a uniform layer covering more than 90%, preferably more than 95%, and most preferably more than 98% of the underlying surface of the semiconductor wafer on which it is deposited.

The layers in the periodic structure are preferably continuous layers. In the present invention, the superlattice structure comprises 20 to 120, preferably 20 to 100, more preferably 20 to 60, periods, wherein each period consists of a, preferably continuous, layer of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and a, preferably continuous, layer of $\text{Al}_y\text{Ga}_{1-y}\text{N}$, with $0.7 \leq x \leq 1.0$ and $0.0 \leq y \leq 0.5$, preferably $0.80 \leq x \leq 1.00$ and $0.05 \leq y \leq 0.40$, most preferred $0.90 \leq x \leq 1.00$ and $0.10 \leq y \leq 0.20$. In a particularly preferred embodiment, the superlattice structure comprises 20 to 40 periods. Preferably, each period of the superlattice structure has a thickness of not less than 18 nm and not more than 50 nm. More preferably, in each period of the super lattice structure, the layer of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ has preferably a thickness of not less than 3 nm and not more than 15 nm and the layer of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ has preferably a thickness of not less than 15 nm and not more than 35 nm. The average Al content of the superlattice structure is preferably less than 50 wt.%. Dislocations are also bent at the interfaces between each layer of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and each layer of $\text{Al}_y\text{Ga}_{1-y}\text{N}$, due to the strain field, which also results in a higher probability of annihilation. Thus, the superlattice structure promotes the annihilation of dislocations, so that monocrystalline, doped or non-doped GaN layers with a lower dislocation density can be deposited on top of the superlattice structure. The desired degree of annihilation of dislocation is achieved when the superlattice structure contains 20 to 120 periods of continuous layers, preferably 20 to 100 periods, more preferably 20 to 60 periods, most preferably 20 to 40 periods of continuous layers.

In a preferred embodiment, the total thickness of the layers located between the monocrystalline silicon substrate and the one or more monocrystalline, doped GaN layers is not less than 0.7 μm and not more than 1.5 μm . Thus, the semiconductor wafer according to the first aspect of the present invention has a relatively thin buffer layer and thus provides the basis for an easier production process and the production of thinner structures.

The multilayered structure may also comprise a second super lattice structure located between the first super lattice structure and the one or more monocrystalline, doped GaN layers. The second super lattice structure comprises periods, wherein each of the periods consists of a layer of $\text{Al}_m\text{Ga}_{1-m}\text{N}$ and a layer of $\text{Al}_n\text{Ga}_{1-n}\text{N}$ with $m < x$ and

$n < y$. The second super lattice structure has a lower average Al content compared to the super lattice structure as defined in claim 1.

In essence, the presence of island of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$ and a superlattice structure with continuous layers consisting of these materials allow the deposition of relatively thick monocrystalline, doped GaN layers which are free of cracks and have low dislocation density. At the same time, the total thickness of the layers located between the monocrystalline silicon substrate and the one or more monocrystalline, doped GaN layers is relatively low. This is due to the fact that the growth of both the superlattice structure and the islands is an effective way to bend and annihilate dislocations leading to a drastic reduction in dislocation density in a relatively thin set of layers. Thus, it is possible to avoid time-consuming conventional methods such as ELOG and thick buffer structures to achieve similar dislocation densities. In addition, sufficient compressive stress can be obtained by the deposition of the islands and the super lattice structure, so that the tensile stress during cooling can be compensated.

As the one or more monocrystalline, doped GaN layers deposited on top of the super lattice act as device layers, their composition, structure and stacking order depends on the application. The one or more monocrystalline, doped GaN layers have a thickness of not less than $6\text{ }\mu\text{m}$, preferably of not less than $7\text{ }\mu\text{m}$. The one or more monocrystalline, doped GaN layer preferably comprises a drain layer, a drift layer and a p-doped GaN layer in this order. In a preferred embodiment, the one or more monocrystalline, doped GaN layers preferably comprise an n-doped GaN layer as the drain layer, a further n-doped GaN layer as the drift layer and a p-doped GaN layer in this order. The n-dopant is preferably Si and the p-dopant is preferably Mg.

At least one of the one or more monocrystalline, doped GaN layers has a threading dislocation density of not more than $5.0 \times 10^8\text{ cm}^{-2}$. The threading dislocation density can be determined by various methods. In the present invention, the threading dislocation density is preferably determined by means of transmission electron microscopy (TEM) or scanning electron microscopy (SEM) by recording an image in plan-view of the semiconductor wafer with the one or more monocrystalline, doped GaN layers and counting the dislocations on the recorded image. In another

embodiment of the present invention, at least one of the one or more monocrystalline, doped GaN layers has a threading dislocation density (TDD) in the range of $8.5 \times 10^8 \text{ cm}^{-2}$ to $1.2 \times 10^9 \text{ cm}^{-2}$.

In a more preferred embodiment, the drift layer has a thickness of not less than $3 \mu\text{m}$,
5 preferably not less than $4 \mu\text{m}$ and most preferably not less than $6 \mu\text{m}$.

Generally, the one or more monocrystalline, doped GaN layers may contain a p-type dopant and/or an n-type dopant. The p-type dopant is preferably one or more element selected from the group consisting of Mg, Be, Zn and C. The n-type dopant is preferably one or more element selected from the group consisting of Si, Ge, Sn, O
10 and C. The Si concentration in a Si-doped GaN layer is preferably not less than $1.0 \times 10^{15} \text{ cm}^{-3}$ and not more than $5.0 \times 10^{19} \text{ cm}^{-3}$, more preferably not less than $1.0 \times 10^{15} \text{ cm}^{-3}$ and not more than $1.0 \times 10^{18} \text{ cm}^{-3}$. If the Si-doped GaN layer is used as a drift layer, the Si concentration is preferably not less than $1.0 \times 10^{15} \text{ cm}^{-3}$ and not more than $5.0 \times 10^{16} \text{ cm}^{-3}$.

15 The Mg concentration in a Mg-doped GaN layer is preferably not less than $1.0 \times 10^{18} \text{ cm}^{-3}$ and not more than $5.0 \times 10^{20} \text{ cm}^{-3}$, more preferably not less than $1.0 \times 10^{19} \text{ cm}^{-3}$ and not more than $5.0 \times 10^{20} \text{ cm}^{-3}$. For a PIN diode, the application of a further thin cap layer is advantageous. Such cap layer has a thickness of not less than 10 nm and not more than 50 nm , more preferably of not less than 10 nm and not more than 30 nm ,
20 and a dopant concentration of not less than $5.0 \times 10^{19} \text{ cm}^{-3}$ and not more than $5.0 \times 10^{20} \text{ cm}^{-3}$. Most preferably, the cap layer has a dopant concentration of not less than $5.0 \times 10^{19} \text{ cm}^{-3}$ and not more than $1.0 \times 10^{20} \text{ cm}^{-3}$, wherein the dopant is Mg.

The oxygen concentration in the one or more monocrystalline, doped GaN layers is preferably less than $1.0 \times 10^{16} \text{ cm}^{-3}$. The carbon concentration in the one or more
25 monocrystalline, doped GaN layers is preferably less than $1.0 \times 10^{18} \text{ cm}^{-3}$, more preferably less than $5.0 \times 10^{17} \text{ cm}^{-3}$, and most preferably less than $5.0 \times 10^{16} \text{ cm}^{-3}$.

For example, the one or more monocrystalline, doped GaN layers may comprise one or more Si-doped GaN layers and one or more Mg-doped GaN layers. The

semiconductor wafer of claim 1 may also comprise one or more Sn-doped GaN layers.

For example, in one embodiment of the invention, the following layers may be deposited on the super lattice structure in this order:

5 A first Si-doped GaN layer, a second Si-doped GaN layer and a Mg-doped GaN layer, wherein the first Si-doped GaN layer has a higher Si concentration and a lower thickness compared to the second Si-doped GaN layer. Optionally, a further Mg-doped GaN layer can be deposited as cap layer. Such stack is suitable for the use as PIN-diode. The structure may also be used as a template for DMOSFETS.

10 In another embodiment of the invention, the following layers may be deposited on the super lattice structure in this order:

A first Si-doped GaN layer, a second Si-doped GaN layer, a Mg-doped GaN layer, a third Si-doped GaN layer and a fourth Si-doped GaN layer, wherein the second Si-doped GaN layer has a lower Si concentration and a higher thickness compared to
15 the other Si-doped GaN layers. Such structure is suitable for a trench MOSFET structure.

Preferably, the semiconductor wafer according to the first aspect of the present invention has an absolute wafer bow at room temperature of not more than 80 μm , more preferably not more than 50 μm , most preferably not more than 40 μm .

20 In the second aspect of the present invention, a method of producing a semiconductor wafer having a multilayered structure is provided. The method comprises the following steps in this order:

- (i) providing a monocrystalline silicon substrate having a {111} orientation;
- (ii) flowing a gas stream which comprises an aluminum precursor and no nitrogen
25 precursor over the substrate at a temperature of not less than 700 °C and not more than 900 °C so that the total amount of aluminum flown over the substrate is not less than 0.1 μmol and not more than 250 μmol ,

- (iii) depositing a low temperature AlN nucleation layer by flowing a gas stream comprising an aluminum precursor and a nitrogen precursor over the substrate at a temperature of not less than 700 °C and not more than 900 °C,
 - (iv) depositing a high temperature AlN nucleation layer by flowing a gas stream comprising an aluminum precursor and a nitrogen precursor over the substrate at a temperature of not less than 950 °C and not more than 1100 °C,
 - (v) depositing an $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer with $0.3 \leq z \leq 0.7$ by flowing a gas stream comprising an aluminum precursor, a gallium precursor and a nitrogen precursor over the substrate at a temperature of not less than 950 °C and not more than 1050 °C,
 - (vi) depositing alternately $\text{Al}_x\text{Ga}_{1-x}\text{N}$ with $0.7 \leq x \leq 1.0$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$ with $0 \leq y \leq 0.5$ for 20 to 120 cycles by flowing a gas stream comprising an aluminum precursor, a gallium precursor and a nitrogen precursor over the substrate at a temperature of not less than 950°C and not more than 1100°C, wherein the alternation of the deposition is achieved by changing the composition of the gas stream; and
 - (vii) depositing one or more monocrystalline, doped GaN layers by flowing a gas stream comprising a gallium precursor, a nitrogen precursor and a dopant precursor over the substrate at a temperature of not less than 900 and not more than 1200°C.
- 20 In the method according to the second aspect of the present invention, various gas streams comprising precursor compounds are subsequently passed over the heated semiconductor wafer in a reactor with a reactor chamber. The reactor may be a horizontal laminar flow reactor, for example a commercially available planetary reactor from AIXTRON, or a vertical reactor, for example a commercially available vertical
- 25 rotating disc reactor from Veeco Instruments.

Various precursors are used. An aluminum precursor within the meaning of the present invention is preferably an organoaluminium compound, more preferably a trialkyl aluminum compound, most preferably trimethyl aluminum or triethyl aluminum. A nitrogen precursor within the meaning of the present invention is preferably ammonia or a trialkyl ammonium compound, more preferably ammonia. An inert

30 compound such as nitrogen is not considered as a nitrogen precursor within the

meaning of the present invention. The Ga precursor is preferably a trialkyl gallium compound, more preferably trimethyl gallium or triethyl gallium. Preferably, in each of steps (ii) to (vii), a carrier gas comprising one or more selected from the group of helium, argon, nitrogen and hydrogen is used. The use of hydrogen and/or nitrogen as
5 the carrier gas is particularly preferable. Most preferably, hydrogen is used as the carrier gas throughout steps (ii) to (vi).

The total pressure in steps (ii) to (vii) is preferably not less than 50 mbar and not more than 1000 mbar, more preferably not more than 500 mbar, even more preferably not more than 300 mbar and most preferably not more than 250 mbar. The total
10 pressures in steps (ii) to (vii) refer to the total pressure inside the reaction chamber during the respective step. In one embodiment, the total pressure in steps (ii) to (vi) is preferably in the range of 50 to 150 mbar.

The monocrystalline silicon substrate used in the method according to the second aspect of the invention is preferably a monocrystalline silicon substrate as described
15 in connection with the first aspect of the present invention. Preferably, the monocrystalline silicon substrate is annealed at a temperature above 800°C, preferably above 1000°C, to remove surface oxides and contamination from the surface of the substrate.

In step (ii), a gas stream comprising an aluminum precursor and no nitrogen precursor
20 is flown over the substrate at a temperature of not less than 700 °C and not more than 900 °C, so that the total amount of aluminum flown over the substrate is not less than 0.1 µmol and not more than 250 µmol.

The partial pressure of the aluminum precursor in the gas flow (*i.e.* the aluminum concentration therein), the volumetric flow rate and the duration of step (ii) is adjusted
25 so that the total amount of aluminum flown over the substrate in this step is not less than 0.1 µmol and not more than 250 µmol, preferably not less than 1 and not more than 100 µmol. The total amount of aluminum flown over the substrate in step (ii) is calculated from the volumetric flow rate of the gas stream, the concentration or partial pressure of the aluminum precursor in the gas stream and the flow time, *i.e.* the time

the gas stream is flown over the semiconductor wafer. Preferably, the time the gas stream is flown over the semiconductor wafer is not less than 2 and not more than 60 seconds, more preferably not less than 2 and not more than 20 seconds. This step is beneficial for preventing nitridation of the monocrystalline silicon substrate prior to the deposition of AlN.

In step (iii), a low temperature AlN nucleation layer is deposited by flowing a gas stream comprising an aluminum precursor and a nitrogen precursor over the substrate at a temperature of not less than 700 °C and not more than 900 °C, preferably not less than 750 °C and not more than 850 °C. The low temperature AlN nucleation layer is preferably a layer as defined in the first aspect of the present invention and has the purpose of providing nucleation sites for the growth of the high temperature AlN layer.

In step (iv), a high temperature AlN nucleation layer is deposited by flowing a gas stream comprising an aluminum precursor and a nitrogen precursor over the substrate at a temperature of not less than 950 °C and not more than 1100 °C, preferably not less than 1000 °C and not more than 1050 °C. The high temperature AlN nucleation layer is preferably a high temperature AlN nucleation layer as defined in the first aspect of the present invention.

In step (v), deposition of an $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer with $0.3 \leq z \leq 0.7$ occurs by flowing a gas stream comprising an aluminum precursor, a gallium precursor and a nitrogen precursor, and optionally a carrier gas such as hydrogen, over the substrate at a temperature of not less than 950 °C and not more than 1050 °C, preferably not less than 980 °C and not more than 1030 °C.

Under the above-mentioned conditions, V-pits are formed in the AlN layers. V-pits are voids having an inverse hexagonal pyramidal shape. The density and size of the V-pits depend on the conditions of AlN deposition. More particularly, the deposition of AlN layers under the conditions as defined in steps (iii) and (iv) results in a density of V-pits of not less than $5.0 \times 10^7 \text{ cm}^{-2}$ and not more than $5.0 \times 10^9 \text{ cm}^{-2}$. The V-pits were found to be associated with screw dislocations in the AlN layer and serve as the source of island growth. The subsequently deposited $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer is preferably

deposited in the V-pits and the subsequent growth of islands occurs on such V-pits filled with $\text{Al}_z\text{Ga}_{1-z}\text{N}$. As a result, the island density is *inter alia* dependent on the growth conditions in steps (iii) to (v). As explained above, an island density in the above-mentioned range promotes the annihilation of dislocations and thus reduces the dislocation density in the one or more monocrystalline, doped GaN layers.

In step (vi), $\text{Al}_x\text{Ga}_{1-x}\text{N}$ with $0.7 \leq x \leq 1.0$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$ with $0 \leq y \leq 0.5$ is deposited alternately for 20 to 120 cycles, preferably for 20 to 100 cycles, by flowing a gas stream comprising an aluminum precursor, a gallium precursor and a nitrogen precursor, and optionally a carrier gas such as hydrogen, over the substrate at a temperature of not less than 950°C and not more than 1100°C , preferably at a temperature of not less than 1000°C and not more than 1100°C . The alternation of the deposition is achieved by changing the composition of the gas stream. Preferably, in step (vi), $\text{Al}_x\text{Ga}_{1-x}\text{N}$ with $0.80 \leq x \leq 1.00$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$ with $0.05 \leq y \leq 0.40$ is deposited. Most preferably, $\text{Al}_x\text{Ga}_{1-x}\text{N}$ with $0.90 \leq x \leq 1.00$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$ with $0.10 \leq y \leq 0.20$.

In this step, islands and a super lattice structure is formed. During the first cycles of step (vi), preferably during at least 5 cycles, more preferably during the first 10 to 20 cycles, the vertical growth rate, *i.e.* the growth rate in a direction perpendicular to a plane of the monocrystalline silicon substrate with a $\{111\}$ orientation, is much higher compared to the horizontal growth rate, *i.e.* the growth rate along a plane of the monocrystalline silicon substrate with a $\{111\}$ orientation. This result in the formation of islands during the first cycles, preferably during at least 5 cycles, more preferably during 10 to 20 cycles. The dimensions, shape and density of the islands is controlled by the process conditions, in particular the temperature, pressure and the atomic ratio of group (v) to group (iii) elements in the gas phase, wherein only group (V) and group (III) elements from precursor compounds are taken into account. The process of island formation is also determined by the strain of the underlying layers. After the first cycles, preferably after not more than 20 cycles, the ratio of the vertical growth rate to the horizontal growth rate is decreased, so that the islands coalesce and continuous layers are deposited. During the transition from island growth to the deposition of continuous layers, new dislocations, in particular threading dislocations, can be generated at the coalescence boundaries. To further reduce the dislocation density,

the superlattice is continued for at least 10 periods to prevent a high dislocation density and thus a fast relaxation of the initially compressive stressed GaN layer. Furthermore, the compressive stressed $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layer and tensile stressed $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer collectively produce an effective lattice parameter, which can be altered by
5 changing the Ga/Al ratio in the superlattice. This lattice parameter governs the amount of compressive stress in GaN.

Generally, in each of steps (ii) to (v), the gas stream satisfies an atomic ratio of group (V) elements resulting from the nitrogen precursor to group (III) elements resulting from the aluminum precursor and, if present, from the gallium precursor, of not less
10 than 5 and not more than 100. Preferably, the said ratio is not less than 10 and not more than 60. As N_2 is not considered as a precursor within the meaning of the present invention, the nitrogen originating from N_2 in the carrier gas is not taken into account, when calculating the above ratio. Preferably, the gas streams in steps (ii) to (vi) contain one or more carrier gases selected from the group of hydrogen, nitrogen,
15 helium and argon. More preferably, the gas stream in each of steps (ii) to (vi) contains hydrogen as the carrier gas. In one embodiment, the aluminum precursor is trimethylaluminum, the gallium precursor is trimethylgallium and the nitrogen precursor is ammonia. Generally, the chemical composition of the deposited layers depends on the atomic ratio of group (V) elements resulting from the nitrogen
20 precursor to group (III) elements resulting from the aluminum precursor and, if present, from the gallium precursor. The growth mode also depends on this ratio.

Preferably, the alternation of the deposition in each cycle of step (vi) is achieved by changing the composition of the gas stream so that the atomic ratio of group (V) elements resulting from the nitrogen precursor to group (III) elements resulting from
25 the aluminum precursor, and if present from the gallium precursor, in the gas stream is alternated between a first value of not more than 100 and a second value of not less than 200. In addition, the ratio of Al to Ga in the gas stream can be adjusted, in order to control the composition of the layers deposited in steps (v) and (vi). More preferably, the first value is not more than 50 and the second value is not less than
30 300. Most preferably, the first value is not less than 5 and not more than 50 and the second value is not less than 300 and not more than 500. In a particularly preferred

embodiment, the first value is not less than 10 and not more than 30 and the second value is not less than 350 and not more than 400.

In one embodiment, the method is carried out in a reactor chamber having a total pressure of not less than 50 mbar and not more than 500 mbar throughout steps (ii) to 5 (vii). The total pressure in the reaction chamber in step (iv) is preferably not less than 50 mbar and not more than 300 mbar. Most preferably, the total pressure in the reaction chamber in step (iv) is not less than 50 mbar and not more than 150 mbar.

The growth rate throughout steps (i) to (iv) is preferably in the range of 100 to 1500 nm/h. In steps (i) to (iii), the growth rate is more preferably in the range of 100 to 300 10 nm/h. Preferably, in step (vi), the growth rate of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is in the range of 100 to 500 nm/h and the growth rate of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ is in the range of 700 to 1300 nm/h. The growth rate can be influenced by adjusting the temperature, the flow rate, the total pressure in the reaction chamber and the precursor concentration in the gas flow. In step (vii), the gas stream is preferably adjusted according to the desired composition of the doped 15 GaN layer for each layer to be deposited.

If the one or more monocrystalline, doped GaN layers of the semiconductor wafer comprise a p-doped GaN layer, the wafer can be optionally in-situ annealed in a hydrogen-free atmosphere. Preferably, in-situ annealing occurs at a temperature of not less than 700 and not more than 900°C. In-situ annealing allows electrical 20 activation of the p-doped GaN layer, in particular of Mg-doped GaN layers.

Examples

A semiconductor wafer according to the first aspect of the present invention is produced in the following manner using the method of producing a semiconductor wafer according to the second aspect of the present invention:

25 Cross-sectional SEM operated in the inlens mode was used to investigate the island coalescence. Defect selective etching in KOH/NaOH melt at 465 °C for 4 min with subsequent observation by SEM was performed to measure the threading dislocation density (TDD) by determining the etch pit density. The defect counting was carried in

an automated way on 10 separate SEM images for each sample to ensure statistical significance of the TDD. The dislocation network was further analyzed by weak beam dark field TEM using a FEI Titan 80-300 operating at 300 keV. Cross-sectional specimens were prepared by conventional mechanical grinding, followed by
5 chemomechanical polishing and ion milling with an Ar ion beam. Finally, the TDD was determined using TEM in plan-view, which complemented the TDD determination by DSE.

A silicon substrate wafer (111) with a diameter of 150 mm and thickness of 750 μm is used as the substrate.

10 The nitride layers are deposited by metalorganic chemical vapour deposition (MOCVD) using trimethylgallium, trimethylaluminium, bis-methylcyclopentadienyl magnesium, silane and ammonia as precursors and hydrogen and nitrogen as carrier gases.

In Examples 1 to 5, the deposition of layers on the substrate by means of MOCVD
15 was carried out in a commercially available vertical rotating disc reactor from Veeco Instruments. The pressure in steps (ii) to (vi) was about 100 mbar and the pressure in step (vii) was about 200 mbar.

The deposition is carried out with the following steps in this order:

The substrate is heated and annealed at 1050 $^{\circ}\text{C}$ to remove the surface oxide and
20 contaminations from the substrate surface. A gas stream comprising an aluminum precursor is flown over the substrate at a temperature of 800 $^{\circ}\text{C}$, wherein the gas flow, the precursor concentration/partial pressure and the flow time are adjusted so that the total amount of aluminum flown over the substrate is about 10 μmol .

Then, the temperature is ramped down to 800 $^{\circ}\text{C}$; a 1 nm thick low temperature AlN
25 nucleation layer is deposited at 800 $^{\circ}\text{C}$ followed by growth interruption. The temperature is ramped up to 1050 $^{\circ}\text{C}$ and a 200 nm thick high temperature AlN nucleation layer is deposited at 1050 $^{\circ}\text{C}$ followed by growth interruption. The temperature is ramped down to 1010 $^{\circ}\text{C}$ and a 25 nm thick $\text{Al}_{0.51}\text{Ga}_{0.49}\text{N}$ layer is

deposited at 1010 °C followed by a growth interruption. Then, a sequence of deposition of 6 nm thick AlN and 26 nm thick $\text{Al}_{0.12}\text{Ga}_{0.88}\text{N}$ is repeated 41 times at 1010 °C, followed by growth interruption. After that, a 800 nm thick GaN:Si layer with a silicon concentration of $5.0 \times 10^{18} \text{ cm}^{-3}$ is deposited as drain layer, followed by growth interruption. A 3.5 μm thick GaN:Si layer with a silicon concentration of $4.0 \times 10^{16} \text{ cm}^{-3}$ is deposited as the drift layer, followed by growth interruption. A 700 nm thick GaN:Mg layer with a magnesium concentration of $5.0 \times 10^{19} \text{ cm}^{-3}$ is deposited, followed by growth interruption and cooling to room temperature. The threading dislocation density was determined by means of transmission electron microscopy (TEM), in particular by means of plan view transmission electron microscopy. The TEM analysis revealed a threading dislocation density of $3.5 \times 10^8 \text{ cm}^{-2}$.

The material obtained in Example 1 is a PIN diode and was subsequently tested for its electrical properties by measuring the electrical current at different voltages. The reverse current–voltage curves obtained by these measurements are shown in Fig. 2a. Fig. 2b shows the temperature-dependent breakdown voltage of the PIN diode produced in Example 1. The curve shows an increase in breakdown voltage with temperature, which is characteristic of avalanche breakdown. This is evidence of good electrical properties of the material obtained in Example 1. In contrast, poor material quality would lead to early breakdown due to high leakage currents that could not support avalanche breakdown.

Example 2 was carried out under the same process conditions as Example 1, except that only 5 sequences/cycles of deposition of 6 nm thick AlN and 26 nm thick $\text{Al}_{0.12}\text{Ga}_{0.88}\text{N}$ are carried out, before growth is interrupted and an image in a scanning electron microscope in plan view (SEM) is recorded. Fig. 1 shows the recorded SEM image. The total density of islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ is determined from the image to be less than $1.0 \times 10^9 \text{ cm}^{-2}$.

Examples 3 and 4 were carried out under the same conditions as Example 1, except that GaN drift layers with a thickness of 3 μm and 4.5 μm , respectively, were deposited, so that the total thickness of the set of GaN layers deposited on top of the buffer layer was 4.5 μm and 6 μm , respectively. After that, PIN diodes were prepared

form these materials. The two PIN diodes obtained in Examples 3 and 4 were both tested for their electrical properties by measuring the reverse I-V curves at room temperature. These reverse I-V curves are shown in Fig. 3 and provide evidence of the good electrical properties of these materials.

- 5 In Example 5, the same buffer layer as in Example 1 was prepared. After the preparation of the buffer layer, a 400 nm thick GaN:Si layer with a silicon concentration of $5.0 \times 10^{18} \text{ cm}^{-3}$ is deposited on top of the super lattice structure as drain layer, followed by growth interruption. A 6 μm thick GaN:Si layer with a silicon concentration of $4.0 \times 10^{16} \text{ cm}^{-3}$ is deposited as the drift layer, followed by growth
10 interruption. A 600 nm thick GaN:Mg layer with a magnesium concentration of $2.0 \times 10^{19} \text{ cm}^{-3}$ is deposited, followed by growth interruption. Finally, a Mg cap layer having a thickness of 30 nm and a magnesium concentration of $1.0 \times 10^{20} \text{ cm}^{-3}$ is deposited, followed by growth interruption. Before cooling to room temperature, the sample can be annealed at 800°C in nitrogen atmosphere. Fig. 4a shows a schematic
15 drawing and Fig. 4 b shows an SEM image of the semiconductor wafer obtained in Example 5. Fig. 5 shows an image of the wafer obtained in Example 5 recorded on an optical microscope. Fig. 5 demonstrates that the present invention enables the deposition a crack-free set of GaN layers with a total thickness of 7 μm , including a crack-free drift layer having a thickness of 6 μm .
- 20 In Example 6, the same buffer layer as in Example 1 was prepared. By using the described buffer consisting of islands, crack-free GaN layers with a total thickness of more than 7 μm could be realised on Si (111) substrates having a diameter of 150 mm. An absolute wafer bow of less than 50 μm was observed. PIN diodes were processed on a wafer with the following active layer stack: a 500 nm thick n-type GaN
25 drain layer, a 6500 nm thick n-type drift layer, and a 630 nm thick p-type GaN layer. The JV blocking characteristic of such diode revealed a hard breakdown at about 1130 V, as shown in Fig. 9.

Claims

1. A semiconductor wafer having a multilayered structure and a diameter of not less than 150 mm and not more than 300 mm, wherein the multilayered structure comprises in this order
- 5 a monocrystalline silicon substrate having a {111} orientation;
 at least one AlN nucleation layer;
 an $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer;
 islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$;
 a superlattice structure comprising 20 to 120 periods, each period consisting of a
10 layer of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and a layer of $\text{Al}_y\text{Ga}_{1-y}\text{N}$; and
 one or more monocrystalline, doped GaN layers having a total thickness of not less than 6 μm ,
 wherein at least one of the one or more monocrystalline, doped GaN layers has a threading dislocation density of not more than $5.0 \times 10^8 \text{ cm}^{-2}$, and
15 wherein $0.3 \leq z \leq 0.7$; $0.7 \leq x \leq 1.0$; and $0 \leq y \leq 0.5$.
2. The semiconductor wafer according to claim 1, wherein $0.80 \leq x \leq 1.00$ and $0.05 \leq y \leq 0.40$.
- 20 3. The semiconductor wafer according to claim 1 or 2, wherein each period of the superlattice structure has a thickness of not less than 18 nm and not more 50 nm.
4. The semiconductor wafer according to any one of claims 1 to 3, wherein the average Al content of the superlattice structure is less than 50 wt.%.
25
5. The semiconductor wafer according to any one of claims 1 to 4, wherein the total density of islands of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and islands of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ is not less than $5.0 \times 10^7 \text{ cm}^{-2}$ and not more than $5.0 \times 10^9 \text{ cm}^{-2}$.
- 30 6. The semiconductor wafer according to any one of claims 1 to 5, wherein the islands have an aspect ratio of not less than 0.1 and not more than 10.

7. The semiconductor wafer according to any one of claims 1 to 6, wherein the height of the islands is not less than 100 nm and not more than 1000 nm.

8. The semiconductor wafer according to any one of claims 1 to 7, wherein the
5 total thickness of the layers located between the monocrystalline silicon substrate and the one or more monocrystalline, doped GaN layers is not less than 0.7 μm and not more than 1.5 μm .

9. The semiconductor wafer according to any one of claims 1 to 8, wherein the
10 total thickness of the at least one AlN nucleation layer is not less than 50 nm and not more than 500 nm.

10. The semiconductor wafer according to any one of claims 1 to 9, wherein the multilayered structure comprises a second super lattice structure located between the
15 first super lattice structure and the one or more monocrystalline, doped GaN layers, and the second super lattice structure has a lower average Al content than the superlattice structure as defined in claim 1.

11. Method of producing a semiconductor wafer having a multilayered structure
20 comprising the following steps in this order

- (i) providing a monocrystalline silicon substrate having a {111} orientation;
- (ii) flowing a gas stream which comprises an aluminum precursor and no nitrogen precursor over the substrate at a temperature of not less than 700 °C and not more than 900 °C so that the total amount of aluminum flown over the
25 substrate is not less than 0.1 μmol and not more than 250 μmol ,
- (iii) depositing a low temperature AlN nucleation layer by flowing a gas stream comprising an aluminum precursor and a nitrogen precursor over the substrate at a temperature of not less than 700 °C and not more than 900 °C,
- (iv) depositing a high temperature AlN nucleation layer by flowing a gas stream
30 comprising an aluminum precursor and a nitrogen precursor over the substrate at a temperature of not less than 950 °C and not more than 1100 °C,
- (v) depositing an $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer with $0.3 \leq z \leq 0.7$ by flowing a gas stream comprising an aluminum precursor, a gallium precursor and a nitrogen

precursor over the substrate at a temperature of not less than 950 °C and not more than 1050 °C,

- (vi) depositing alternately $\text{Al}_x\text{Ga}_{1-x}\text{N}$ with $0.7 \leq x \leq 1.0$ and $\text{Al}_y\text{Ga}_{1-y}\text{N}$ with $0 \leq y \leq 0.5$ for 20 to 120 cycles by flowing a gas stream comprising an aluminum precursor, a gallium precursor and a nitrogen precursor over the substrate at a temperature of not less than 950°C and not more than 1100°C, wherein the alternation of the deposition is achieved by changing the composition of the gas stream; and
- (vii) depositing one or more monocrystalline, doped GaN layers by flowing a gas stream comprising a gallium precursor, a nitrogen precursor and a dopant precursor over the substrate at a temperature of not less than 900°C and not more than 1200°C.

12. The method of producing a semiconductor wafer having a multilayered structure according to claim 11, wherein, in each of steps (ii) to (iv), the gas stream satisfies an atomic ratio of group (V) elements resulting from the nitrogen precursor to group (III) elements resulting from the aluminum precursor of not less than 5 and not more than 100.

13. The method of producing a semiconductor wafer having a multilayered structure according to claim 11 or 12, wherein the alternation of the deposition in each cycle of step (vi) is achieved by changing the composition of the gas stream so that the atomic ratio of group (V) elements resulting from the nitrogen precursor to group (III) elements resulting from the aluminum precursor and, if applicable, the gallium precursor, in the gas stream is alternated between a first value of not more than 100 and a second value of not less than 200.

14. The method of producing a semiconductor wafer having a multilayered structure according to any one of claims 11 to 13, wherein the method is carried out in a reactor chamber having a total pressure of not less than of 50 and not more than 300 mbar throughout steps (ii) to (vii).

15. The method of producing a semiconductor wafer having a multilayered structure according to any one of claims 11 to 14, wherein in step (vi) the growth rate of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is in the range of 100 to 500 nm/h and the growth rate of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ is in the range of 700 to 1300 nm/h.