CLAIMS

1. A liquid crystal display device comprising:

a display portion including a plurality of video signal lines, a plurality of scanning signal lines crossing the video signal lines, a plurality of pixel forming portions including respective pixel electrodes arranged in a matrix so as to correspond to the video signal lines and the scanning signal lines, a plurality of auxiliary capacitance lines arranged along the scanning signal lines, and auxiliary capacitors formed between the auxiliary capacitance lines and the pixel electrodes corresponding to the scanning signal lines along the auxiliary capacitance lines;

a display control circuit for generating clock signals alternating between on- and off-levels cyclically;

a scanning signal line driver circuit for driving the scanning signal lines such that a scanning period in which the scanning signal lines are selected sequentially and an idle period in which all of the scanning signal lines are in an unselected state alternate with each other in cycles of a frame period consisting of the scanning period and the idle period; and

an auxiliary capacitance line driver circuit formed integrally with the display portion to drive the auxiliary capacitance lines independently of one another in accordance with auxiliary capacitance clock signals included in the clock signals, wherein,

the auxiliary capacitance line driver circuit includes a first shift register with a plurality of first bistable circuits cascaded to one another, the first shift register

sequentially setting output signals from the first bistable circuits to an on-level in accordance with the first shift operation clock signals included in the auxiliary capacitance clock signals, and

the first shift operation clock signals have a lower frequency during the idle period than during the scanning period.

2. The liquid crystal display device according to claim 1, wherein the first shift operation signals have a lower amplitude during the idle period than during the scanning period.

3. The liquid crystal display device according to claim 1, wherein the idle period is longer than the scanning period.

4. The liquid crystal display device according to claim 1, wherein,

the auxiliary capacitance line driver circuit further includes a plurality of first switching elements with first conduction terminals respectively connected to the auxiliary capacitance lines,

the display control circuit provides a bias signal to a second conduction terminal of each of the first switching elements, the bias signal switching between two potentials every frame period and being fixed at one of the potentials during each frame period, and

each of the first switching elements is provided with an output signal at a control terminal, the output signal being derived from the first bistable circuit that corresponds to the auxiliary capacitance line connected to the first conduction

terminal of the first switching element.

5. The liquid crystal display device according to claim 4, wherein,

the display control circuit provides a first bias signal as the bias signal to the second conduction terminal of one of the first switching elements whose first conduction terminals are respectively connected to adjacent auxiliary capacitance lines, and also provides a second bias signal as the bias signal to the second conduction terminal of the other of the first switching elements whose first conduction terminals are respectively connected to the adjacent auxiliary capacitance lines, and

the first bias signal and the second bias signal differ in potential during each frame period.

6. The liquid crystal display device according to claim 4, wherein,

the auxiliary capacitance line driver circuit further includes a plurality of second switching elements respectively corresponding to the first switching elements,

the display control circuit provides an idle-period operation clock signal included in the auxiliary capacitance clock signal to a control terminal of each of the second switching elements, the idle-period operation clock signal having a potential that is at an off-level during the scanning period and that alternates between on- and off-levels cyclically during the idle period, and also having a lower frequency during the idle period than a frequency of the first shift operation signals during the scanning period,

a first conduction terminal of each of the second switching elements is connected to the auxiliary capacitance line that is connected to the first conduction terminal of the first switching element that corresponds to the second switching element, and

the bias signal provided to the second conduction terminal of the first switching element that corresponds to the second switching element is provided to a second conduction terminal of each of the second switching elements.

7. The liquid crystal display device according to claim 1, wherein the first shift operation clock signals are of three or more phases different from one another.

8. The liquid crystal display device according to claim 1, wherein the scanning signal line driver circuit is formed integrally with the display portion.

9. The liquid crystal display device according to claim 8, wherein the scanning signal line driver circuit includes a second shift register for sequentially setting output signals from a plurality of second bistable circuits cascaded to one another, to an on-level in accordance with a plurality of second shift operation clock signals included in the clock signals, the scanning signal line driver circuit providing the output signals from the second bistable circuits to the scanning signal lines, respectively.

10. The liquid crystal display device according to claim 8, wherein,

the scanning signal line driver circuit and the auxiliary capacitance line driver circuit share the first shift register,

the scanning signal line driver circuit further includes a plurality of output buffers provided corresponding to the first bistable circuits respectively,

the display control circuit provides the output buffers with buffer input signals being set at an on-level during the scanning period and also at an off-level during the idle period, and

the output buffers provide the scanning signal lines with logical ANDs of the buffer input signals and output signals from the first bistable circuits corresponding thereto.

11. The liquid crystal display device according to any one of claims 1 through 7, wherein the auxiliary capacitance line driver circuit is realized using thin-film transistors whose semiconductor layers are made of an oxide semiconductor.

12. The liquid crystal display device according to any one of claims 8 through 10, wherein the scanning signal line driver circuit and the auxiliary capacitance line driver circuit are realized using thin-film transistors whose semiconductor layers are made of an oxide semiconductor.

13. The liquid crystal display device according to any one of claims 1 through 7, wherein the auxiliary capacitance line driver circuit is realized using thin-film transistors whose semiconductor layers are made of amorphous silicon.

14. The liquid crystal display device according to any one of claims 8 through 10, wherein the scanning signal line driver circuit and the auxiliary capacitance line driver circuit are realized using thin-film transistors whose semiconductor layers are made of amorphous silicon.

15. A drive method for auxiliary capacitance lines in a liquid crystal display device provided with a display portion including a plurality of video signal lines, a plurality of scanning signal lines crossing the video signal lines, a plurality of pixel forming portions including respective pixel electrodes arranged in a matrix so as to correspond to the video signal lines and the scanning signal lines, a plurality of auxiliary capacitance lines arranged along the scanning signal lines, and auxiliary capacitors formed between the auxiliary capacitance lines and the pixel electrodes corresponding to the scanning signal lines along the auxiliary capacitance lines, a display control circuit for generating clock signals alternating between on- and off-levels cyclically, a scanning signal line driver circuit for driving the scanning signal lines, and an auxiliary capacitance line driver circuit formed integrally with the display portion to drive the auxiliary capacitance lines, the method comprising the steps of:

driving the scanning signal lines such that a scanning period in which the scanning signal lines are selected sequentially and an idle period in which all of the scanning signal lines are in an unselected state alternate with each other in cycles of a frame period consisting of the scanning period and the idle period;

driving the auxiliary capacitance lines

independently of one another in accordance with auxiliary capacitance clock signals included in the clock signals; and

setting first shift operation clock signals included in the auxiliary capacitance clock signals at a lower frequency during the idle period than during the scanning period, wherein,

the auxiliary capacitance line driver circuit includes a first shift register with a plurality of first bistable circuits cascaded to one another, the first shift register sequentially setting output signals from the first bistable circuits to an on-level in accordance with the first shift operation clock signals.

16. The drive method according to claim 15, wherein the first shift operation signals have a lower amplitude during the idle period than during the scanning period.

17. The drive method according to claim 15, wherein the idle period is longer than the scanning period.

18. The drive method according to claim 15, wherein the first shift operation clock signals are of three or more phases different from one another.

CLAIMS

1. A liquid crystal display device comprising:

a display portion including a plurality of video signal lines, a plurality of scanning signal lines crossing the video signal lines, a plurality of pixel forming portions including respective pixel electrodes arranged in a matrix so as to correspond to the video signal lines and the scanning signal lines, a plurality of auxiliary capacitance lines arranged along the scanning signal lines, and auxiliary capacitors formed between the auxiliary capacitance lines and the pixel electrodes corresponding to the scanning signal lines along the auxiliary capacitance lines;

a display control circuit for generating clock signals alternating between on- and off-levels cyclically;

a scanning signal line driver circuit for driving the scanning signal lines such that a scanning period in which the scanning signal lines are selected sequentially and an idle period in which all of the scanning signal lines are in an unselected state alternate with each other in cycles of a frame period consisting of the scanning period and the idle period; and

an auxiliary capacitance line driver circuit formed integrally with the display portion to drive the auxiliary capacitance lines independently of one another in accordance with auxiliary capacitance clock signals included in the clock signals, wherein,

the auxiliary capacitance line driver circuit includes a first shift register with a plurality of first bistable circuits cascaded to one another, the first shift register sequentially setting output signals from the first bistable circuits to an on-level in accordance with first shift operation clock signals included in the auxiliary capacitance clock signals, and

the first shift operation clock signals have a lower frequency during the idle period than during the scanning period.

2. The liquid crystal display device according to claim 1, wherein the first shift operation clock signals have a lower amplitude during the idle period than during the

scanning period.

3. The liquid crystal display device according to claim 1, wherein the idle period is longer than the scanning period.

4. The liquid crystal display device according to claim 1, wherein,

the auxiliary capacitance line driver circuit further includes a plurality of first switching elements with first conduction terminals respectively connected to the auxiliary capacitance lines,

the display control circuit provides a bias signal to a second conduction terminal of each of the first switching elements, the bias signal switching between two potentials every frame period and being fixed at one of the potentials during each frame period, and

each of the first switching elements is provided with an output signal at a control terminal, the output signal being derived from the first bistable circuit that corresponds to the auxiliary capacitance line connected to the first conduction terminal of the first switching element.

5. The liquid crystal display device according to claim 4, wherein,

the display control circuit provides a first bias signal as the bias signal to the second conduction terminal of one of the first switching elements whose first conduction terminals are respectively connected to adjacent auxiliary capacitance lines, and also provides a second bias signal as the bias signal to the second conduction terminal of the other of the first switching elements whose first conduction terminals are respectively connected to the adjacent auxiliary capacitance lines, and

the first bias signal and the second bias signal differ in potential during each frame period.

6. The liquid crystal display device according to claim 4, wherein,

the auxiliary capacitance line driver circuit further includes a plurality of

second switching elements respectively corresponding to the first switching elements,

the display control circuit provides an idle-period operation clock signal included in the auxiliary capacitance clock signal to a control terminal of each of the second switching elements, the idle-period operation clock signal having a potential that is at an off-level during the scanning period and that alternates between on- and off-levels cyclically during the idle period, and also having a lower frequency during the idle period than a frequency of the first shift operation clock signals during the scanning period,

a first conduction terminal of each of the second switching elements is connected to the auxiliary capacitance line that is connected to the first conduction terminal of the first switching element that corresponds to the second switching element, and

the bias signal provided to the second conduction terminal of the first switching element that corresponds to the second switching element is provided to a second conduction terminal of each of the second switching elements.

7. The liquid crystal display device according to claim 1, wherein the first shift operation clock signals are of three or more phases different from one another.

8. The liquid crystal display device according to claim 1, wherein the scanning signal line driver circuit is formed integrally with the display portion.

9. The liquid crystal display device according to claim 8, wherein the scanning signal line driver circuit includes a second shift register for sequentially setting output signals from a plurality of second bistable circuits cascaded to one another, to an on-level in accordance with a plurality of second shift operation clock signals included in the clock signals, the scanning signal line driver circuit providing the output signals from the second bistable circuits to the scanning signal lines, respectively.

10. The liquid crystal display device according to claim 8, wherein,

the scanning signal line driver circuit and the auxiliary capacitance line driver circuit share the first shift register,

the scanning signal line driver circuit further includes a plurality of output buffers provided corresponding to the first bistable circuits respectively,

the display control circuit provides the output buffers with buffer input signals being set at an on-level during the scanning period and also at an off-level during the idle period, and

the output buffers provide the scanning signal lines with logical ANDs of the buffer input signals and output signals from the first bistable circuits corresponding thereto.

11. The liquid crystal display device according to claim 8, wherein the scanning signal line driver circuit and the auxiliary capacitance line driver circuit are realized using thin-film transistors whose semiconductor layers are made of an oxide semiconductor.

12. The liquid crystal display device according to claim 8, wherein the scanning signal line driver circuit and the auxiliary capacitance line driver circuit are realized using thin-film transistors whose semiconductor layers are made of amorphous silicon.

13. The liquid crystal display device according to claim 1, wherein the auxiliary capacitance line driver circuit is realized using thin-film transistors whose semiconductor layers are made of an oxide semiconductor.

14. The liquid crystal display device according to claim 1, wherein the auxiliary capacitance line driver circuit is realized using thin-film transistors whose semiconductor layers are made of amorphous silicon.

15. A drive method for auxiliary capacitance lines in a liquid crystal display device provided with a display portion including a plurality of video signal lines, a

plurality of scanning signal lines crossing the video signal lines, a plurality of pixel forming portions including respective pixel electrodes arranged in a matrix so as to correspond to the video signal lines and the scanning signal lines, a plurality of auxiliary capacitance lines arranged along the scanning signal lines, and auxiliary capacitors formed between the auxiliary capacitance lines and the pixel electrodes corresponding to the scanning signal lines along the auxiliary capacitance lines, a display control circuit for generating clock signals alternating between on- and off-levels cyclically, a scanning signal line driver circuit for driving the scanning signal lines, and an auxiliary capacitance line driver circuit formed integrally with the display portion to drive the auxiliary capacitance lines, the method comprising the steps of:

driving the scanning signal lines such that a scanning period in which the scanning signal lines are selected sequentially and an idle period in which all of the scanning signal lines are in an unselected state alternate with each other in cycles of a frame period consisting of the scanning period and the idle period;

driving the auxiliary capacitance lines independently of one another in accordance with auxiliary capacitance clock signals included in the clock signals; and

setting first shift operation clock signals included in the auxiliary capacitance clock signals at a lower frequency during the idle period than during the scanning period, wherein,

the auxiliary capacitance line driver circuit includes a first shift register with a plurality of first bistable circuits cascaded to one another, the first shift register sequentially setting output signals from the first bistable circuits to an on-level in accordance with the first shift operation clock signals.

16. The drive method according to claim 15, wherein the first shift operation clock signals have a lower amplitude during the idle period than during the scanning period.

17. The drive method according to claim 15, wherein the idle period is longer than the scanning period.

18. The drive method according to claim 15, wherein the first shift operation clock signals are of three or more phases different from one another.