FIG. 1

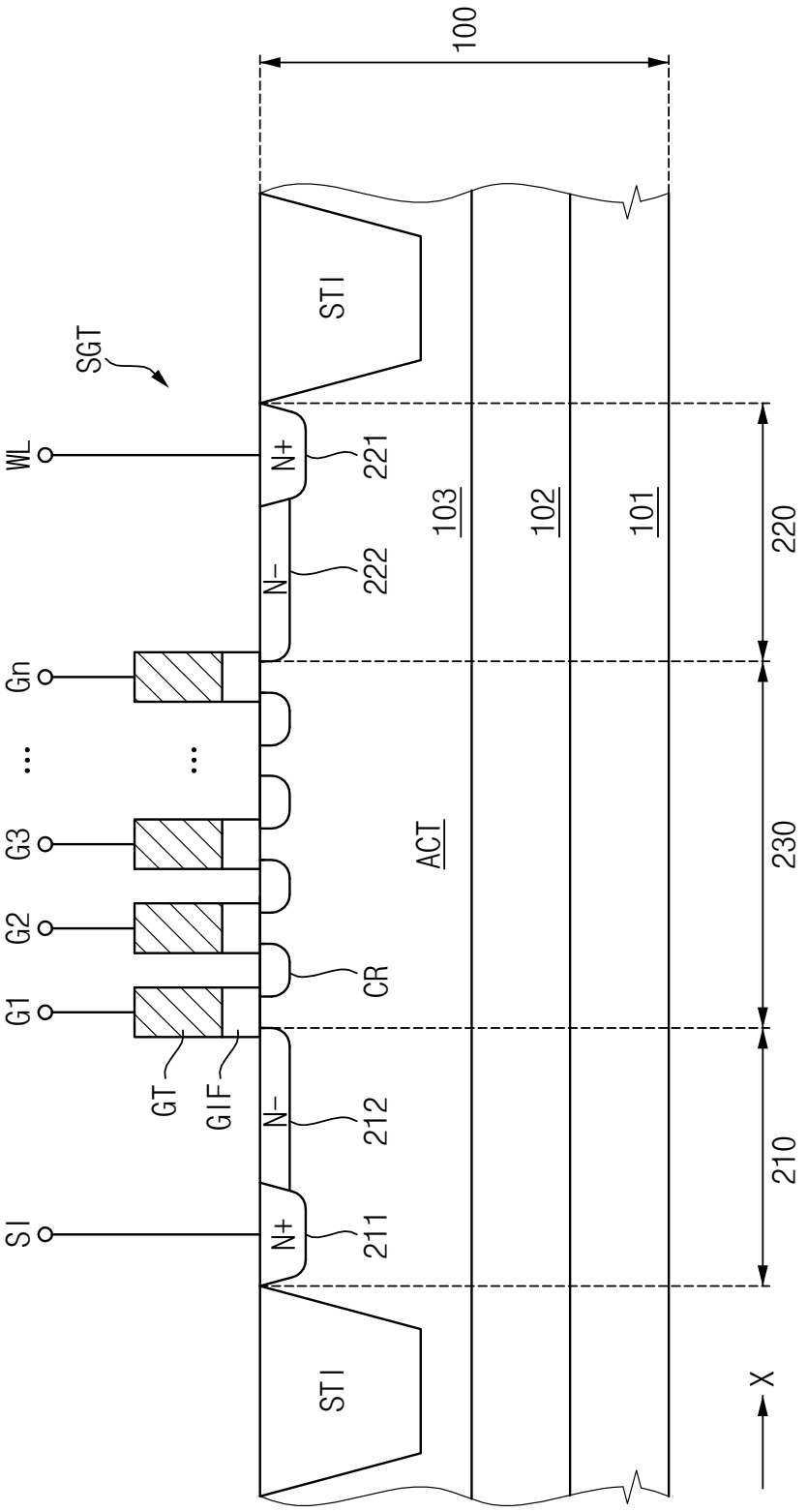

100
STI
SGT
WL
N+
221
103
102
101
220
N−
222
Gn
...
...
G3
G2
G1
ACT
230
CR
GT
GIF
N−
212
SI
N+
211
210
STI
X

FIG. 2

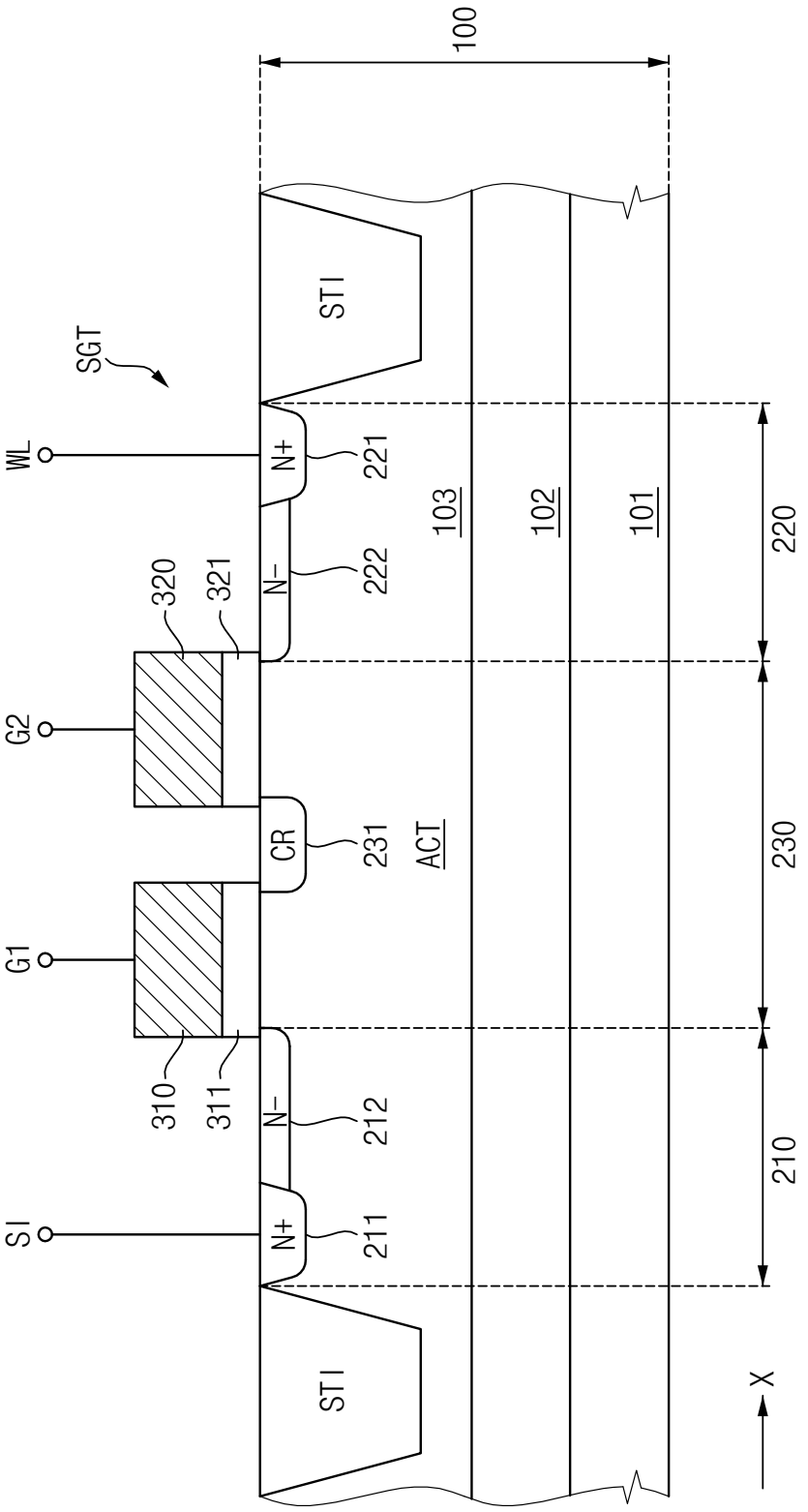

100
STI
SGT
WL
N+
221
103
102
101
220
320
321
N−
222
G2
CR
231
ACT
230
G1
310
311
N−
212
SI
N+
211
210
STI
X

FIG. 3

VSI > VWL	ON	VG1 > VSI,VG1 ≥ VG2
	OFF	VG2 < VSI,VG1 ≥ VG2
VSI < VWL	ON	VG2 > VWL,VG2 ≥ VG1
	OFF	VG1 > VWL,VG2 ≥ VG1

FIG. 4

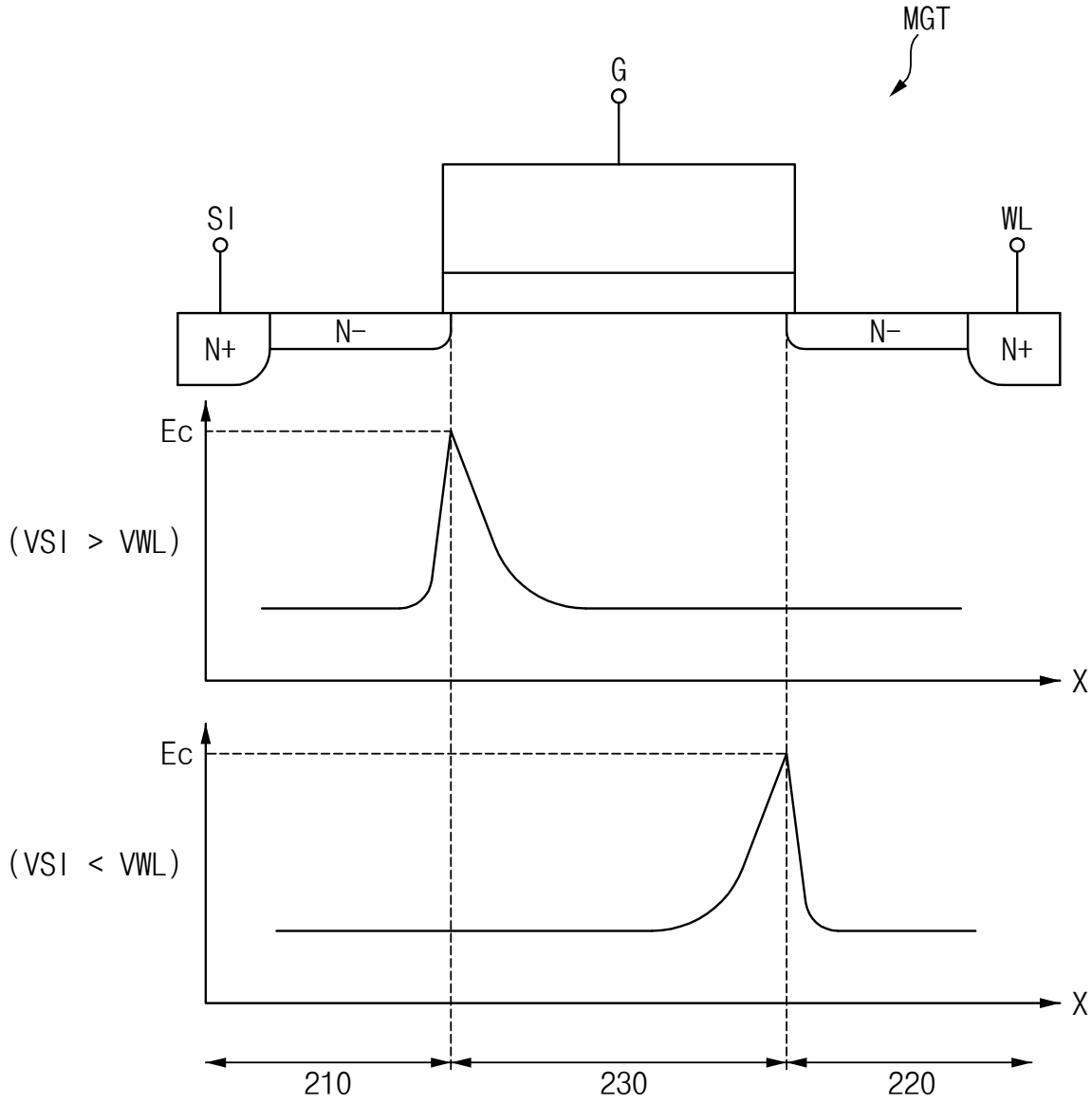


FIG. 5

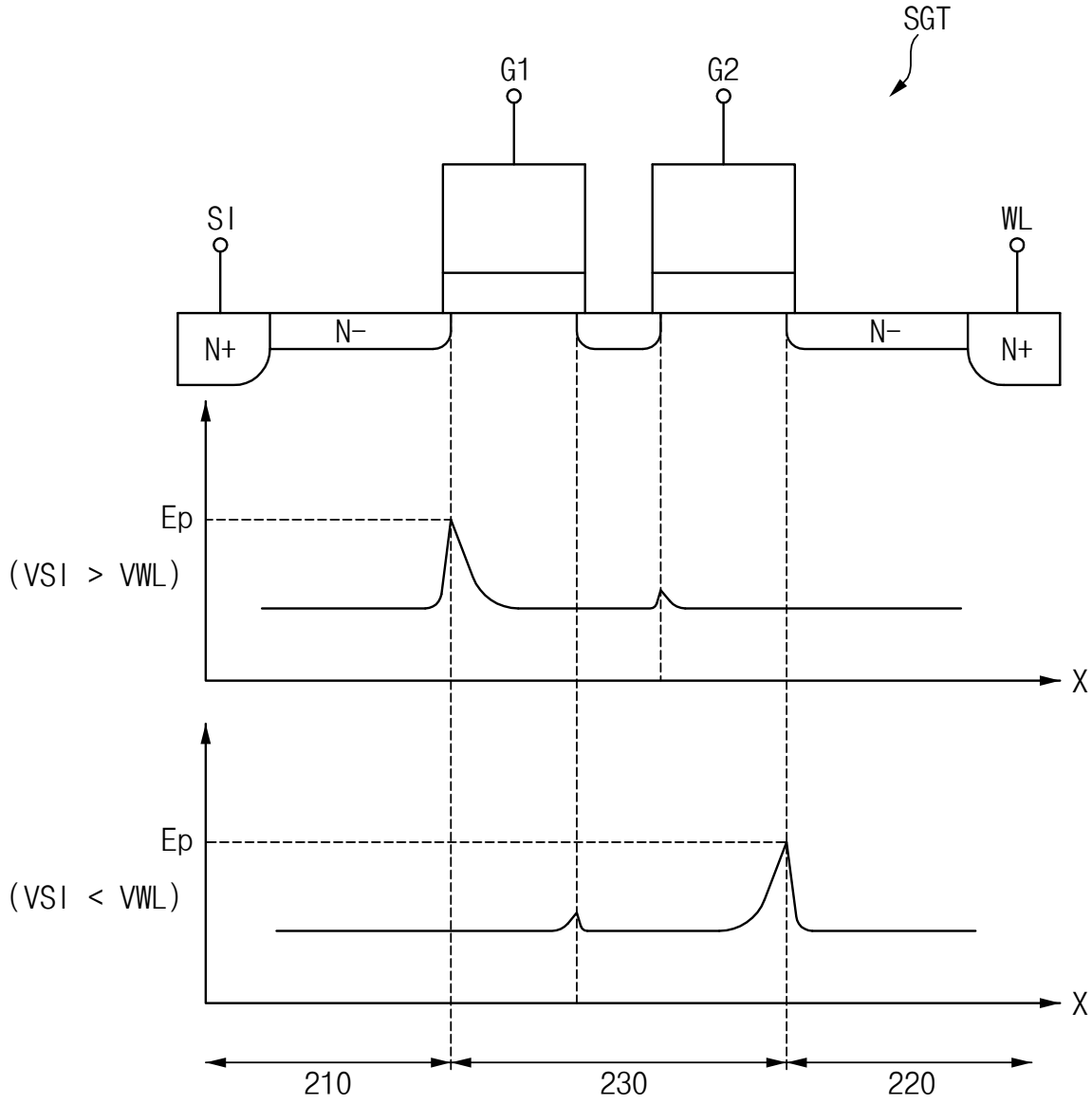


FIG. 6

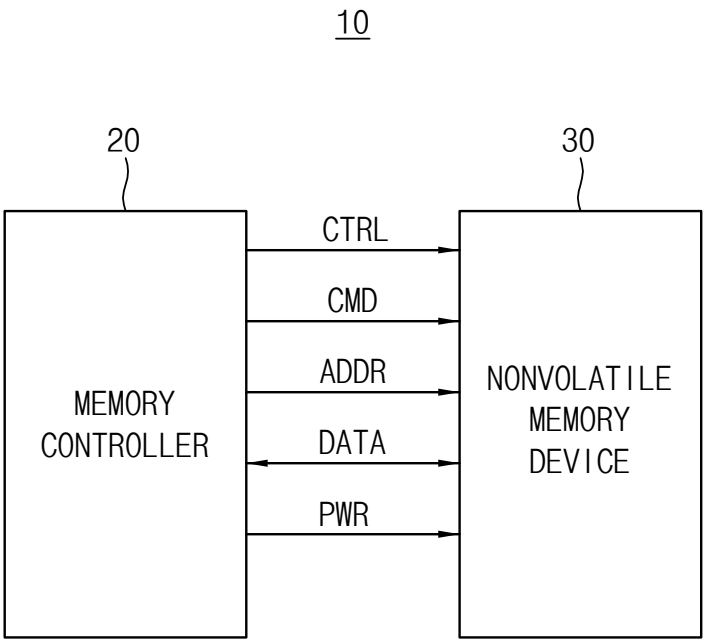

10
20
30
MEMORY CONTROLLER
NONVOLATILE MEMORY DEVICE
CTRL
CMD
ADDR
DATA
PWR

FIG. 7

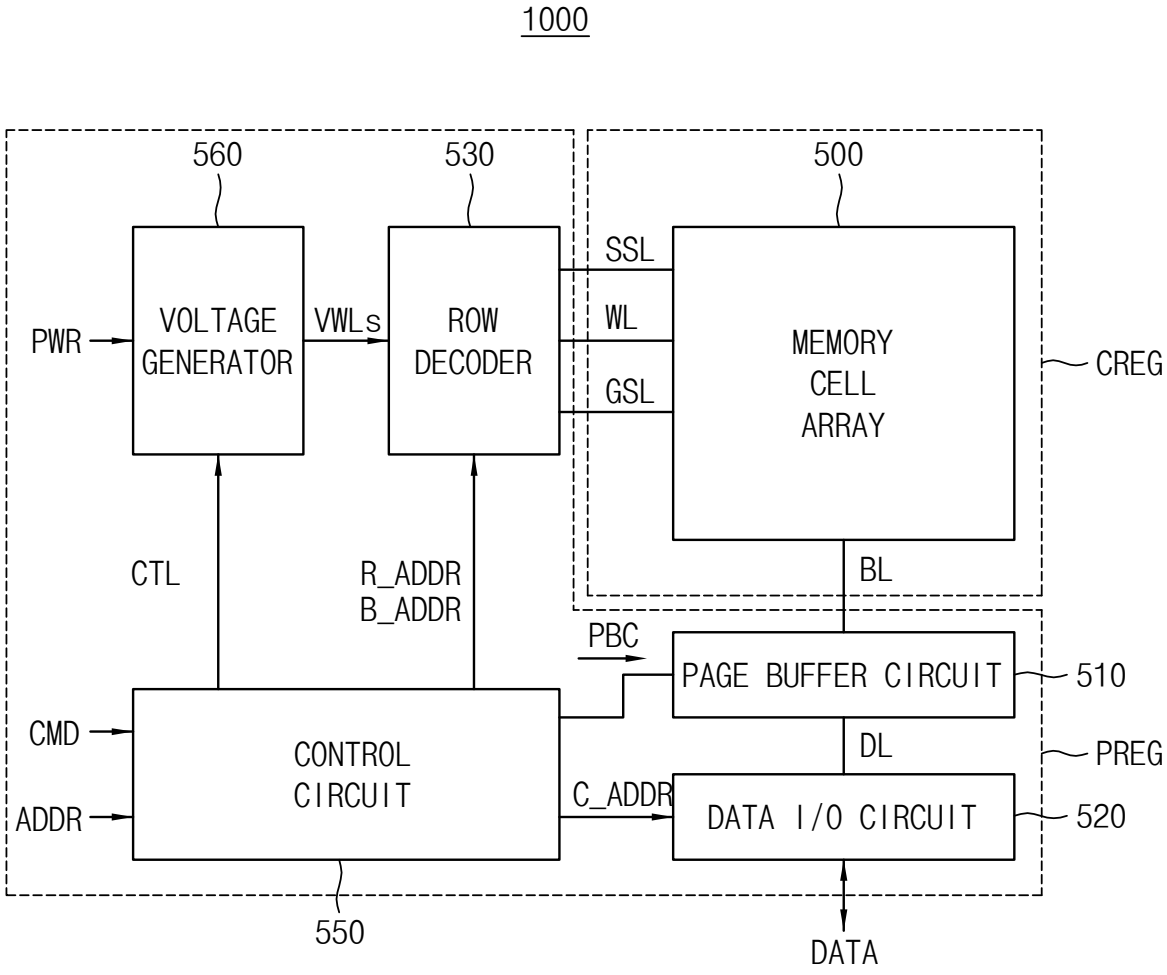

1000
560
530
500
VOLTAGE GENERATOR
VWLs
ROW DECODER
SSL
WL
GSL
MEMORY CELL ARRAY
CREG
PWR
CTL
R_ADDR
B_ADDR
BL
PBC
PAGE BUFFER CIRCUIT
510
CMD
ADDR
CONTROL CIRCUIT
DL
PREG
C_ADDR
DATA I/O CIRCUIT
520
550
DATA

FIG. 8

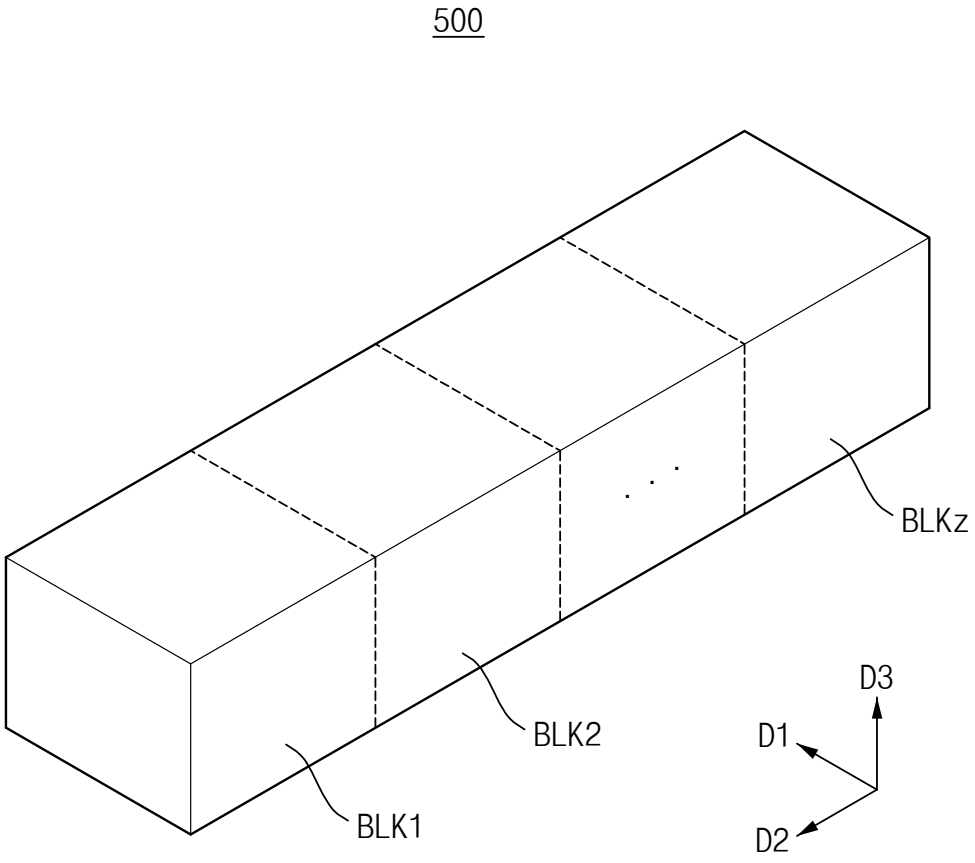


FIG. 9

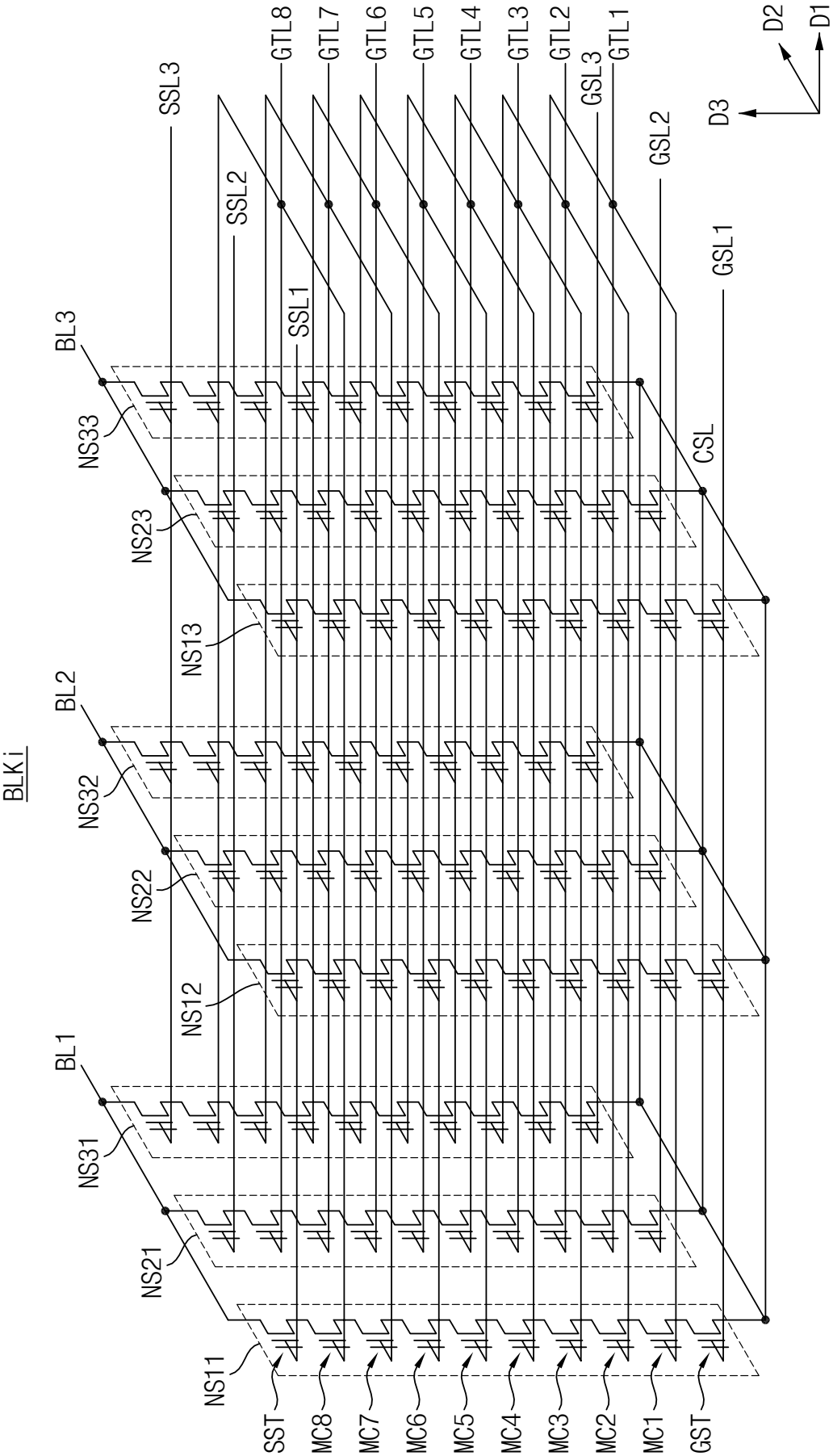

BLKi
BL1
BL2
BL3
NS11
NS21
NS31
NS12
NS22
NS32
NS13
NS23
NS33
SST
MC8
MC7
MC6
MC5
MC4
MC3
MC2
MC1
GST
SSL3
SSL2
SSL1
GTL8
GTL7
GTL6
GTL5
GTL4
GTL3
GTL2
GTL1
GSL3
GSL2
GSL1
CSL
D3
D2
D1

FIG. 10

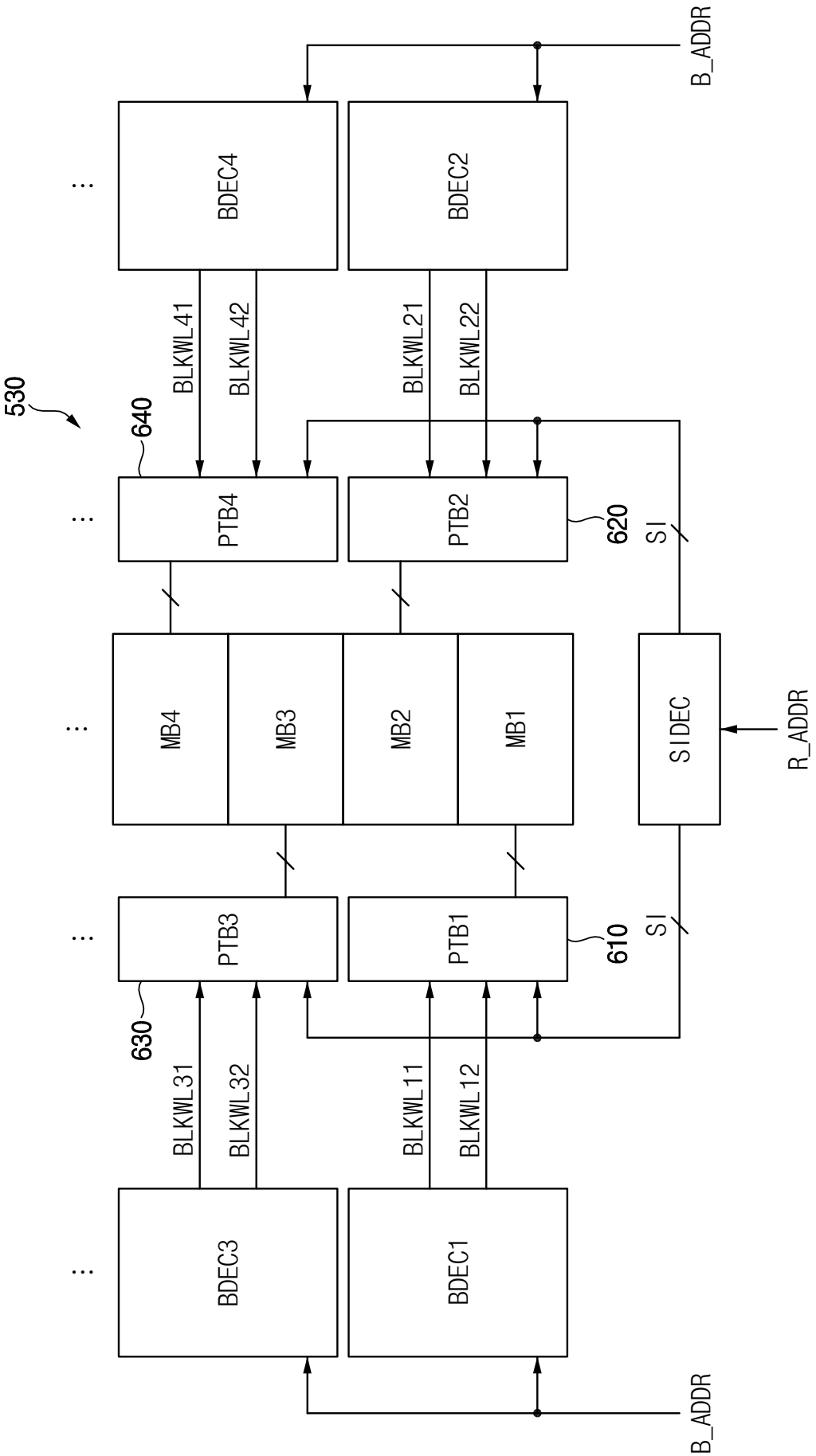

530
640
630
620
610
B_ADDR
BDEC4
BDEC2
BLKWL41
BLKWL42
BLKWL21
BLKWL22
PTB4
PTB2
SI
MB4
MB3
MB2
MB1
SIDEC
R_ADDR
PTB3
PTB1
SI
BLKWL31
BLKWL32
BLKWL11
BLKWL12
BDEC3
BDEC1
B_ADDR

FIG. 11

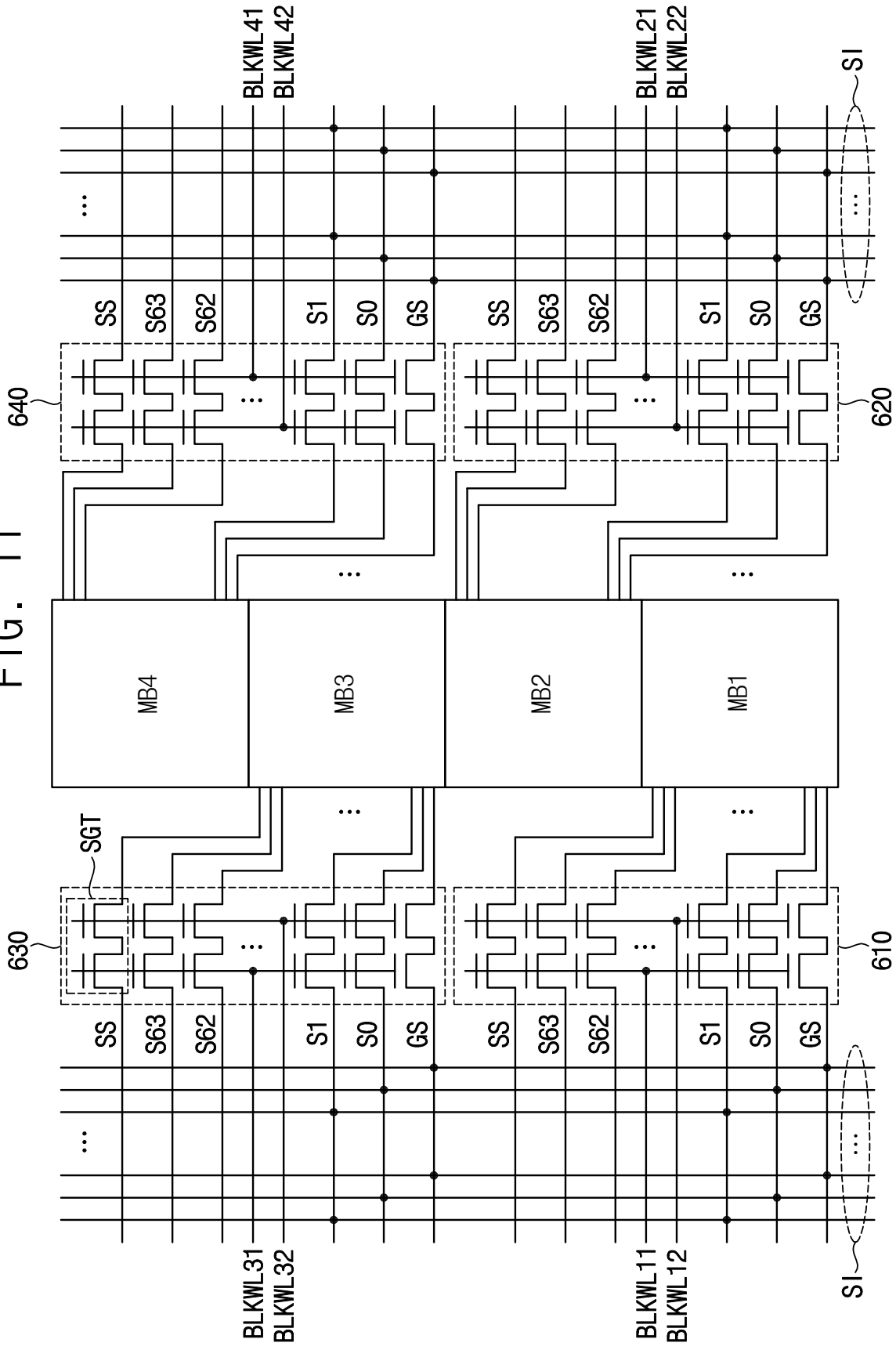

BLKWL41
BLKWL42
BLKWL21
BLKWL22
SI
640
620
SS
S63
S62
S1
S0
GS
MB4
MB3
MB2
MB1
SGT
630
610
BLKWL31
BLKWL32
BLKWL11
BLKWL12
SI

FIG. 12A

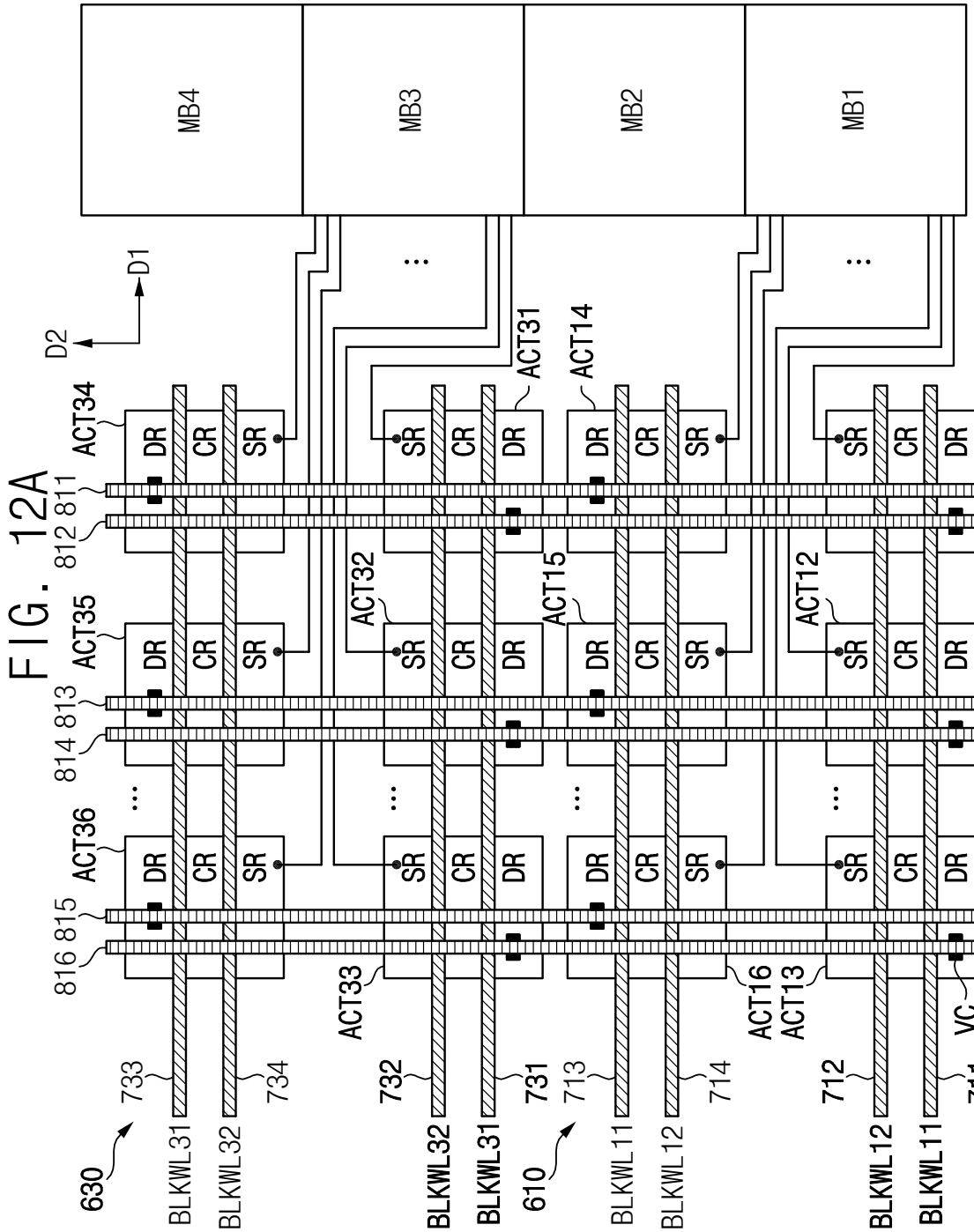

MB4
MB3
MB2
MB1
D1
D2
ACT34
ACT35
ACT36
ACT31
ACT14
ACT11
ACT32
ACT15
ACT12
ACT33
ACT16
ACT13
DR
CR
SR
811
812
813
814
815
816
GS
SS
S63
S0
S32
S31
VC
630
610
733
734
732
731
713
714
712
711
BLKWL31
BLKWL32
BLKWL32
BLKWL31
BLKWL11
BLKWL12
BLKWL12
BLKWL11

FIG. 12B

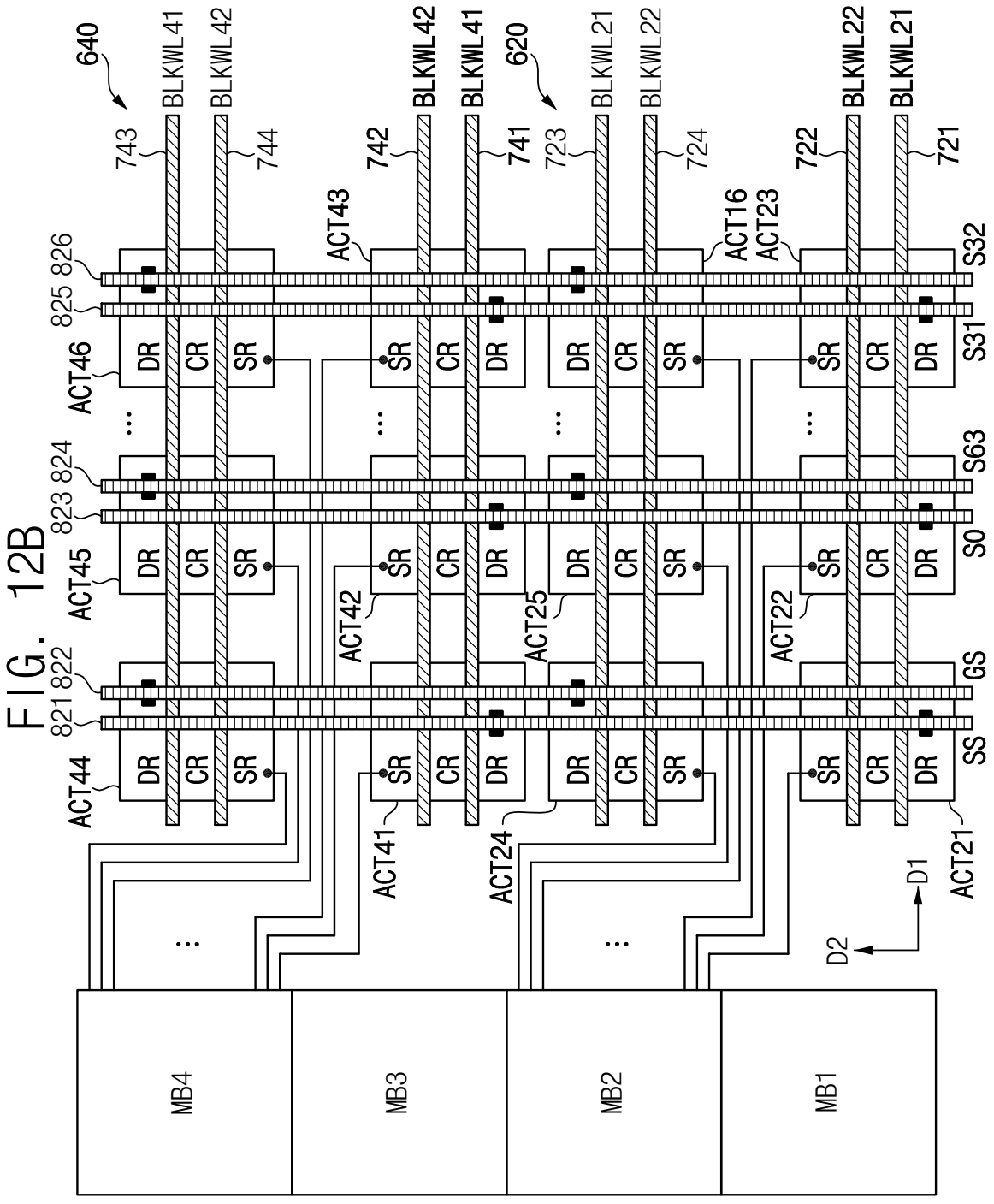

640
620
BLKWL41
BLKWL42
BLKWL21
BLKWL22
743
744
742
741
723
724
722
721
ACT43
ACT16
ACT23
ACT46
ACT45
ACT44
ACT42
ACT25
ACT22
ACT41
ACT24
ACT21
DR
CR
SR
821
822
823
824
825
826
GS
SS
S0
S63
S31
S32
MB4
MB3
MB2
MB1
D1
D2

FIG. 13A

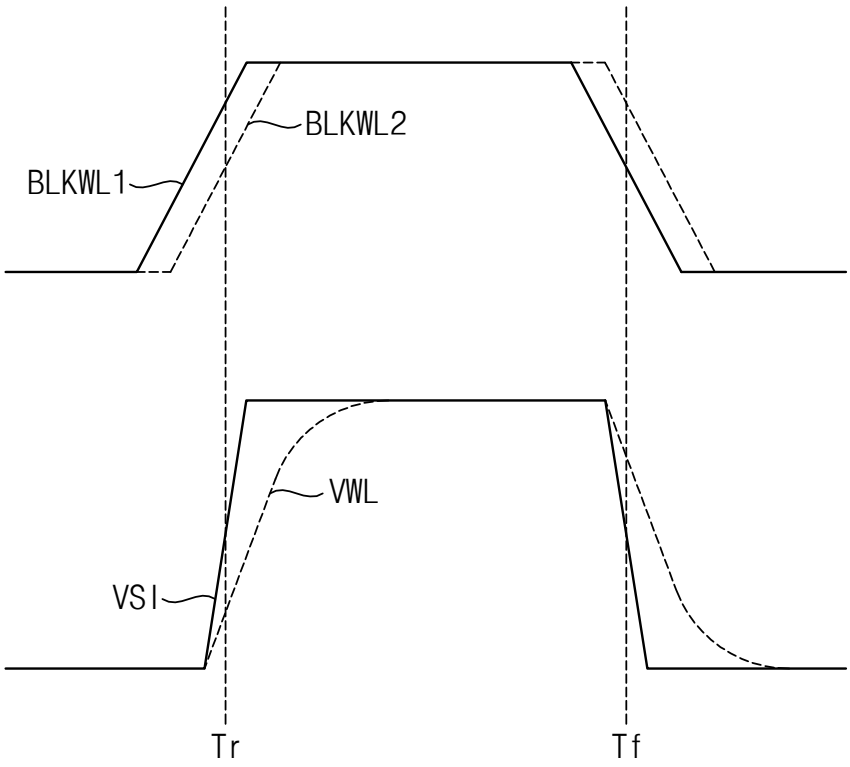


FIG. 13B

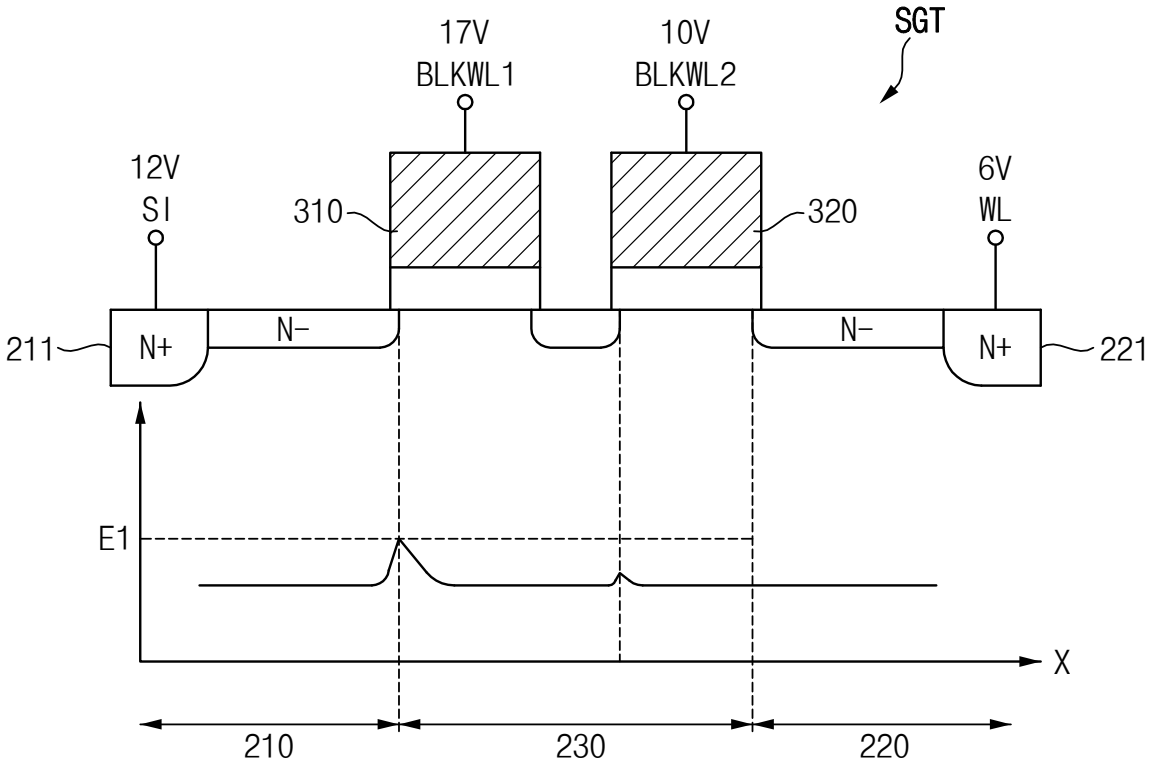


FIG. 13C

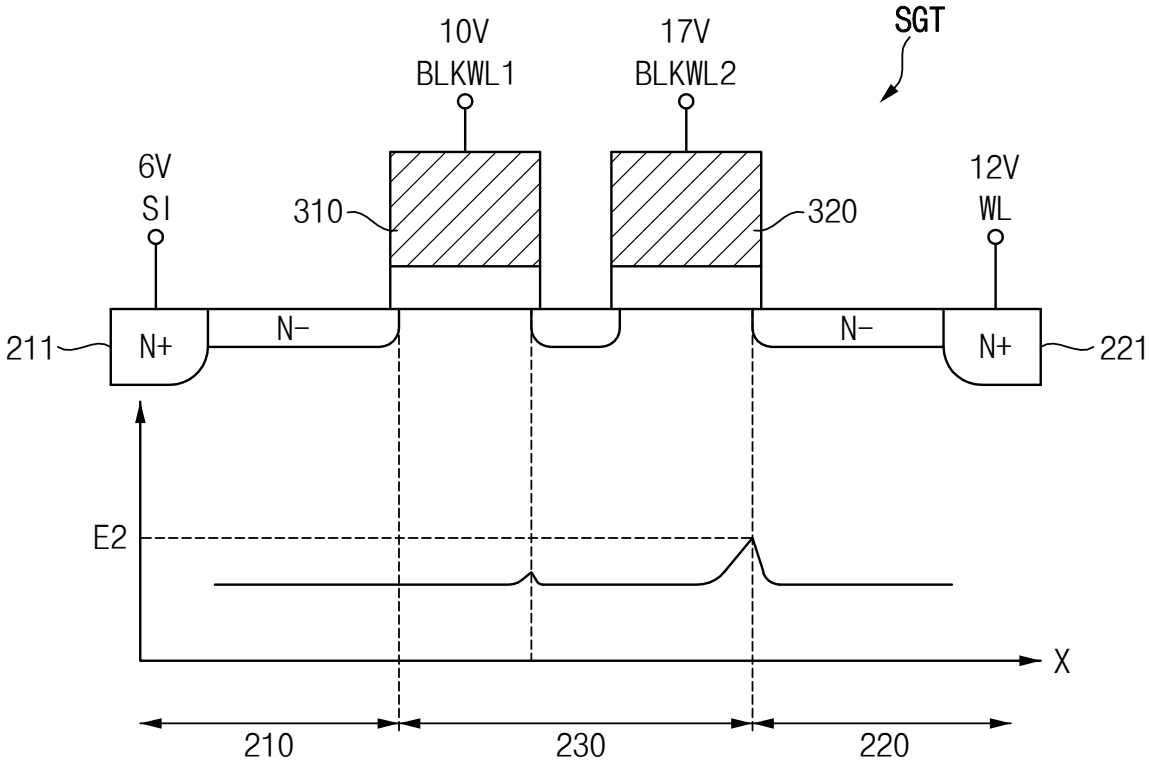


FIG. 13D

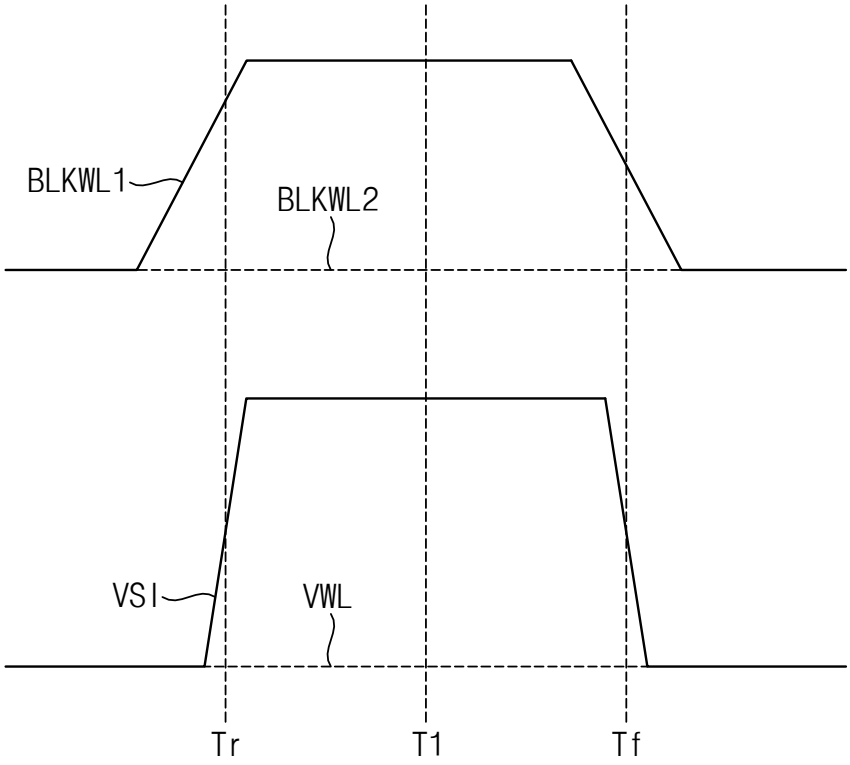


FIG. 13E

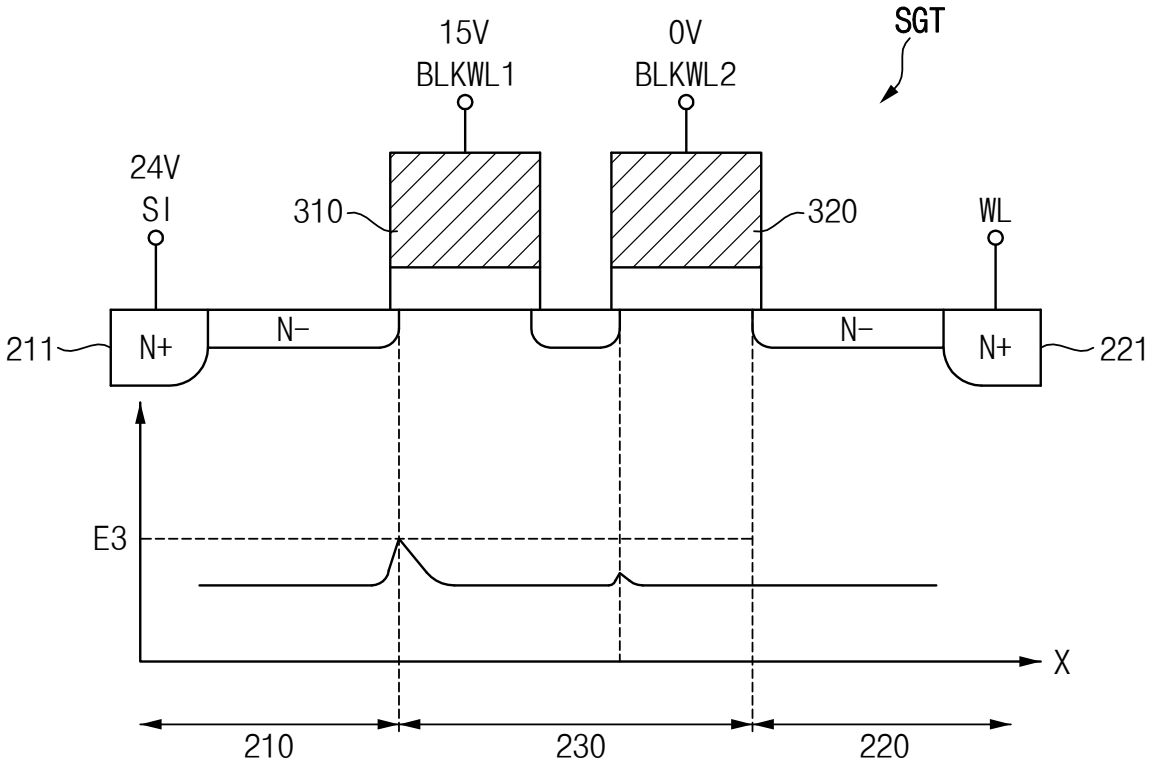


FIG. 14A

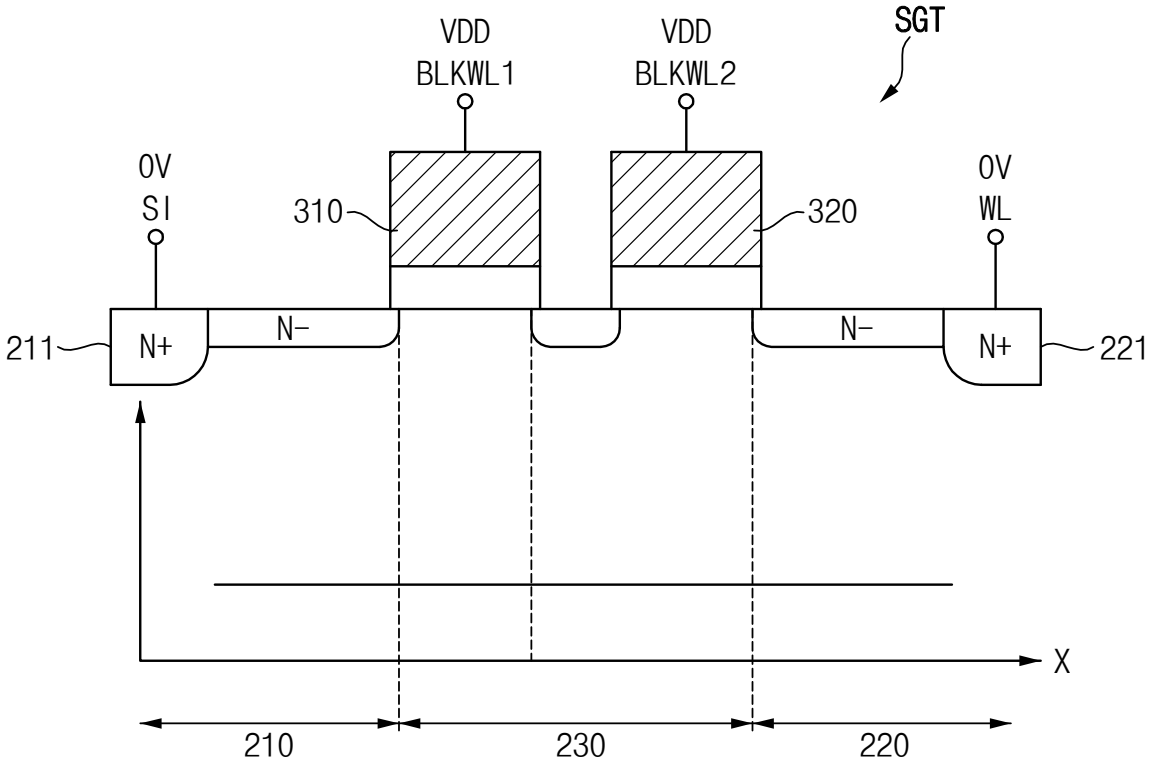


FIG. 14B

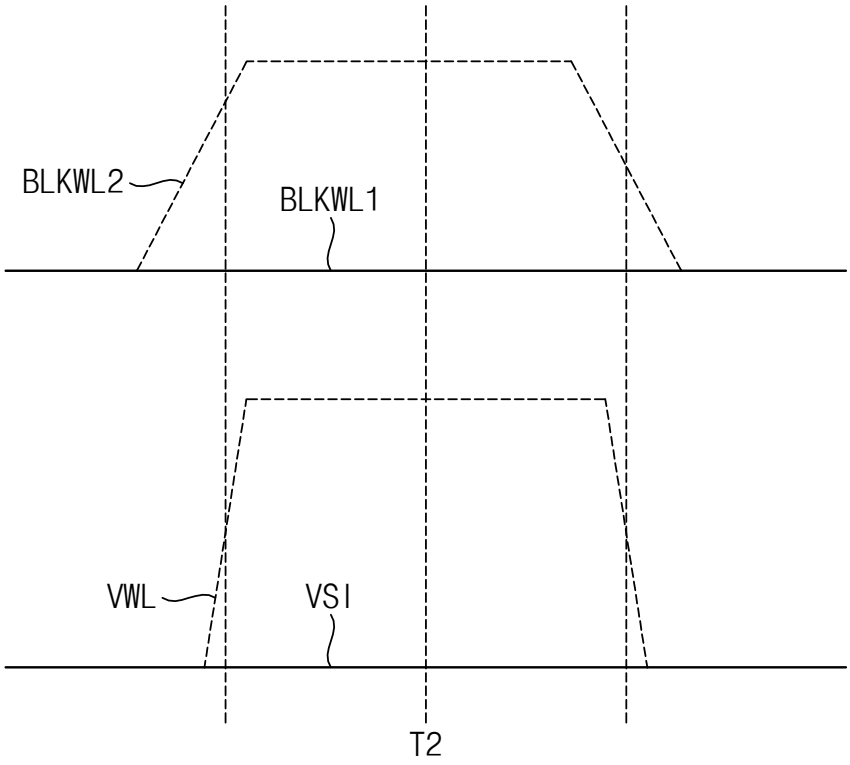


FIG. 14C

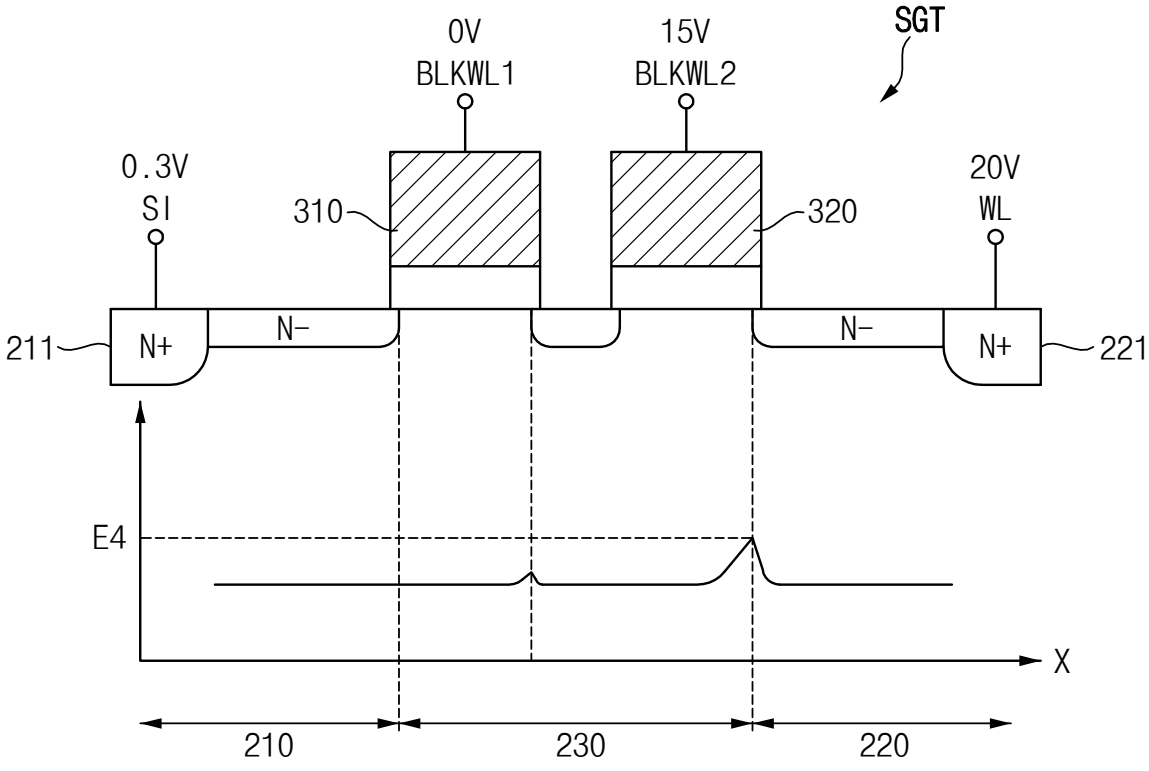


FIG. 15

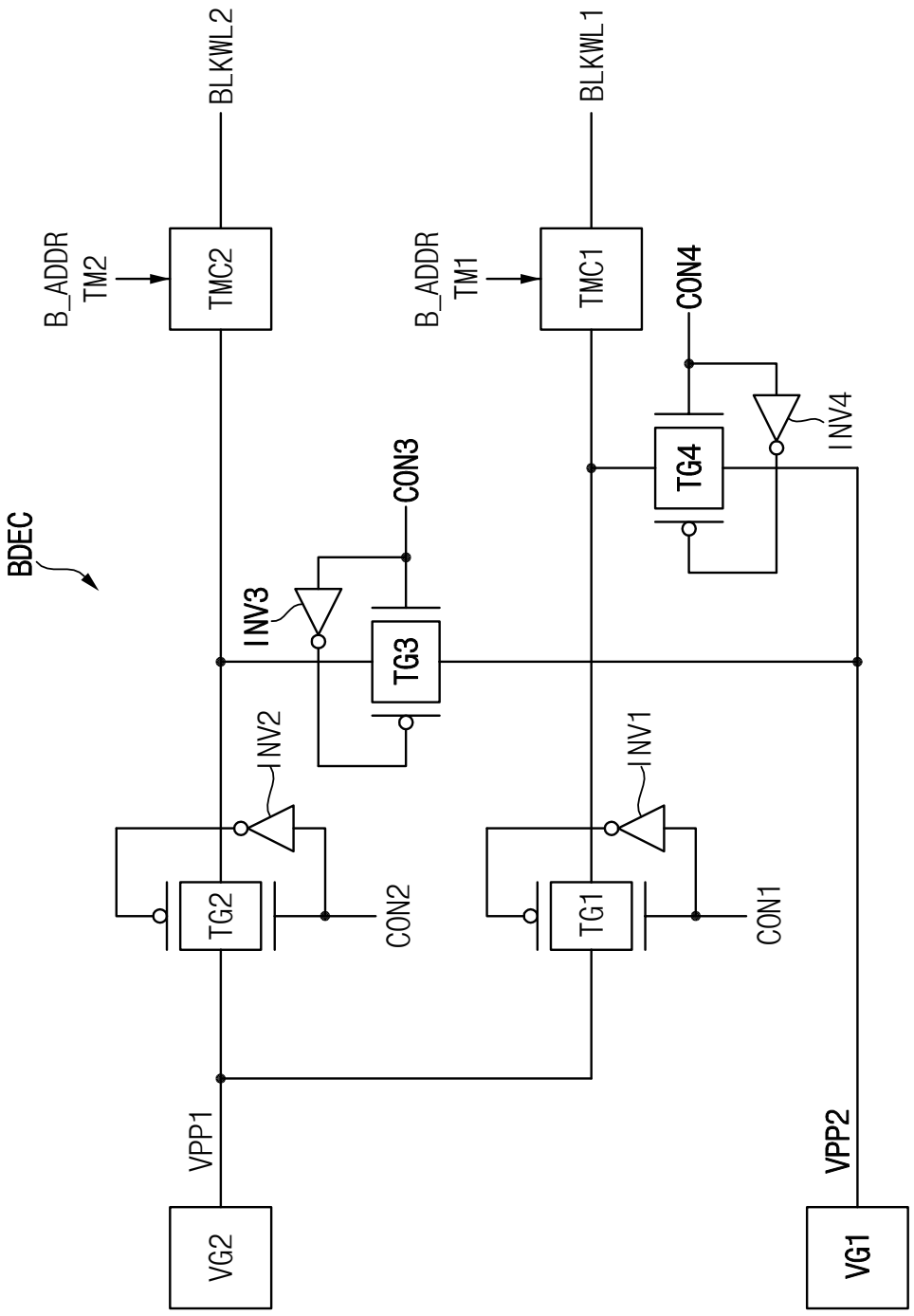

BDEC
B_ADDR
TM2
TMC2
BLKWL2
B_ADDR
TM1
TMC1
BLKWL1
CON4
INV4
TG4
CON3
INV3
TG3
INV2
INV1
TG2
CON2
TG1
CON1
VPP1
VPP2
VG2
VG1

FIG. 16

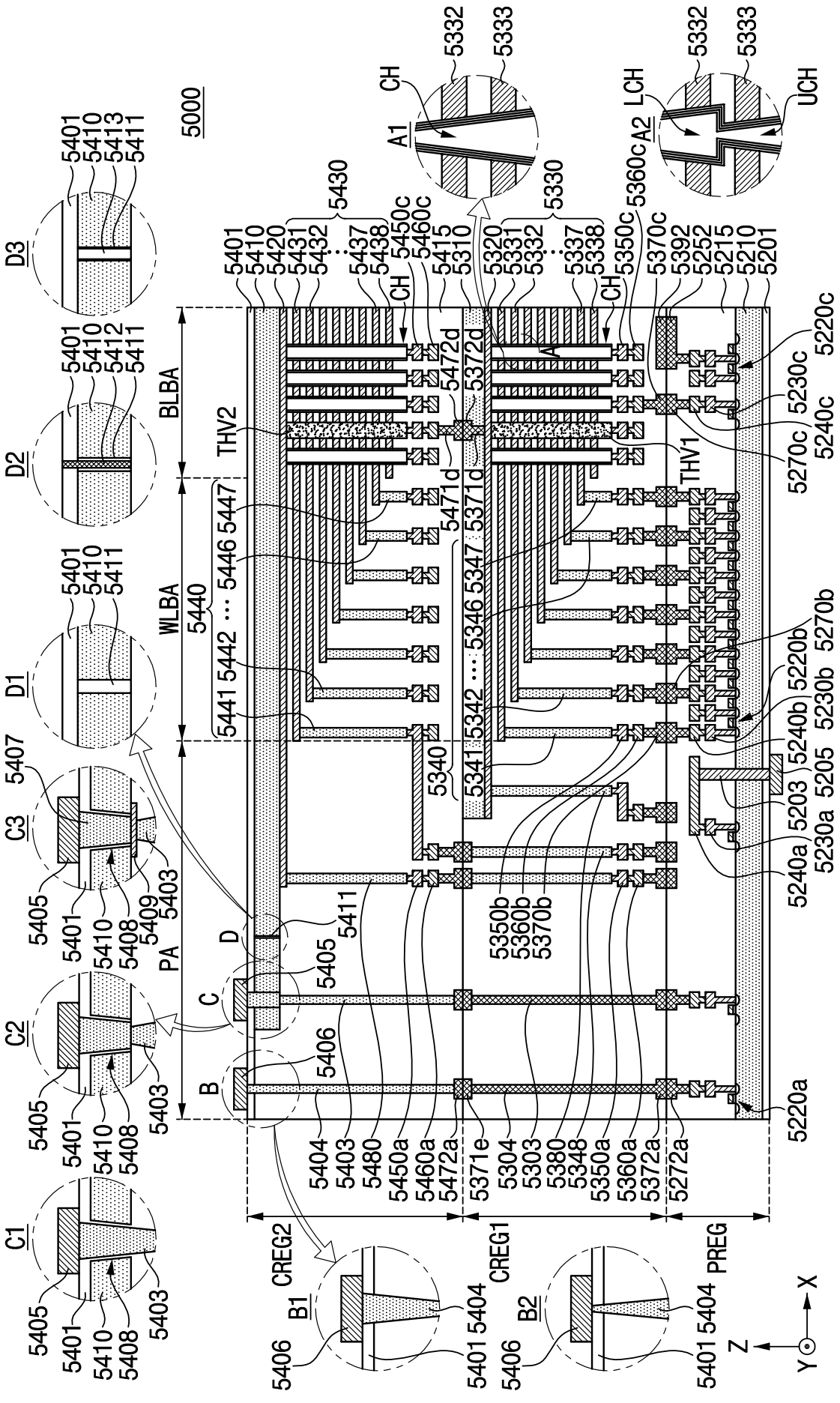

5000
BLBA
WLBA
PA
THV2
THV1
CREG2
CREG1
PREG
A1
A2
CH
LCH
UCH
D1
D2
D3
C1
C2
C3
B1
B2
X
Y
Z

FIG. 17

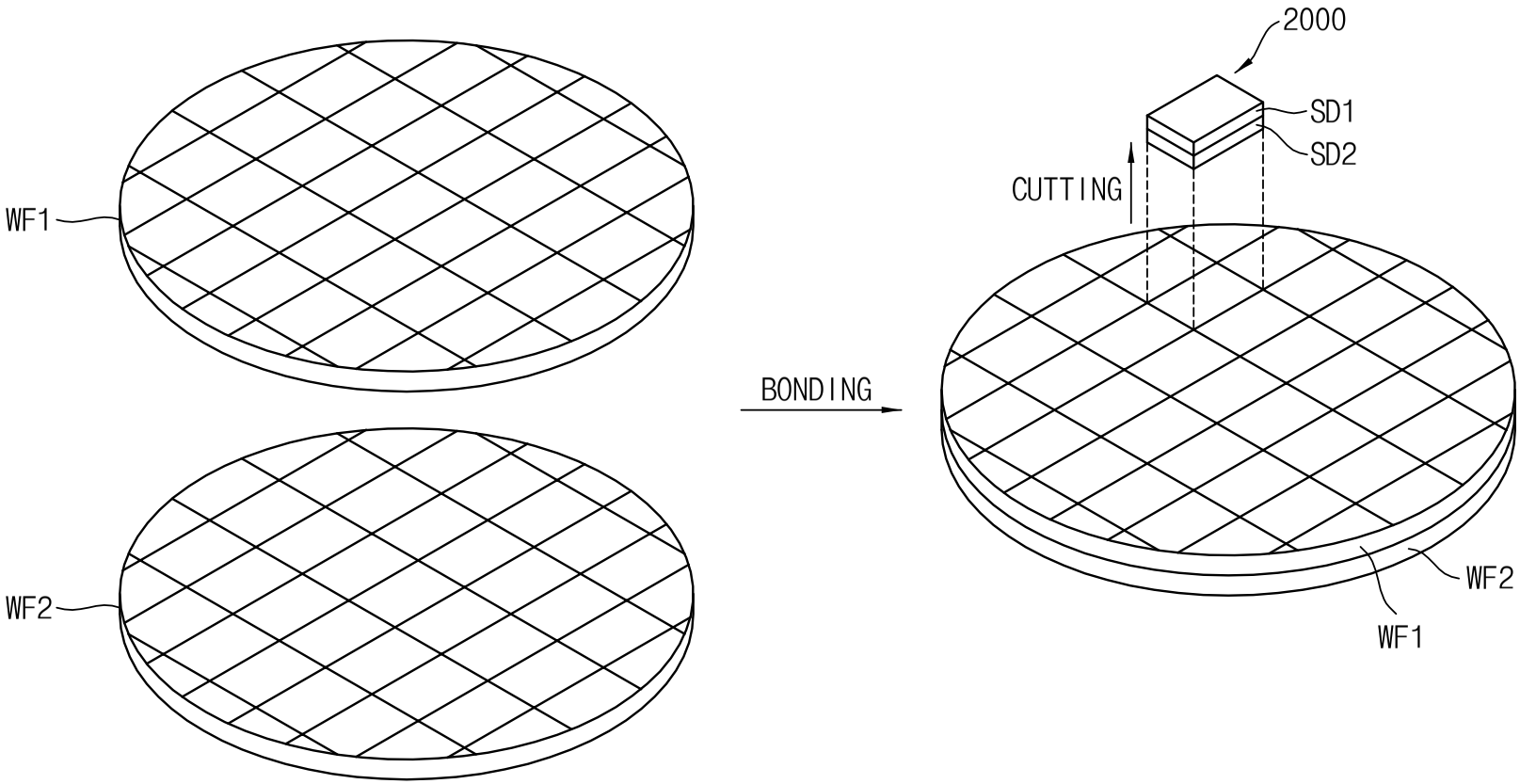
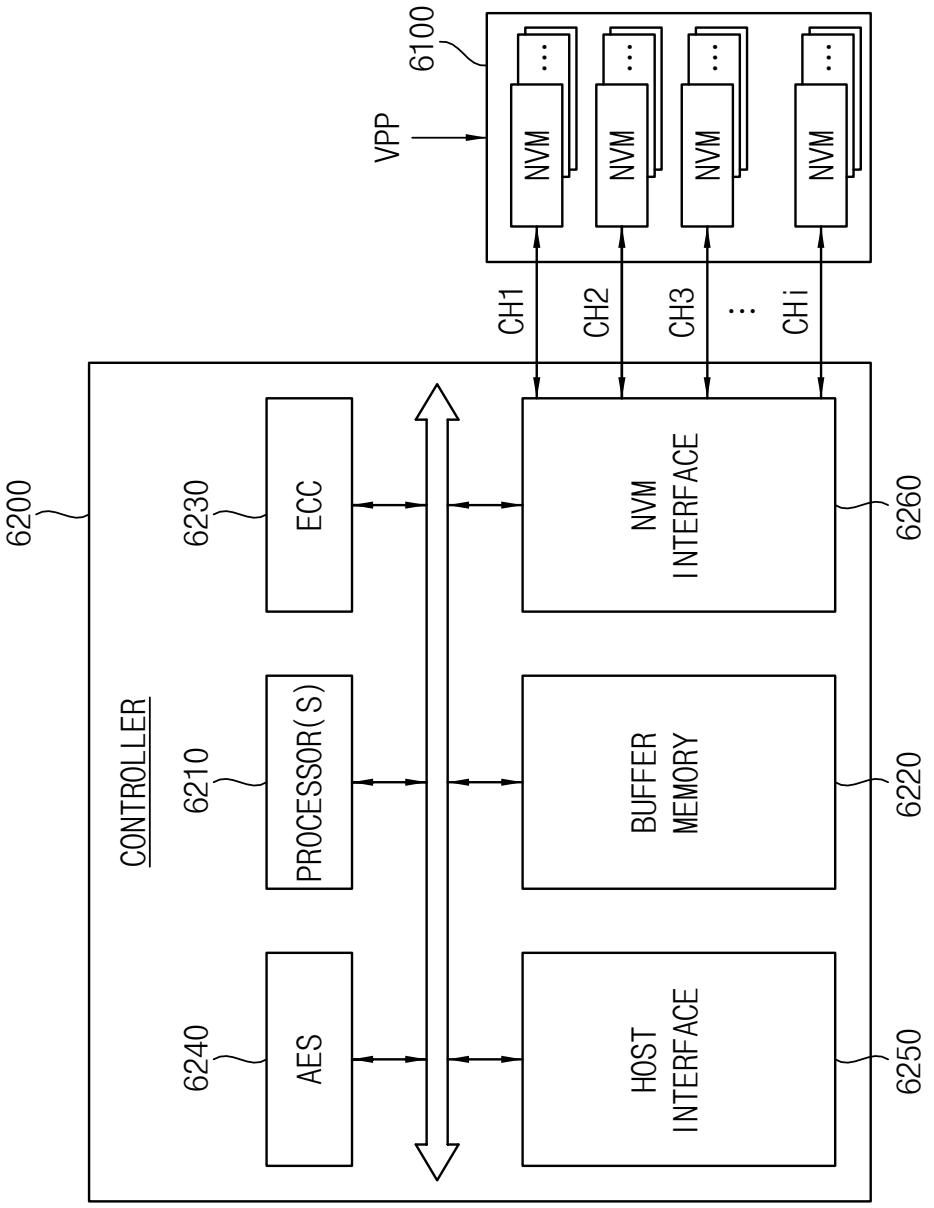


FIG. 18


6000
6100
VPP
NVM
NVM
NVM
NVM
CH1
CH2
CH3
CH i
6200
CONTROLLER
6230
ECC
6210
PROCESSOR(S)
6240
AES
NVM INTERFACE
6260
BUFFER MEMORY
6220
HOST INTERFACE
6250