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RECONFIGURABLE PROGRAMMABLE DIGITAL FILTER
ARCHITECTURE

Modes of communicating information between a transmitter and one or more receivers may be accomplished by terrestrial broadcast, by satellite, and/or by cable. Such communicated information includes analog NTSC television signals, digital HDTV television signals and digital mobile telephone signals, by way of examples. The received signal may be distorted with respect to the transmitted signal due to multipath effects or other signal transmission effects. As known, such distortion may be minimized at the receiver by means of a suitable equalization filter thereat. In particular, so-called deghosting filters may be used as a multipath equalization filter to minimize multipath distortion displayed by a television receiver. One example of such deghosting filter, which is implemented in digital form, is disclosed in U.S. patent 5,065,242, which issued to Dieterich et al. on November 11, 1991.

The specific filter characteristics of a deghosting filter or other type of equalization filter of each individual television set, mobile telephone, or other type of communication receiver incorporating such a filter preferably are tailored to that particular receiver in order to be effective in minimizing the distortion of the signal received thereby. However, television sets and mobile telephones are mass-produced items in which cost also must be minimized. What is needed is a single integrated circuit (chip) architecture which permits one or more of such chips to efficiently and economically implement a reconfigurable programmable digital filter having characteristics of a deghosting filter or any other type of equalization filter that may be separately tailored for use in each individual receiver of any type of communication equipment.

The invention is directed to filter architecture which may be implemented as an integrated circuit. The architecture comprises means including multiplexer means combined with first and second input-weighted digital filter units each of which has a given number of multiplier-coefficient taps that provides a reconfigurable programmable digital filter suitable for use as a deghosting filter. The first and second digital filter units can be



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configured with this combination for operation either as a single complex digital filter unit with the given number of complex multiplier coefficients for a complex sampled input signal or, alternatively, at least one of the two digital filter units can be

5 configured with this combination for operation as a separate real digital filter unit with twice the given number of real multiplier coefficients for a real sampled input signal.

BRIEF DESCRIPTION OF THE DRAWING

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FIGURE 1 diagrammatically illustrates an overview of the architecture of an $(n+1)$ section VLSI chip suitable for efficiently implementing a reconfigurable programmable deghosting filter having n filter sections, and FIGURE 1a diagrammatically

15 illustrates an arrangement employing a plurality of such chips;

FIGURE 2 diagrammatically illustrates a first configuration of a pair of real-coefficient FIR filter units employed in each of the n filter sections of FIGURE 1, and FIGURE 2a is a timing diagram indicative of the operation thereof;

20 FIGURE 3 diagrammatically illustrates a second configuration of the pair of real-coefficient FIR filter units employed in each of the n filter sections of FIGURE 1, and FIGURE 3a is a timing diagram indicative of the operation thereof; and

25 FIGURES 4a, 4b and 5 to 12 diagrammatically show in detail illustrative examples of various types of filters suitable for use as deghosting and/or equalization filters, each of which may be implemented on a VLSI chip by a different programmable configuration of a single global section and three identically-structured filter sections.

30 A digital channel equalization and deghosting filter for either HDTV or NTSC signals must adapt to any combination of preghost, postghost, and other linear channel impairments in a channel that is then being received. These filter types are needed to accomplish attenuation of post ghosts, preghosts, and channel

35 equalization using a variety of algorithms. Channel equalization is accomplished by dense Finite Impulse Response (FIR) filters; postghost cancellation is accomplished by sparse Infinite Impulse Response (IIR) filters, and pre-ghost attenuation is accomplished



by sparse FIR filters. Further, while the values of digitized NTSC signals are defined by only real values and require only real-valued digital filters, digitized HDTV signals are complex and require complex-valued digital filters. The present invention is directed to a versatile filter architecture that enables various combinations of the above-described filter modes to be configured on a single VLSI chip without physically rewiring the chip. This not only provides a low cost single filter integrated circuit (IC) that allows for selection of the optimal filter topology for a given input signal.

Referring now to FIGURE 1, there is diagrammatically shown a VLSI chip 100 area divided into $(n+1)$ subareas consisting of a single IIR input and global section subarea and filter section (FS) subareas 1 through n , in which all filter sections have identical architectures. The data input bus provides input data to the transposed architecture filter in a FIR configuration. The IIR output bus provides the output of an IIR adder to the input of a transposed architecture filter for IIR filter implementations. The bus is indicated as bidirectional since a configurable multichip system may have the IIR adder located on any of the n chips. In principle, n could have a value as small as one (i.e., VLSI chip 100 could comprise only a single filter section). However, in practice, the value of n is normally larger than one (VLSI chip 100 normally comprises a given plurality of filter sections). In an actually designed VLSI chip, the value of n is five. However, for illustrative purposes in describing the present invention, it is assumed in the examples shown in FIGURES 4a, 4b and 5 to 12 that the value of n is only three.

Each of the n filter sections of chip 100 includes a pair of input-weighted filter units 102T and 102B that are shown in FIGURE 1. In addition, each of these n filter sections comprises other structure including input multiplexers, routing multiplexers registers, and bulk delay means that are not shown in FIGURE 1 but are shown and described in detail below in connection with FIGURES 2, 2a, 3, 3a, 4a, 4b and 5 to 12. The IIR input and global section of chip 100, is shown and described in detail below in connection with FIGURES 4a, 4b and 5 to 12, includes routing multiplexers and other structure (a) for selectively



interconnecting the n filter sections, (b) for selectively operating none, part or all of the n filter sections as FIR filters and/or operating none, part or all of the n filter sections as IIR filters, and (c) for selectively controlling the filter section output which is forwarded to the cascade output of chip 100.

A single chip 100 is all that is needed for the case of a deghosting and/or equalization filter requiring n or fewer filter sections. In the case of a deghosting and/or equalization filter requiring more than n filter sections, a given plurality of chips 100-1 to 100- m may be cascaded, as shown in FIGURE 1a. In this case the cascade output of each chip except that of the last chip 100- m is forwarded to the cascade input of each chip except that of first chip 100-1.

15 Complex and real configurations of filter units 102T and 102B:

The pair of filter units 102T and 102B may be alternatively configured to operate as a single complex-coefficient input-weighted digital filter having a given number of taps for a complex input signal, as shown in FIGURE 2, or to operate as two independent real-coefficient input-weighted digital filters having twice the given number of taps for two independent real input signals, as shown in FIGURE 3, or to operate as four independent real-coefficient input-weighted digital filters each having the given number of taps for four independent real input signals.

Reference is made to FIGURE 2, which shows top real-coefficient FIR filter unit 102T and bottom real-coefficient FIR filter unit 102B associated with an input multiplexer 200, and to FIGURE 2a, which is a timing diagram indicative of the operation of the FIGURE 2 structure. Each of filter units 102T and 102B is a multitap input-weighted filter having two multiplier-accumulator registers associated with each tap, as indicated in FIGURE 2. Input signals are provided from a source of television signal video component for example, and output signals are provided to video signal processing circuits in a television signal receiver for example. Successive Real (R) and Imaginary (I) input data samples are respectively applied to first and second inputs of multiplexer 200 at a given sample rate that is one-half the filter clock (Clk) rate. Multiplexer 200, in response to Clk applied to the



switch (S) input thereof, forwards an R input data sample to the inputs of both filter units 102T and 102B during the first Clk period of each successive sample period (designated SP in FIGURE 2a) and forwards an I input data sample to the inputs of both filter units 102T and 102B during the second Clk period of each successive sample period. Although not specifically shown in FIGURE 2, during the first Clk period, an appropriately-valued multiplier coefficient R is applied to the first of the two multiplier-accumulator registers associated with each tap of filter unit 102T and each tap of filter unit 102B. During the second Clk period, the negative of an appropriately-valued multiplier coefficient -I is applied to the second of the two multiplier-accumulator registers associated with each tap of filter unit 102T and an appropriately-valued multiplier coefficient R is applied to the second of the two multiplier-accumulator registers associated with each tap of filter unit 102B.

The value of a complex multiplier coefficient c involves both a real value R and an imaginary value I and a complex input sample i also involves both a real value R and an imaginary value I. Therefore, the product $(R+jI)_c(R+jI)_i$ of the complex coefficient c times the complex input sample i is equal to $(RcRi - IcIi) + j(RcIi + IcRi)$. It usually requires four digital filter units to perform this involved complex product computation. However, filter units 102T and 102B, by employing time-multiplexed coefficients and two multiplier-accumulator registers between taps, permits this involved complex product computation to be performed with only the two filter units 102T and 102B.

In particular, the sample output from filter 102T during the first Clk period of each sample period is RR and during the second Clk period of each sample period is -II. Together, they represent the real portion of each complex output sample, shown as EE in the FIGURE 2a timing diagram. Similarly, the sample output from filter 102B during the first Clk period of each sample period is RI and during the second Clk period of each sample period is IR. Together, they represent the imaginary portion of each complex output sample, shown as FF in the FIGURE 2a timing diagram.

In a designed chip, each of filter units 102T and 102B comprises only three taps. For this reason, a whole filter usually



comprises a plurality of cascaded filter units on a single chip or, in some cases, on a plurality of cascaded chips. The real cascade output of a corresponding filter unit 102T of a preceding filter section, designated E, can be forwarded to the sumin input of the filter unit 102T of FIGURE 2. In a similar manner the imaginary cascade output of a corresponding filter unit 102B of a preceding filter section, designated F, can be forwarded to the sumin input of the filter unit 102B of FIGURE 2.

There are two alternative ways of handling the sumin input sample value forwarded to an input-weighted filter unit 102T or 102B. A first way, not shown in FIGURE 2, is to handle the sumin value in the same manner as such sample values are handled internally within an input-weighted filter unit 102T or 102B of any filter section. More specifically, each of the multiplexed first and second multiplier-accumulator registers associated with each tap of filter unit 102T or 102B multiplies the current input sample value by a coefficient value associated therewith, then adds this product value to the accumulated sum value from the corresponding multiplexed register forwarded thereto from the preceding tap after a delay of a specified number of Clk periods. In this first way, The sumin input E or F to a filter unit of a given filter section from the multiplexed output EE or FF of a corresponding filter unit of a preceding filter section is directly forwarded to the given filter section in multiplexed form. In this case, the first and second Clk period sample values of this sumin input is respectively added to the sum value of the first multiplier-accumulator register and to the sum value of the second multiplier-accumulator register associated with the first tap of the filter unit of the given filter section. In the second way, shown in FIGURE 2, the multiplexed outputs EE and FF are demultiplexed before being forwarded to the E and F sumin filter-unit inputs of a following filter section. This is accomplished by delaying The EE and FF outputs by a Clk period in registers 202T and 202B and then adding the delayed EE and FF outputs to the undelayed EE and FF outputs in summers 204T and 204B. In this second way, the Real Out output from summer 204T and the Imag Out output from summer 204B (designated Out in FIGURE 2a) is forwarded only during a selected valid one of the first and second



Clk periods of each sample period SP (designated V portions of Out in FIGURE 2a), and is not forwarded during the unselected invalid one of the first and second Clk periods of each sample period SP (designated X portions of Out in FIGURE 2a). The selected valid one of the first and second Clk periods of each sample period SP for summers 204T and 204B need not be the same as one another.

Reference is now made to FIGURE 3, which shows the same top real-coefficient FIR filter unit 102T and bottom real-coefficient FIR filter unit 102B that are multiplex-operated as a single complex-coefficient input-weighted digital filter having a given number of taps in above-described FIGURE 2, reconfigured to multiplex-operate as two independent real-coefficient input-weighted digital filters having twice this given number of taps. FIGURE 3a is a timing diagram indicative of the operation of the FIGURE 3 structure.

FIGURE 3 shows top filter unit 102T associated with input multiplexer 300T and bottom real-coefficient FIR filter unit 102B associated with input multiplexer 300B. As shown in FIGURE 2 and indicated in FIGURE 2a, multiplexers 300T and 300B, each of which operates in a manner intrinsically similar to that described above in connection with multiplexer 200, respectively feed back the Out output of filter units 102T and 102B to the sumin input thereof during the first Clk period of each sample period SP, and respectively forward the cascade output of a corresponding filter unit of a preceding filter section to the sumin input of filter units 102T and 102B during the second Clk period of each sample period SP. Each of the filter units 102T and 102B of FIGURE 3, which derives a GG output, operates as an input-weighted filter having its given number of real coefficients during a first pass therethrough of each of successive input samples that takes place during the first Clk periods of the successive sample periods SP (which successive samples of the GG output during the first Clk periods are designated P1 in FIGURE 3a). Each of these successive samples P1 of the GG output of respective filter units 102T and 102B, after being delayed by a Clk period by respective registers 302T and 302B, is fed back for a second pass through filter units 102T and 102B that takes place during the second Clk periods of the successive sample periods SP (which successive samples of the



GG output during the second Clk periods are designated P2 in FIGURE 3a). Filter units 102T and 102B of FIGURE 3, during the second pass, again operate as an input-weighted filter having its given number of real coefficients during the second pass

5 therethrough of each of the successive delayed P1 samples. Therefore, with respect to the successive input samples, each of respective filter units 102T and 102B operates as an input-weighted filter having twice the given number of real coefficients to derive the successive P2 samples. The successive delayed P2
10 samples at the Out output of each of respective filter units 102T and 102B occurring during the first Clk periods of successive sample periods constitutes the valid V output and those occurring during the first Clk periods of successive sample periods constitutes the invalid X output, as indicated in FIGURE 3a.

15 It is obvious that multiplex techniques similar to those employed in the FIGURE 3 configuration could, without using feedback, configure filter units 102T and 102B to operate as up to four independent real FIR filters each with its own given number of real coefficients. Alternatively, using feedback, filter units 102T
20 and 102B can be configured to forward the output samples of one of these two filter units as a cascade input to the other of these two filter units, thereby operating them as a single real FIR filter with four times the given number of real coefficients of each of them.

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Examples of reconfigurable programmable filter chip architecture:

The filter clock employed by the designed VLSI chip embodying the reconfigurable programmable digital filter architecture of the present invention is 28.636MHz and the input
30 data sample clock is 14.318MHZ (i.e., one half the rate of the filter clock). The programming of the filter is determined by a software-controlled CPU. As stated in the above "overview", the designed VLSI chip comprises six sections comprising a single IIR input and global section and five filter sections, all of which filter sections
35 have identical architectures. Because of the large amount of structure included in each of these sections, it is necessary in FIGURES 4a, 4b and 5 to 12 to abbreviate the designations of each structural item and to limit the illustrative examples of



reconfigurable filter chip architecture shown in in FIGURES 4a, 4b and 5 to 12 to only three filter sections in order to fit all this structure within available drawing area. Nomenclature for this VLSI chip is derived from its use in a complex mode. Real filter sections and associated hardware relate to filter sections 102T and associated hardware in the description, while imaginary filter sections relate to filter sections 102B. The following is a list of the abbreviated designations employed in FIGURES 4a, 4b and 5 to 12:

10 1. Filter-section abbreviated designations:

FIR Filter--Multiplexed FIR filter units similar to those shown in FIGURES 2 and 3. These input-weighted filters contain inter-tap programmable delays of from 1 to 4 sample periods, and they include multiplexed coefficients. "Input" connects to the coefficient multipliers, "sumin" adds in to the product of the first coefficient multiplier, and "sumout" is the output of the last adder, delayed by a clock period equal to one half a sample period.

15 RB[4..1], IB[4..1]--Real and Imaginary Input Multiplexer Control. There are four inputs to each input multiplexer. There are four control bits to each multiplexer. On each of the first and second clock periods T0 and T1 of a sample period, different data are presented to the control of the input multiplexer. This allows any input to be selected from the four input selections during T0, and any input to be selected during T1. This is an easy way to obtain the required flexibility to cascade devices and support all required modes of operation. Each input multiplexer control includes a first latch for storing two control bits written into it by a CPU control line which define the effective one of the four inputs during any clock period T0, and a second latch for storing two control bits written into it by the CPU control line which define the effective one of the four inputs during any clock period T1.

30 35 RIReg, IIReg--Real and Imaginary Input Data Registers. This is a pipeline delay, as well as a buffer for data into the filter inputs. This is programmable to sample at clock rate for complex modes, and at sample rate for real mode.



RM1, IM1--Real and Imaginary Real/complex mode multiplexers. Real mode is set to input 0, Complex mode is set to input 1.

5 RM2, IM2--Real and Imaginary Output Multiplexers for selecting the data output source from the following 4 options:

Option	Real Mode Function	Complex Mode Function
0	Inter Section delay 2	Inter Section delay 2
1	Not Useful	Inter Section delay 1
2	Inter Section delay 3-155	Inter Section delay 3-155
3	Inter Section delay 1	Not Useful

ROReg, IOReg--Real and Imaginary Output Data Registers.

T0--First clock period of a sample period.

T1--Second clock period of a sample period.

10 Tlena--Enable in T1. This is a register operating at sample rate, enabled only during the T1 clock periods. Data will transition only on the sample period transitions. The bulk delay operates at sample period rate, not clock period rate. This forms the third delay added to the bulk delay range of 0 to 152 to get the range from 3 to 155.

15 z-1--Delay of clock period where it stands alone in FIGURES 4a, 4b and 5 to 12. Otherwise, it is adjustable to be either one clock period for complex, one full sample period for real (RIReg, IIRcg), or one full sample period always (Tlena), or one full sample period enabled in T1 for real, T0 for complex (ROReg, IOReg). Its only consistent definition is that it is implemented with only a single register stage.

20 z-3kr, z-3ki--Real and Imaginary programmable inter-tap delay. Used Only in real mode configurations. Range from 0 to 3 sample period delays.

25 z-RDEL, z-IDEL--Real and Imaginary Bulk Delay Registers. Programmable from 0 to 152 sample period delays.

2. IIR input and global section abbreviated designations:

30 ISC, QSC--In-phase Scaling Control and Quadrature Scaling Control. This multiplexer allows shifting of IIR feedback data to get additional precision when all IIR coefficients are less than 1, 1/2, or 1/8. In FIR only mode, it is



convenient to select a 0 as input. This multiplexer is statically controlled and resembles a switch.

5 M2--Quadrature (Imaginary) cascade source select. In conjunction with M5, any filter section or IIR adder output or zero can be cascaded to the sum input of the input filter section of the chip (filter section n in FIGURE 1 and filter section 3 in FIGURES 4a, 4b and 5 to 12). Like RB and IB, this multiplexer can alternately select different inputs on each clock period cycle. This is required for some
10 complex mode configuration cascades.

M3--In-phase (Real) cascade source select. In conjunction with M4, any filter section or IIR adder output or zero can be cascaded to the sum input of the input filter section of the chip (filter section n in FIGURE 1 and filter section 3 in
15 FIGURES 4a, 4b and 5 to 12). Like RB and IB, this multiplexer can alternately select any input clock period cycle. This is required for some complex mode cascades.

M4--In-phase (Real) section select. Selects the output of any real (In-phase) half filter section or the real IIR adder
20 output to drive M3.

M5--Quadrature (Imaginary) section select. Selects the output of any imaginary (quadrature) half filter section or the imaginary IIR adder output to drive M2.

M6--In-phase (Real) output select. Selects the output of any real half filter section or the real IIR adder output to be
25 output from the Iout terminals.

M7--Quadrature (Imaginary) output select. Selects the output of any imaginary half filter section or the imaginary IIR adder output to be output from the Qout terminals.

30 M8--FIR Input Multiplexer. In FIR modes, input data comes from either the IIR filter output or the phase rotator output. Either way, it is routed through the IIR filter adder--the other IIR addend is set to 0 by ISC and QSC if the filter is pure FIR. In real mode, either adder can be
35 used as a data source. In complex modes, M8 multiplexes real and imaginary data at the clock period rate which is twice the sample period rate, thereby formatting the input data for the multiplexed filter sections.



TOena z-1--A register enabled in the T0 clock period of a sample period.

3. Chip system input and output abbreviated designations:

5 0 --The constant value of zero.

I1, I2, I3--Outputs of In-phase (real) filter sections 1, 2, 3.

Iout--In-phase filter output.

Iph--In-phase input to IIR adder, from phase rotator. Used as real input in real mode.

10 Iumin--In-phase Cascade Input. Used as real only cascade input in real mode configuration.

MIO--Multiplexed Filter I/O - Real/Imaginary multiplexed signal in complex mode, real signal in real mode. This is an output on the chip with the active IIR feedback adder. It is input on all other chips. MIOena enables the output capability.

15 MIOena--Enables the output capability of the MIO bus.

Q1, Q2, Q3--Outputs of Quadrature filter sections 1, 2, 3.

Qout--Quadrature Filter output.

20 Qph--Quadrature input to IIR adder, from phase rotator.

Qsumin--Quadrature Phase Cascade Input.

The identical chip architecture of the three filter sections and the single IIR input and global section shown in each of FIGURES 4a, 4b and 5 to 12 is selectively programmed to be reconfigured into a particular one of nine different filter configurations or, alternatively, to merely forward the cascade input to the chip with a certain amount of delay to the cascade output of the chip without any filtering taking place. A software-controlled CPU accomplishes this selective programming solely by (1) determining the input-output connection of each input multiplexer of each filter section during respective clock periods To and T1 of each sample period; (2) determining the input-output connection of each routing multiplexer RM1, IM1, RM2 and IM2 of each filter section; (3) determining the input-output connection of each routing multiplexer ISC, QSC, M2, M3, M4, M5, M6, M7 and M8 of the single IIR input and global section; and (4) controlling the respective digital values of the in-phase (real) Iph portion and the



quadrature-phase (imaginary) Q_{ph} portion of a complex phase-rotating coefficient.

As known, NTSC television signals are real signals, not complex signals. In this case, the three filter sections and the single IIR input and global section should be configured into a real (not complex) filter. The chip architecture configuration shown in FIGURE 4a is an example of a real IIR filter followed by a real FIR filter for the case in which the IIR filter uses fewer filter sections than the FIR filter. In FIGURE 4a, the FIR is constructed from all imaginary sections and the real half of section 3. Further, input data is fed into the real side of the IIR input adder by providing a complex phase-rotating coefficient value $1-2^{-10}+j0$ (where 2^{-10} is the closest value to 1 that can be expressed in $\pm$ binary form with 11 significant digits). The IIR output is fed back by the MIO bus, and the first section of the FIR filter is implemented by the imaginary (bottom) half of filter section 3. The output of the imaginary half of filter section 1 is fed back to the real sumin (top) of filter section 3. The FIR filter output is taken from the real output of filter section 3.

The chip architecture configuration shown in FIGURE 4b is an example of a real IIR filter followed by a real FIR filter for the case in which the IIR filter uses more filter sections than the FIR filter. FIGURE 4b defines a real IIR filter using the imaginary half of all filter sections and the real half of filter section 1. The FIR filter is composed of the real half of filter sections 1 and 2. The real input data is fed to the imaginary side of the IIR input adder by providing a complex phase-rotating coefficient value $0+j(1-2^{-10})$. As always, the IIR output is fed back by the MIO bus.

FIGURES 5-12 show other examples of configurations that are useful as deghosting and/or equalization filters for HDTV television currently being developed and/or NTSC television. These filters include real filters, complex filters and combinations thereof.

FIGURE 5 shows an example of a complex IIR filter configuration. In this configuration, the entire chip is programmed as a complex IIR filter. Sections 1 and 2 are shown with only a z^{-1} delay and section 3 is separated from section 2 by the bulk delay. The Isumin and Qsumin terminals are not used, except possibly



for cascading; input data arrives on I and Q input terminals of the VLSI chip (not shown), and the filter output is derived on Iout and Qout. RReg and IReg are all configured for clocking during both the T0 and T1 clock periods, and RReg and IReg are
5 configured for clocking only at the end of a T0 clock period.

FIGURE 6 shows an example of a configuration comprising a complex IIR filter with a complex FIR filter on one chip. In this configuration, filter sections 1 and 2 are in IIR filter mode, while section 3 is configured as a 3 tap FIR. Phase adjusted input data
10 arrives on Iph and Qph, and output data is derived on Iout and Qout, which receives their output from filter section 3. RReg and IReg are all configured for clocking during both T0 and T1 clock periods, and RReg and IReg are configured for clocking only at the end of T0 clock periods. Filter section 2 is separated from
15 filter section 1 by a z^{-1} delay of one sample period (i.e. e clock periods), while filter section 1 uses the bulk delay to get a total delay of 3 to 155 sample periods before being added to the input data. Note that a delay is incurred in recovering the complex output data of section 3. If section 3 were to cascade to the next
20 chip, the complex components (i.e., the four coefficient/data products RR, -II, RI, and IR) could be passed over the output busses. Since this example is a stand alone configuration, the real and imaginary filter outputs are computed before the output. This delay is simply signal latency.

FIGURE 7 shows an example of a configuration comprising a complex IIR filter followed by a real FIR filter processing the real part of a complex IIR output. In this configuration, filter sections 1 and 2 compute complex IIR, filter section 3 computes a 12 tap real FIR. The bulk delay RDEL from section 3 can be used to
30 separate the two six tap sections of real FIR in time. To capture only the real output data from the real filter, one must use the bulk delay path to the output terminals. If cascading, the input section would zero the intermediate tap information. RReg and IReg of section 3 are enabled only in the T1 clock period for real
35 only operation. RReg and IReg of section 3 are always enabled for real only operation. RReg and IReg of sections 1 and 2 are always enabled, while RReg and IReg in sections 1 and 2 are enabled only in T0. The imaginary output of the complex IIR filter



is available on the multiplexed output bus MIO and on the Qout terminals of the chip.

FIGURE 8 shows an example of a configuration comprising a complex IIR filter followed by a half complex FIR filter. In this configuration, filter section 1 computes an IIR filter, filter sections 2 and 3 compute a 12 tap half complex FIR filter. The 12 tap FIR filter is configured as a 9 tap equalizer, with a 3 tap pre-ghost attenuator separated from the equalizer by the bulk delay IDEL in filter section 3. Real output is on Iout. Imaginary IIR output available in multiplexed MIO bus and Qout terminals. The FIR filter sections are cascaded. When bulk delay is required, the real data times real coefficients sum and imaginary data times imaginary coefficients sums must be subtracted, and the complete real result is stored in the bulk delay. Direct cascades require transfer of the partial sums of real data times real coefficients, and imaginary data times imaginary coefficients in a multiplexed form (real times real in T0 clock periods and imaginary times imaginary in T1 clock periods).

FIGURE 9 shows an example of a configuration comprising a single real FIR filter. In this configuration, the input to Iph is routed to all filter inputs. The effective first filter section of this real FIR filter is the imaginary half of filter section 3. The imaginary half of filter section 1 is routed back to the real half of filter section 3, and the output is taken from the real half of filter section 1.

FIGURE 10 shows an example of a configuration comprising a single complex FIR filter. In the light of the above teaching, this configuration is straight forward.

FIGURE 11 shows an example of a configuration comprising a half complex FIR filter. In this configuration, complex data is input to Iph and Qph. It is multiplexed real/complex on T0 and T1 clock periods by M8 and fed to the inputs of all filter sections 1, 2 and 3. The imaginary half of filter section 3 is the effective first FIR filter section, the output of the imaginary half of filter section 1 is fed back to the real half of filter section 3, and the real output is taken from the real half of filter section 1.

FIGURE 12 shows an example of a configuration which conveys data unchanged by operating merely as a delay line



between the chip inputs and outputs. This is the the default condition that occurs on power startup of the chip. The data passes through unchanged because the coefficients are all set to zero in response to a special control signal present on power startup, which is applied to multiplexers ISC and QSC to cause these multiplexers to forward 0 values to the IIR adders, while this special control signal also causes the value of the complex coefficient defined by I_{ph} and Q_{ph} to be $1-2^{-10}+j0$, rather than being 0. The default operation passes data from input to sumout on the chip and cause data to ripple through the sum of the FIR filters to the next sumout.

It is not intended that the particular illustrative examples shown in FIGURES 4a, 4b and 5 to 12 of the filter architecture of the present invention be in any way limiting. Many different or larger filter configurations of input-weighted multiplexed filter-unit pairs that form real FIR or IIR filters, complex FIR or IIR filters or filters which are various combinations thereof, can be implemented with the designed six-section VLSI chip, and even larger filter configurations can be implemented with a plurality of such chips connected in cascade.

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CLAIMS:

1. In a reconfigurable programmable digital filter architecture suitable for use as an equalizer filter such as a multipath reducing filter; wherein said architecture includes first and second input-weighted digital filter units each of which has a given number of multiplier-coefficient taps; the combination therewith characterized by:

input means for providing signals to said digital filter; means including multiplexer means (200, 202T, 202B; 300T, 302T, 300B, 302B) (1) for configuring said first (102T) and second (102B) digital filter units for operation as a single complex digital filter (100) unit with said given number of complex multiplier coefficients for a complex sampled input signal, or (2) for configuring at least one of said first (102T) and second (102B) digital filter units for operation as a separate real digital filter unit (100) with more than said given number of real multiplier coefficients for a real sampled input signal; and

output means for receiving signals from said digital filter.

2. The digital filter architecture defined in claim 1, characterized in that:

each of said given number of multiplier-coefficient taps of each of said first and second filter units has a first multiplier-accumulator register and a second multiplier-accumulator register associated therewith.



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3. The digital filter architecture defined in claim 2, characterized in that said means including multiplexer means in configuration (1) comprises:

means for (a) applying the value of the real component of each input sample as an input to said first filter unit and applying the value of the real component of the multiplier coefficient of the first register associated with each tap of said said first filter unit to that first register during each first clock period of first and second time-multiplexed clock periods, (b) applying the value of the imaginary component of each input sample as an input to said second filter unit and applying the value of the real component of the multiplier coefficient of the first register associated with each tap of said said second filter unit to that tap during each first clock period of said first and second time-multiplexed clock periods, (c) applying the value of the imaginary component of each input sample as an input to said first filter unit and applying the the negative of the value of the imaginary component of the multiplier coefficient of the second register associated with each tap of said said first filter unit to that tap during each second clock period of said first and second time-multiplexed clock periods, and (d) applying the value of the imaginary component of each input sample as an input to said second filter unit and applying the value of the real component of the multiplier coefficient of the second register associated with each tap of said said second filter unit to that tap during each second clock period of said first and second time-multiplexed clock periods.



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4. The digital filter architecture defined in claim 3, characterized in that said means including multiplexer means further includes:

first means responsive to respective outputs of said first filter unit during each of said first and second clock periods for deriving, during a certain one of said first and second clock periods, an output sample from said first means having a value corresponding to the sum of said respective outputs of said first filter unit ; and

second means responsive to respective outputs of said second filter unit during each of said first and second clock periods for deriving, during said certain one of said first and second clock periods, an output sample from said second means having a value corresponding to the sum of said respective outputs of said second filter unit.

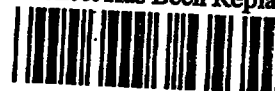
5. The digital filter architecture defined in claim 2, characterized in that said means including multiplexer means in configuration (2) comprises:

first means for (a) applying the value of each real input sample associated with one of said first and second filter unit as an input thereto during both of first and second time-multiplexed clock periods, (b) applying the value of each of a first group of said given number of real multiplier coefficients to a corresponding one of the first registers associated with the taps of said said one filter unit during each first clock period of said first and second time-multiplexed clock periods, and (c) applying the value of each of a second group of said given number of real multiplier coefficients to a corresponding one of the second registers associated with the taps of said said one filter unit during each second clock period of said first and second time-multiplexed clock periods; and

second means responsive to each output sample of said one of said first and second filter unit during each first clock period of said first and second time-multiplexed clock periods for feeding back that output sample through said one of said first and second filter unit during each second clock period of said first and second time-multiplexed clock periods.



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6. The digital filter architecture defined in claim 5, characterized in that said means including multiplexer means in configuration (2) further comprises:

third means for (d) applying the value of each real input sample associated with the other of said first and second filter units as an input thereto during both of first and second time-multiplexed clock periods, (e) applying the value of each of a third group of said given number of real multiplier coefficients to a corresponding one of the first registers associated with the taps of said said other filter unit during each first clock period of said first and second time-multiplexed clock periods, and (f) applying the value of each of a fourth group of said given number of real multiplier coefficients to a corresponding one of the second registers associated with the taps of said said other filter unit during each second clock period of said first and second time-multiplexed clock periods; and

fourth means responsive to each output sample of said other of said first and second filter unit during each first clock period of said first and second time-multiplexed clock periods for feeding back that output sample through said other of said first and second filter unit during each second clock period of said first and second time-multiplexed clock periods.

7. The digital filter architecture defined in claim 1, characterized in that each of said first and second filter units includes means for inserting a programmable delay adjustable between a minimum and a maximum number of clock periods between adjacent taps thereof.



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8. The digital filter architecture defined in claim 1, wherein said architecture further includes third and fourth digital filter units and second means including multiplexer means that correspond respectively to said first and second digital filter units and said first-mentioned means including multiplexer means; and wherein said combination further characterized by:

cascading means for coupling an output of at least one of said first and second digital filter units to an input of a corresponding one of said third and fourth digital filter units to thereby provide a reconfigurable programmable digital filter having twice said given number of multiplier-coefficient taps.

9. The digital filter architecture defined in claim 8, characterized in that:

said cascading means includes means for inserting a programmable bulk delay that is adjustable between a minimum and a maximum number of clock periods between said output of said one of said first and second digital filter units and said input of said corresponding one of said third and fourth digital filter units.

10. A VLSI circuit (Fig. 1; each of Figs. 4a, 4b; 5-12) having a given architecture for defining a reconfigurable programmable digital filter for a periodically sampled input signal; wherein each sample period is divided into two successive clock periods; and wherein said given architecture comprises a first given plural number of filter sections and a single IIR input and global section; and characterized by:

each of said filter sections includes a pair of first and second input-weighted filter units (102T, 102B) that respectively have a second given plural number of taps and two multiplier-accumulator registers between taps thereof and a programmable delay between taps thereof that can be adjusted between first and second relatively small numbers of sample periods, programmable multiplexer means (1) for configuring each pair of first and second digital filter units as a single complex digital filter unit with said second given plural number of complex multiplier coefficients for a complex sampled input signal, or (2) for configuring at least one



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of said first and second digital filter units as a separate real digital filter unit with twice said second given plural number of real multiplier coefficients for a real sampled input signal, and programmable delay means for introducing a sample delay that can be adjusted between one clock period and a relatively large numbers of sample periods; and

said single IIR input and global section includes in-phase (Iph) and quadrature-phase (Qph) means for programmably adjusting the phase of samples applied as inputs thereto, and programmable routing multiplexers (1) (ISC,QSC) for selectively applying the output of a certain one of said filter sections as inputs to said in-phase and quadrature-phase means, and (2) (M2-M8) for selectively cascading at least some of said first given plural number of filter sections to alternatively configure said cascaded filter sections as a certain real FIR or IIR filter, complex FIR or IIR filter, or a particular combination of real and complex FIR and/or IIR filters.

11. The VLSI circuit defined in Claim 10, characterized in that:

said given architecture further comprises a cascade input and a cascade output; and

said programmable routing multiplexers further applies a filter output of said circuit to said cascade output thereof;

whereby said cascade output may be forwarded to a cascade input of another VLSI circuit having said given architecture.

12. The VLSI circuit defined in Claim 10, characterized in that:

said programmable multiplexer means of each of said filter sections and said programmable routing multiplexers are selectively operated to provide a default-condition configuration in which said filter sections perform only as a delay line to pass data therethrough unchanged between said cascade input and said cascade output.



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