

CLAIMS

1. A computer system, comprising:

a processor in communication with one or more types of memory, the processor configured to:

execute a virtual machine (VM) configuration comprising at least a first logical core and a second logical core, each of the first logical core and the second logical core enabled to operate in a single thread (ST) mode or a multithreading (MT) mode, the ST mode including a single physical thread and the MT mode including a plurality of physical threads on shared resources of one or more physical cores;

execute a core-oriented system control area (COSCA) comprising a common area representing at least the first logical core and the second logical core, the COSCA further comprising a first core description area for the first logical core and a second core description area for the second logical core, the first core description area indicating a location of a first set of one or more thread description areas and the second core description area indicating a location of a second set of one or more thread description areas, wherein each thread description area in the first set contains a state description address indicating a location of a state description of a logical thread in the first logical core and each thread description area in the second set contains a state description address indicating a location of a state description of a logical thread in the second logical core, wherein the COSCA is implemented as a tree structure comprising a first leaf representing the first logical core and a second leaf representing the second logical core, and wherein the first leaf contains a first list of a first set of one or more logical threads in the first logical core and the second leaf contains a second list corresponding to a second set of one or more logical threads in the second logical core;

execute, by a hypervisor configured to control the VM configuration using the COSCA, a first core dispatch instruction to dispatch the first logical core on a physical core, wherein the hypervisor operates in the ST mode and the first core dispatch instruction specifies that the first logical core is to be dispatched in the MT mode;

execute a first logical thread of the first logical core to issue an inter-processor-interrupt instruction to signal a second logical thread of the second logical core;

modify a state description associated with a thread description area in the second set that is associated with the second logical thread to make an inter-processor-interrupt that is associated with the inter-processor-interrupt instruction pending;

execute, by the hypervisor, a second core dispatch instruction to dispatch the second logical core on the physical core;

enable the second logical core for the inter-processor-interrupt; and
 present the inter-processor-interrupt to the first logical core.

2. The computer system of claim 1, wherein the common area further includes a core validity mask that indicates a validity of each of the first logical core and the second logical core.

3. The computer system of claim 1, wherein the first core description area further includes a thread validity mask that indicates a validity of one or more logical threads in the first logical core.

4. The computer system of claim 1, wherein each state description further indicates a location of the common area.

5. A computer-implemented method for managing multiple threads in a virtual machine (VM) configuration, the method comprising:

providing, the VM configuration comprising at least a first logical core and a second logical core, each of the first logical core and the second logical core enabled to operate in a single thread (ST) mode or a multithreading (MT) mode, the ST mode including a single physical thread and the MT mode including a plurality of physical threads on shared resources of one or more physical cores;

providing a core-oriented system control area (COSCA) comprising a common area representing at least the first logical core and the second logical core, the COSCA further comprising a first core description area for the first logical core and a second core description area for the second logical core, the first core description area indicating a location of a first set of one or more thread description areas and the second core description area indicating a location of a second set of one or more thread description areas, wherein each thread description area in the first set contains a state description address indicating a location of a state description of a logical thread in the first logical core and each thread description area in the second set contains a state description address indicating a location of a state description of a logical thread in the second logical core, wherein the COSCA is implemented as a tree structure comprising a first leaf representing the first logical core and a second leaf representing the second logical core, and wherein the first leaf contains a first list of a first set of one or more logical threads in the first logical core and the second leaf contains a second list corresponding to a second set of one or more logical threads in the second logical core;

executing, by a hypervisor configured to control the VM configuration using the COSCA, a first core dispatch instruction to dispatch the first logical core on a physical core, wherein the hypervisor operates in the ST mode and the first core dispatch instruction specifies that the first logical core is to be dispatched in the MT mode;

executing a first logical thread of the first logical core to issue an inter-processor-interrupt instruction to signal a second logical thread of the second logical core;

modifying a state description associated with a thread description area in the second set that is associated with the second logical thread to make an inter-processor-interrupt that is associated with the inter-processor-interrupt instruction pending;

executing, by the hypervisor, a second core dispatch instruction to dispatch the second logical core on the physical core;

enabling the second logical core for the inter-processor-interrupt; and

present the inter-processor-interrupt to the first logical core.

6. The method of claim 5, wherein the common area further includes a core validity mask that indicates a validity of each of the first logical core and the second logical core.

7. The method of claim 5, wherein the first core description area further includes a thread validity mask that indicates a validity of one or more logical threads in the first logical core.

8. A computer program product comprising a non-transitory storage medium readable by a processing circuit and storing instructions for execution by the processing circuit for performing a method comprising:

providing a virtual machine (VM) configuration comprising at least a first logical core and a second logical core, each of the first logical core and the second logical core enabled to operate in a single thread (ST) mode or a multithreading (MT) mode, the ST mode including a single physical thread and the MT mode including a plurality of physical threads on shared resources of one or more physical cores;

providing a core-oriented system control area (COSCA) comprising a common area representing at least the first logical core and the second logical core, the COSCA further comprising a first core description area for the first logical core and a second core description area for the second logical core, the first core description area indicating a location of a first set

of one or more thread description areas and the second core description area indicating a location of a second set of one or more thread description areas, wherein each thread description area in the first set contains a state description address indicating a location of a state description of a logical thread in the first logical core and each thread description area in the second set contains a state description address indicating a location of a state description of a logical thread in the second logical core, wherein the COSCA is implemented as a tree structure comprising a first leaf representing the first logical core and a second leaf representing the second logical core, and wherein the first leaf contains a first list of a first set of one or more logical threads in the first logical core and the second leaf contains a second list corresponding to a second set of one or more logical threads in the second logical core;

executing, by a hypervisor configured to control the VM configuration using the COSCA, a first core dispatch instruction to dispatch the first logical core on a physical core, wherein the hypervisor operates in the ST mode and the first core dispatch instruction specifies that the first logical core is to be dispatched in the MT mode;

executing a first logical thread of the first logical core to issue an inter-processor-interrupt instruction to signal a second logical thread of the second logical core;

modifying a state description associated with a thread description area in the second set that is associated with the second logical thread to make an inter-processor-interrupt that, is associated with the inter-processor interrupt pending;

executing, by the hypervisor, a second core dispatch instruction to dispatch the second logical core on the physical core;

enabling the second logical core for the inter-processor-interrupt; and

present the inter-processor interrupt to the first logical score.

9. The computer program product of claim 8, wherein the common area further includes a core validity mask that indicates a validity of each of the first logical core and the second logical core.

10. The computer program product of claim 8, wherein the first core description area further includes a thread validity mask that indicates a validity of one or more logical threads in the first logical core.