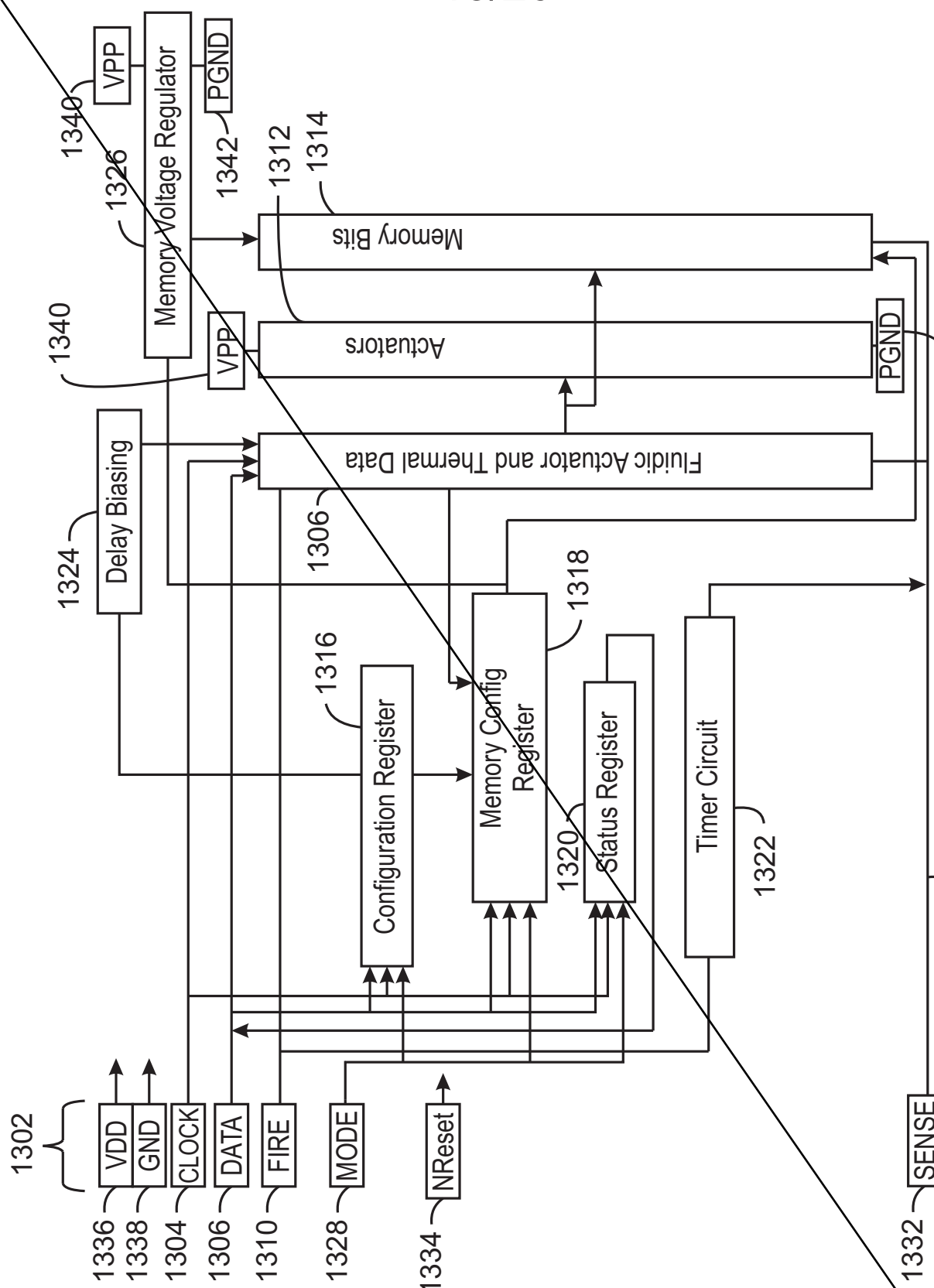
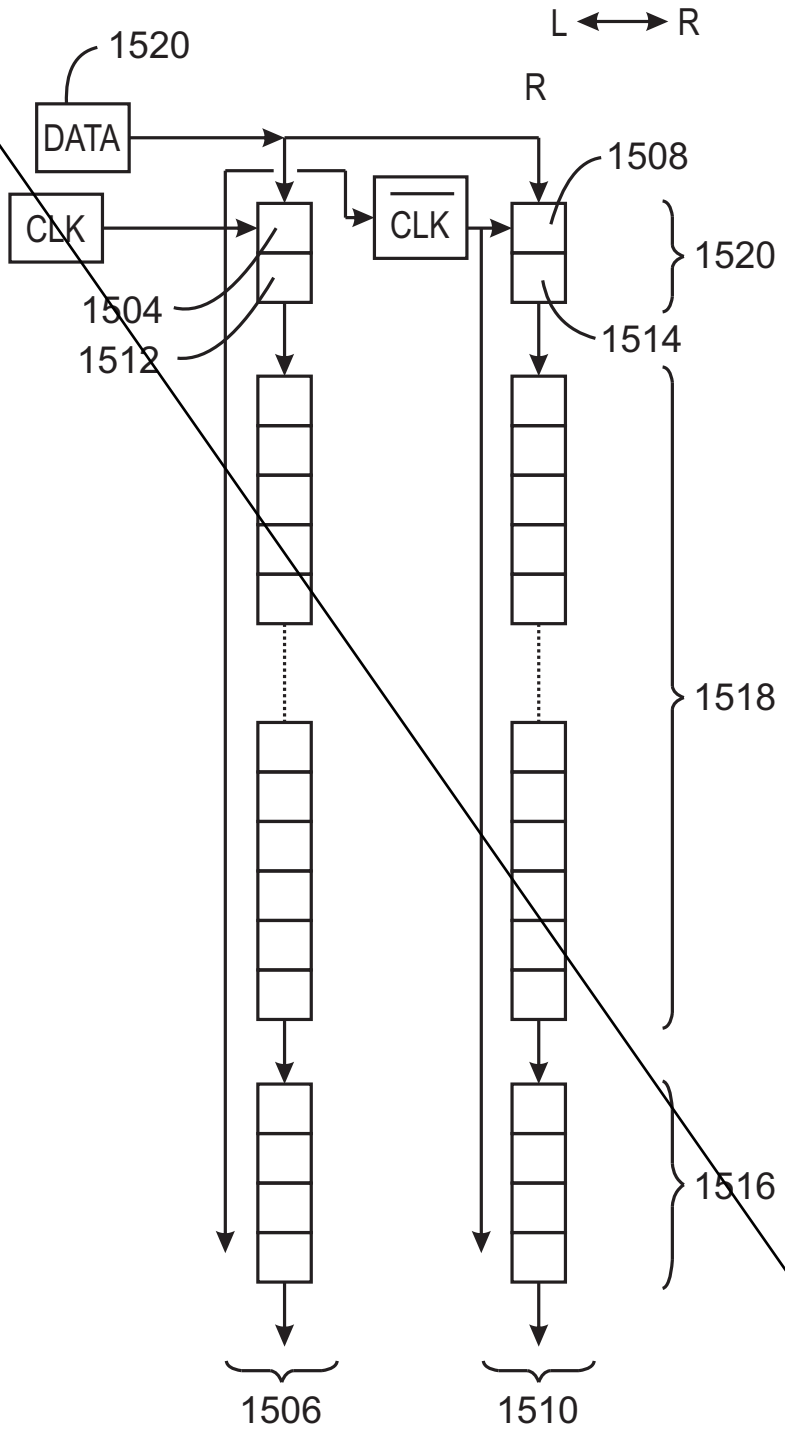

1300
1302
VDD
GND
CLOCK
DATA
FIRE
MODE
NReset
SENSE
1336
1338
1304
1306
1310
1328
1334
1332
1330
Configuration Register
1316
Memory Config Register
1318
Status Register
1320
Timer Circuit
1322
Delay Biasing
1324
Memory Voltage Regulator
1326
VPP
PGND
1340
1342
Memory Bits
1312
1314
Actuators
Fluidic Actuator and Thermal Data
1306

FIG. 13


L
R
R
1520
DATA
CLK
CLK
1508
1520
1504
1512
1514
1518
1516
1506
1510

1308

FIG. 15

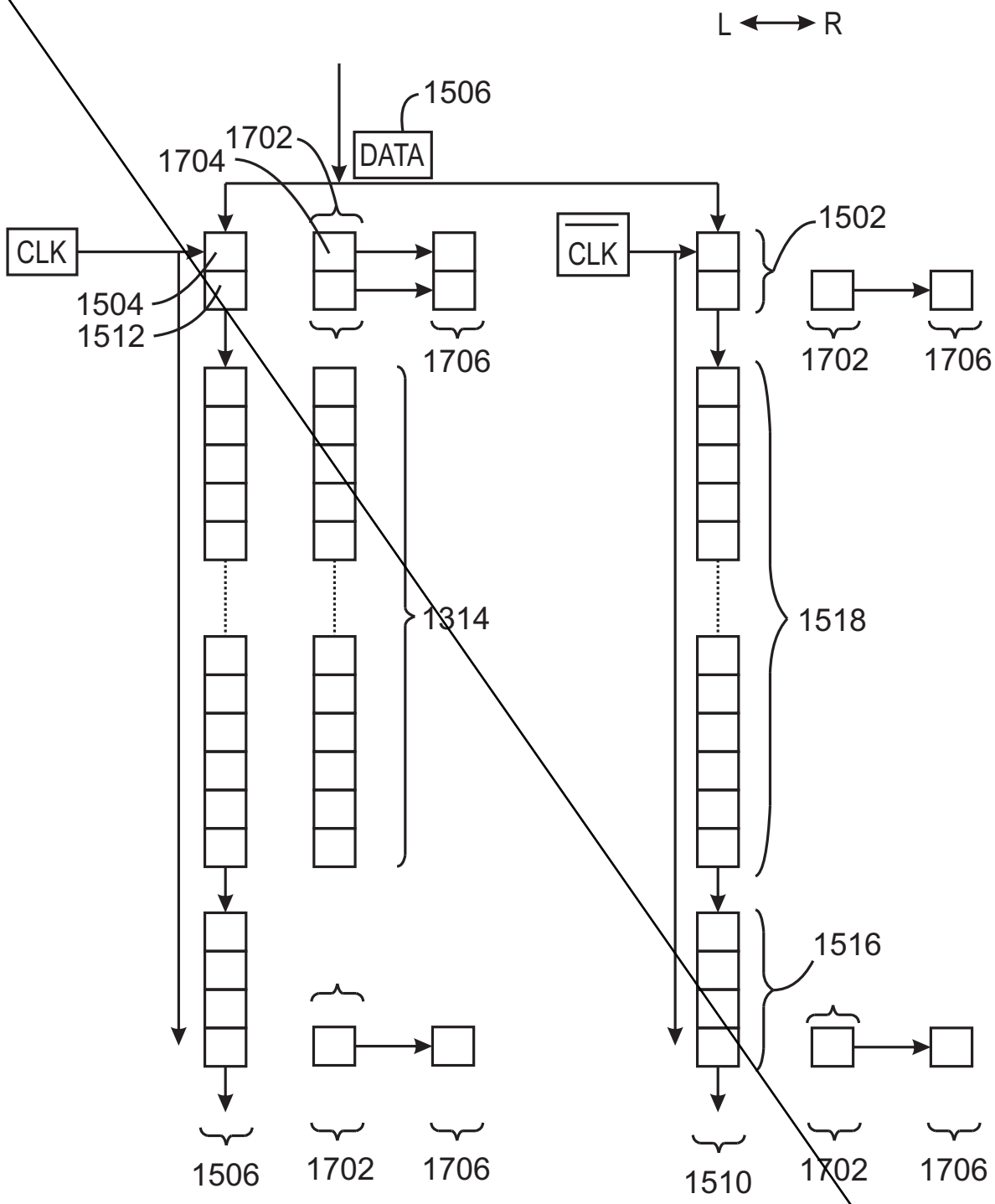

L
R
1506
DATA
1702
1704
CLK
1504
1512
1706
1314
1506
1702
1706
CLK
1502
1702
1706
1518
1516
1510
1702
1706

FIG. 17

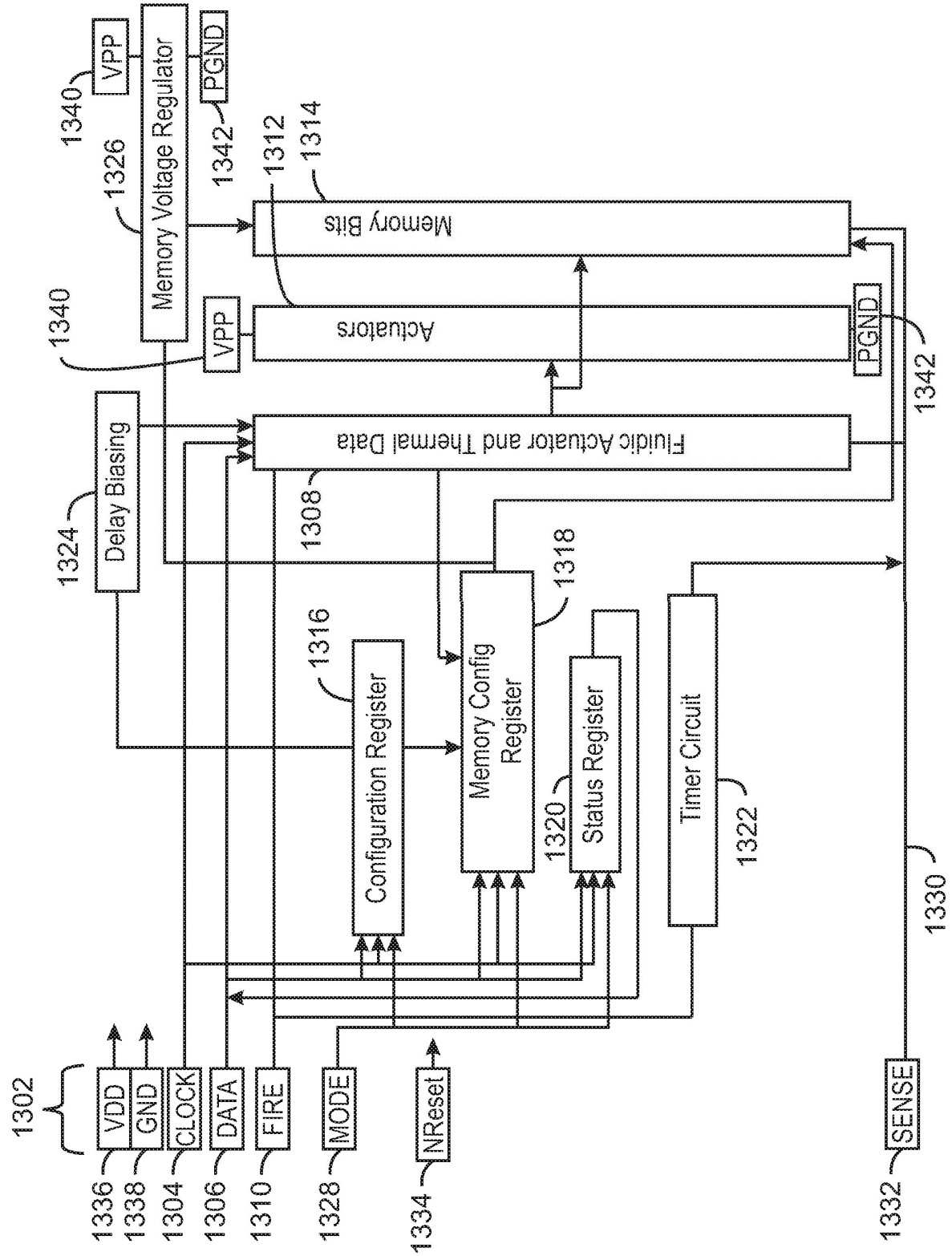
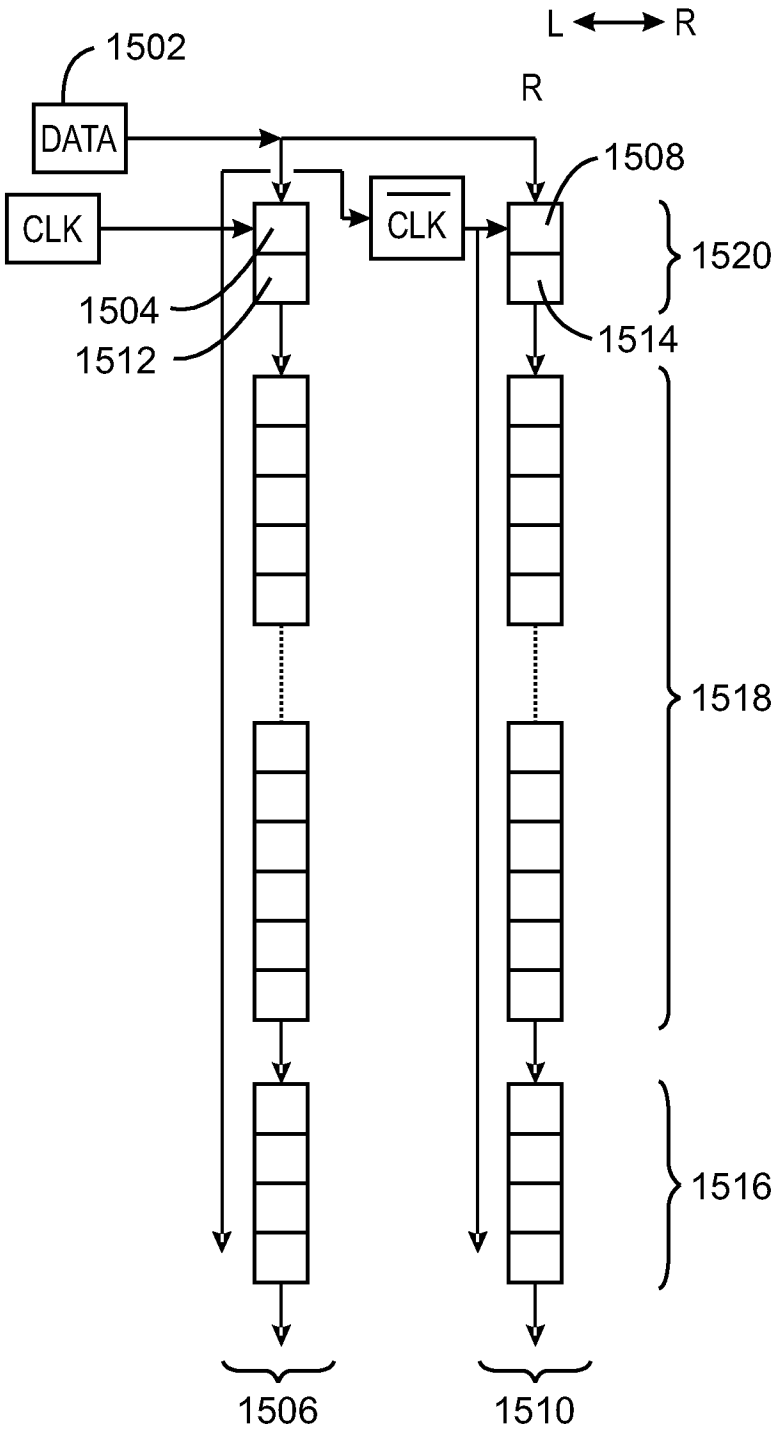

1300
1302
VDD
GND
CLOCK
DATA
FIRE
MODE
NReset
SENSE
1336
1338
1304
1306
1310
1328
1334
1332
Delay Biasing
1324
Memory Voltage Regulator
1326
VPP
PGND
1340
1342
Memory Bits
1312
1314
Actuators
Fluidic Actuator and Thermal Data
1308
Configuration Register
1316
Memory Config Register
1318
Status Register
1320
Timer Circuit
1322
1330

FIG. 13


L
R
R
1502
DATA
CLK
CLK
1508
1520
1504
1512
1514
1518
1516
1506
1510

1308

FIG. 15

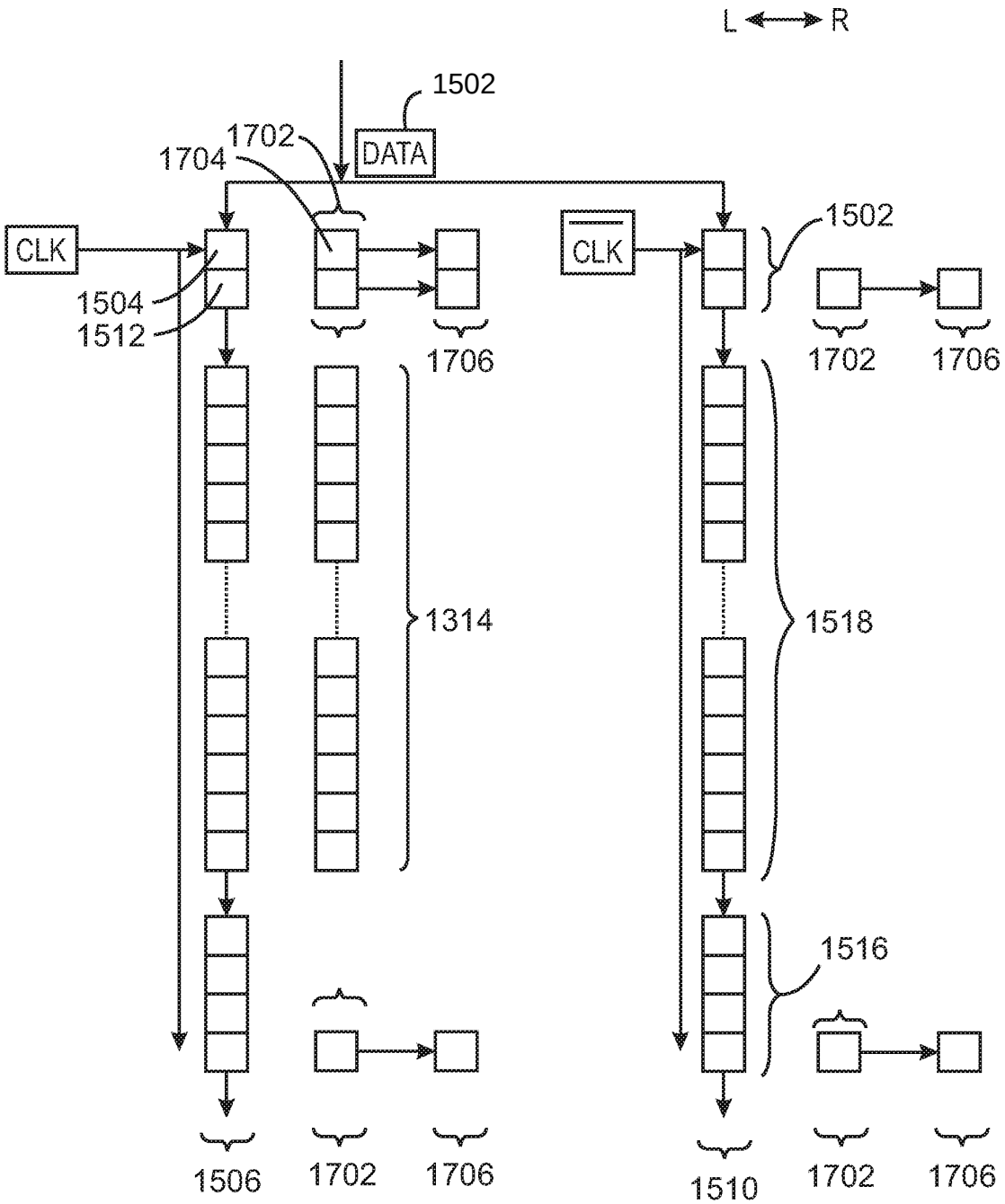

L
R
1502
DATA
1702
1704
CLK
1504
1512
1706
1314
1506
1702
1706
CLK
1502
1702
1706
1518
1516
1510
1702
1706

FIG. 17