ABSTRACT

A memory device includes a phase change memory (PCM) cell connected between a bit line and a word line. An X-decoder provides a word line voltage to the word line during a reset operation, and a Y-decoder provides a bit line voltage to the bit line during the reset operation. A voltage bias circuit generates the word line voltage and the bit line voltage based on a first bias during a first period of the reset operation, the word line voltage and the bit line voltage based on a second bias greater than the first bias during a second period of the reset operation, and the word line voltage and the bit line voltage based on a third bias smaller than the first and second biases during a third period of the reset operation.

FIG. 1