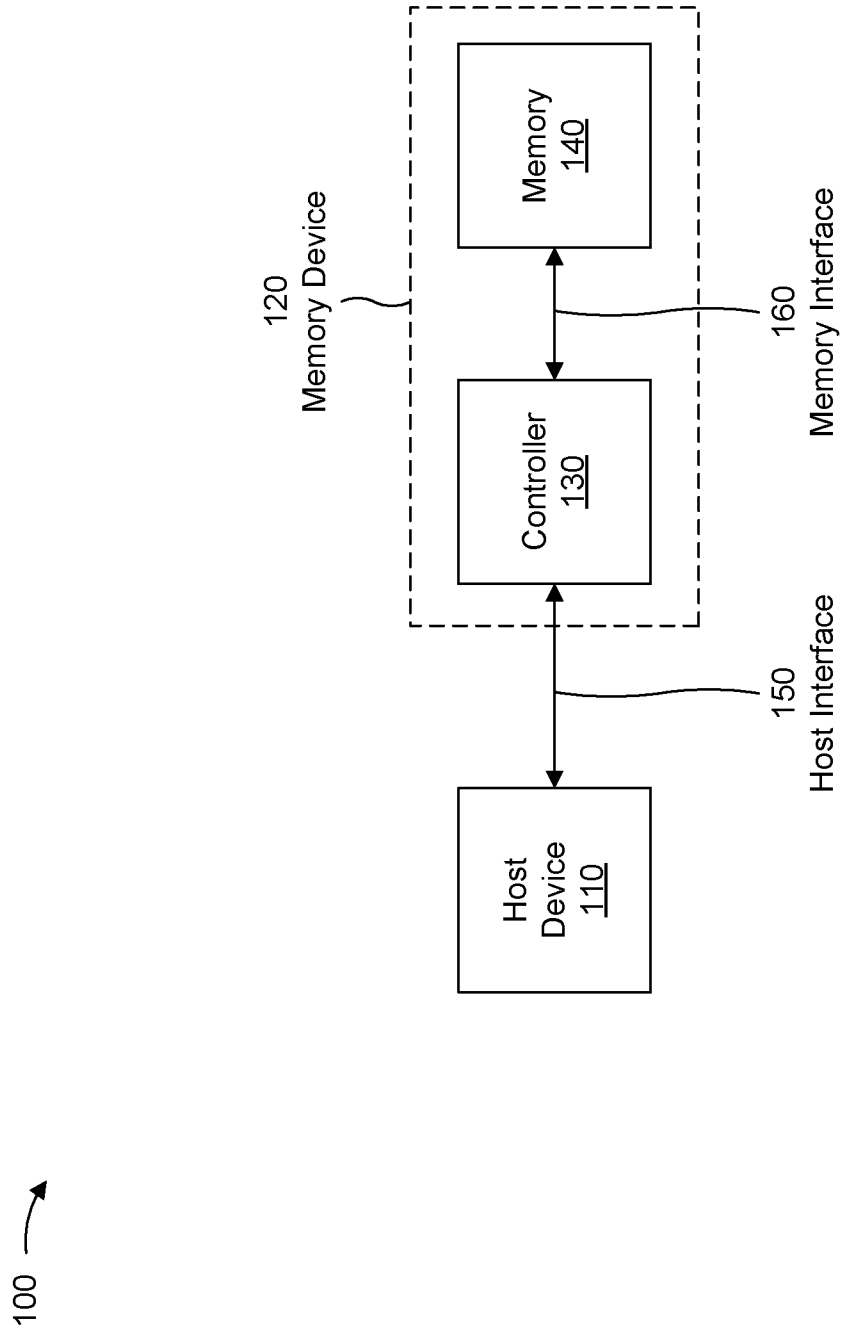
100
120
Memory Device
Memory
140
Controller
130
160
Memory Interface
150
Host Interface
Host
Device
110

FIG. 1

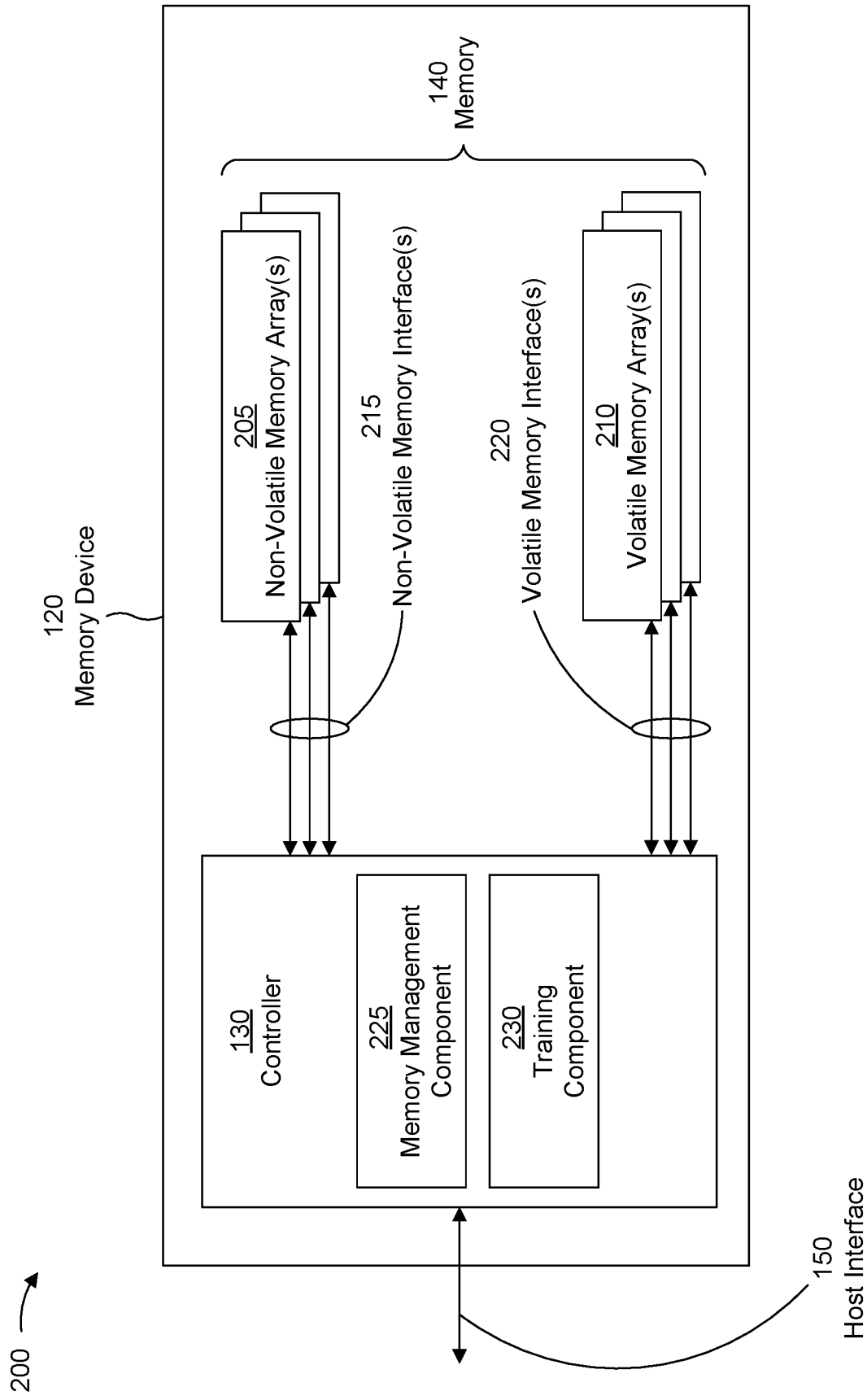
200
120
Memory Device
140
Memory
205
Non-Volatile Memory Array(s)
215
Non-Volatile Memory Interface(s)
220
Volatile Memory Interface(s)
210
Volatile Memory Array(s)
130
Controller
225
Memory Management Component
230
Training Component
150
Host Interface

FIG. 2

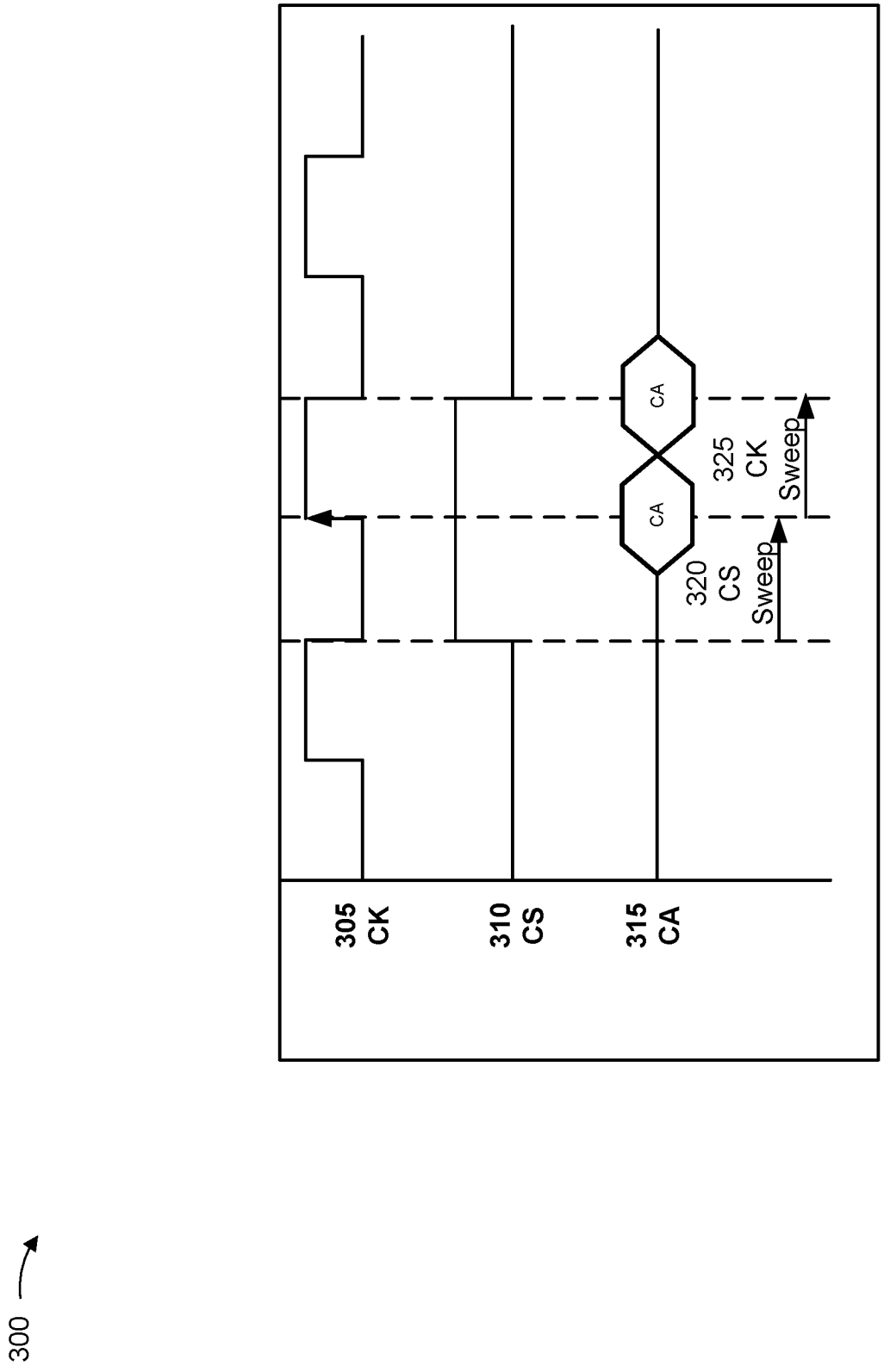

FIG. 3

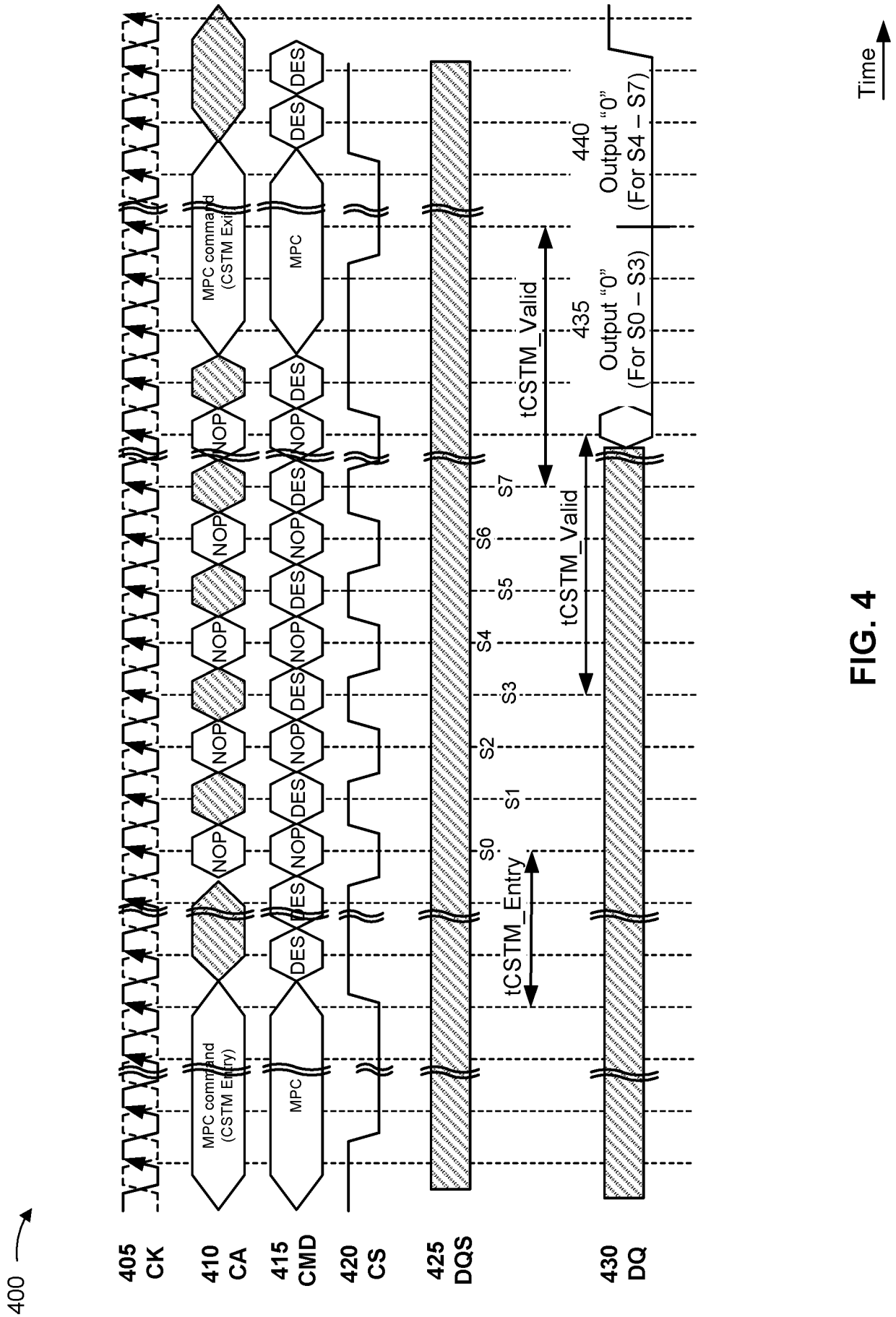
400
405 CK
410 CA
415 CMD
420 CS
425 DQS
430 DQ
MPC command (CSTM Entry)
MPC command (CSTM Exit)
MPC
NOP
DES
S0
S1
S2
S3
S4
S5
S6
S7
tCSTM_Entry
tCSTM_Valid
tCSTM_Valid
435
Output "0" (For S0 – S3)
440
Output "0" (For S4 – S7)
Time

FIG. 4

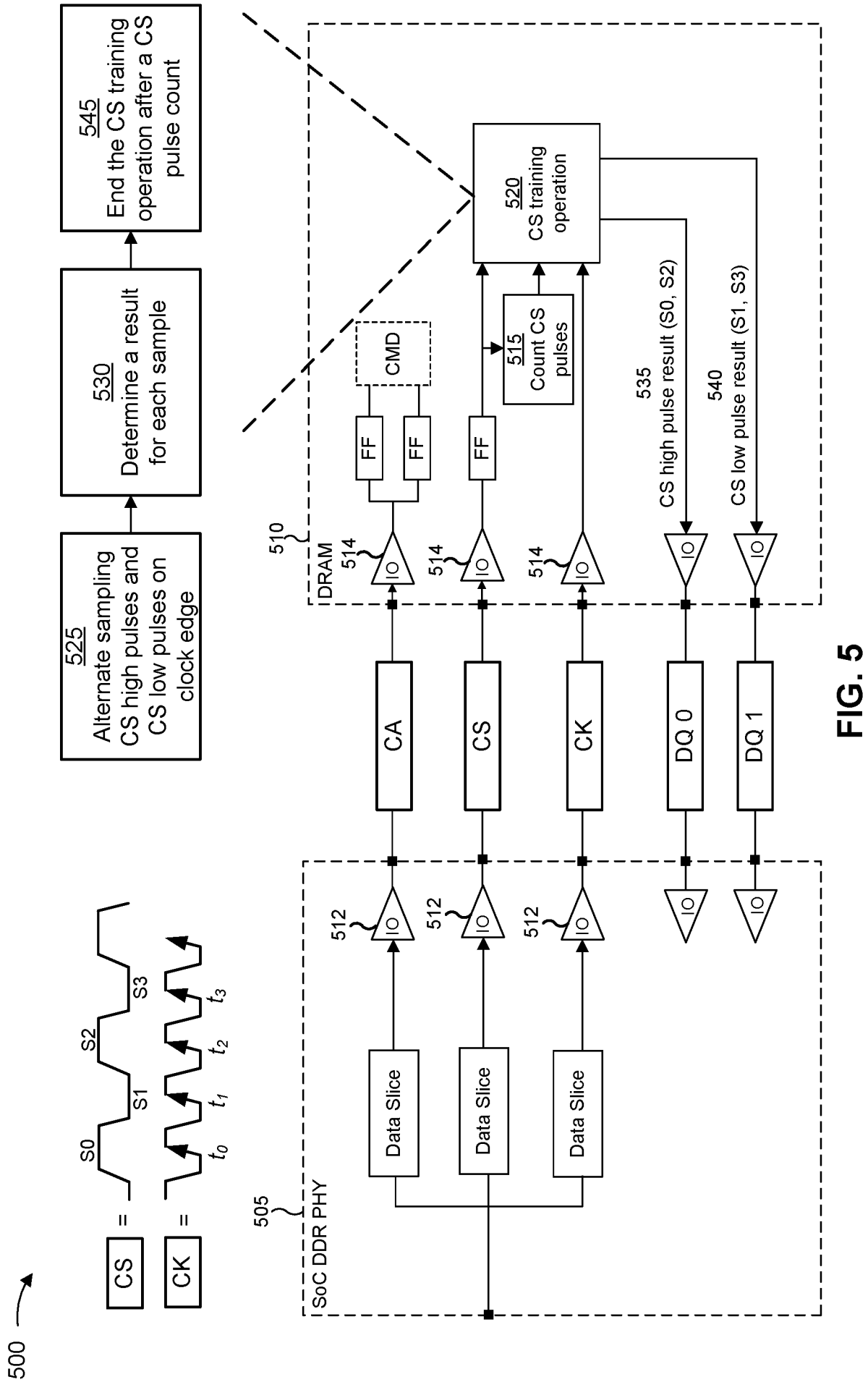
500
CS
CK
S0
S1
S2
S3
t_0
t_1
t_2
t_3
505
SoC DDR PHY
Data Slice
Data Slice
Data Slice
512
IO
CA
CS
CK
DQ 0
DQ 1
510
DRAM
514
FF
CMD
515
Count CS pulses
520
CS training operation
535
CS high pulse result (S0, S2)
540
CS low pulse result (S1, S3)
525
Alternate sampling CS high pulses and CS low pulses on clock edge
530
Determine a result for each sample
545
End the CS training operation after a CS pulse count

FIG. 5

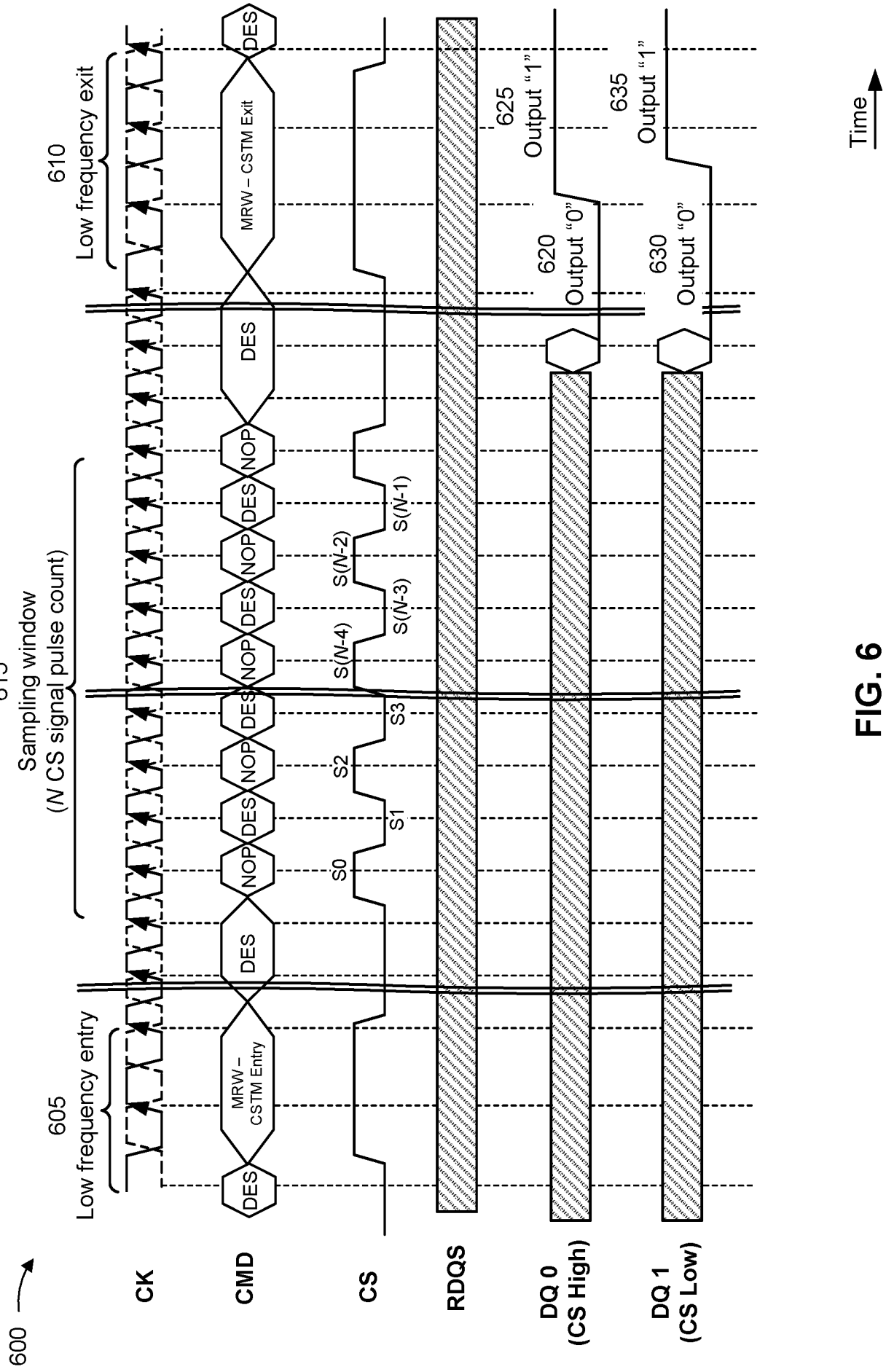
600
CK
CMD
CS
RDQS
DQ 0
(CS High)
DQ 1
(CS Low)
605
Low frequency entry
610
Low frequency exit
615
Sampling window
(N CS signal pulse count)
MRW – CSTM Entry
MRW – CSTM Exit
DES
NOP
S0
S1
S2
S3
S(N-4)
S(N-3)
S(N-2)
S(N-1)
620
Output "0"
625
Output "1"
630
Output "0"
635
Output "1"
Time

FIG. 6

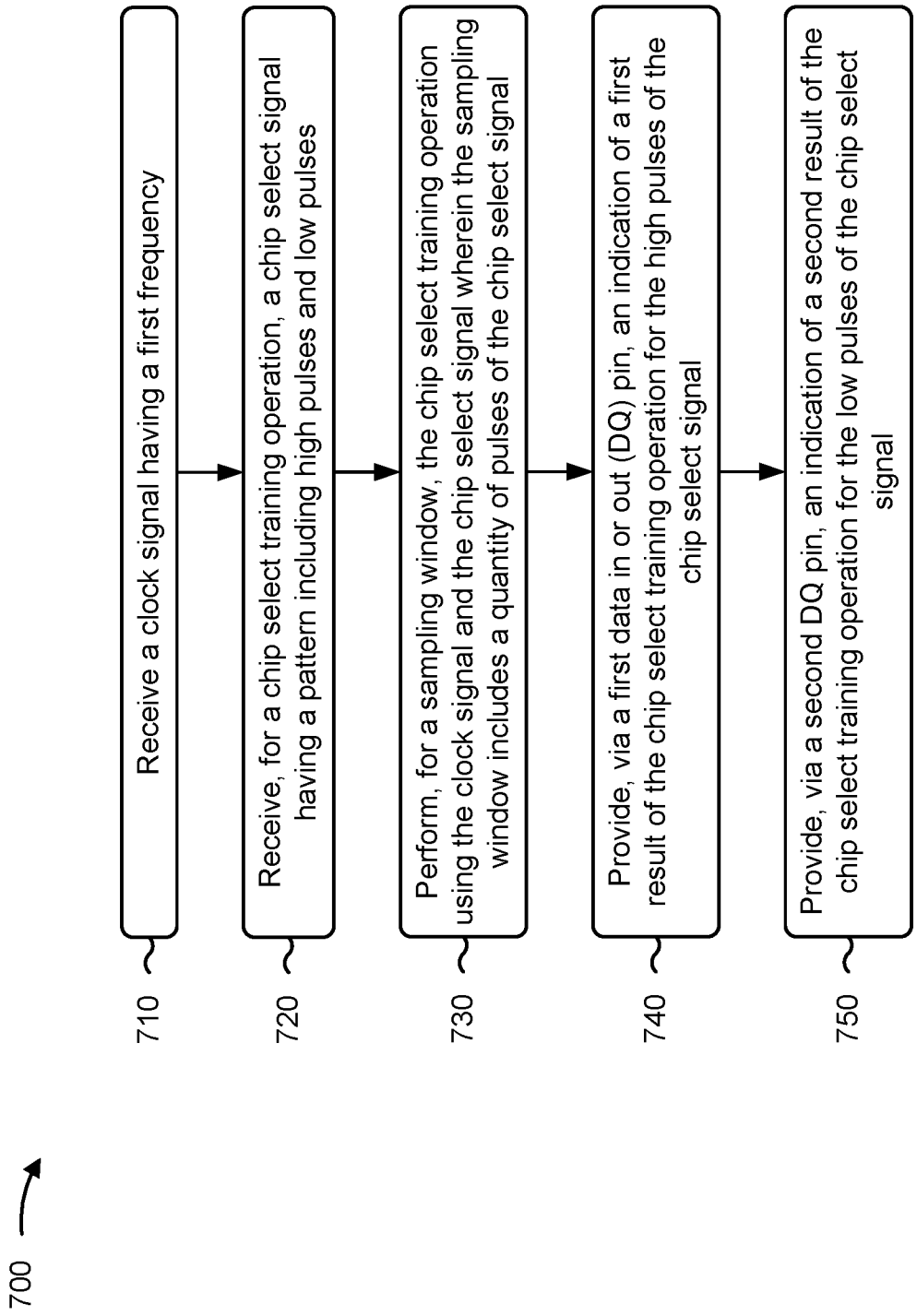
700
710
Receive a clock signal having a first frequency
720
Receive, for a chip select training operation, a chip select signal having a pattern including high pulses and low pulses
730
Perform, for a sampling window, the chip select training operation using the clock signal and the chip select signal wherein the sampling window includes a quantity of pulses of the chip select signal
740
Provide, via a first data in or out (DQ) pin, an indication of a first result of the chip select training operation for the high pulses of the chip select signal
750
Provide, via a second DQ pin, an indication of a second result of the chip select training operation for the low pulses of the chip select signal

FIG. 7

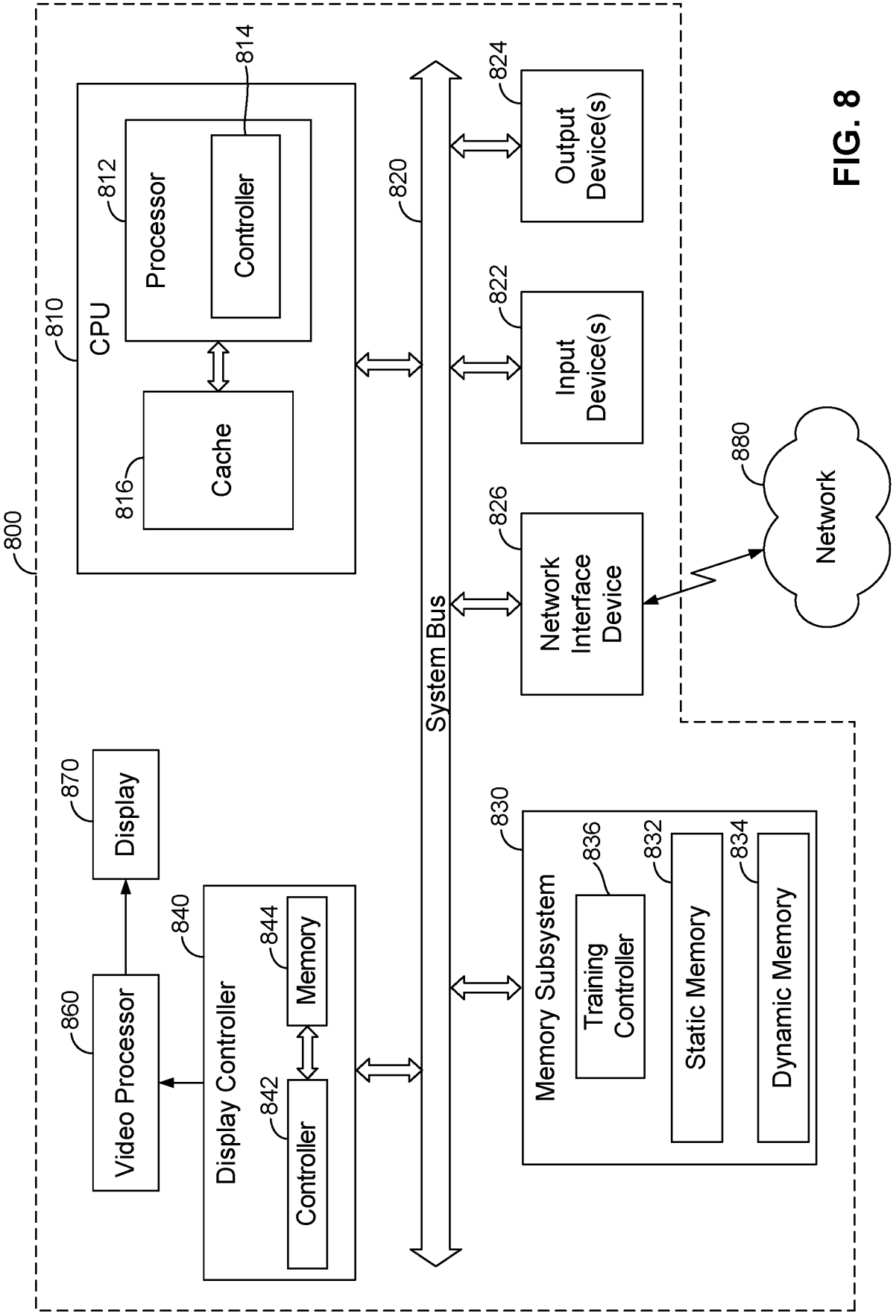
800
CPU
810
Processor
812
Controller
814
Cache
816
System Bus
820
Output Device(s)
824
Input Device(s)
822
Network Interface Device
826
Network
880
Memory Subsystem
830
Training Controller
836
Static Memory
832
Dynamic Memory
834
Display Controller
840
Memory
844
Controller
842
Video Processor
860
Display
870

FIG. 8